Integrated Device Technology, Inc.

BiCMOS HIGH-SPEED STATIC RAM 72K (8K x 9-BIT) With Address Latches

ADVANCE INFORMATION
IDT71B569

FEATURES:

- 8192-words x 9-bits organization
- JEDEC standard 28-pin DIP and SOJ
- Fast access time:
  - — Commercial: 12/15/20ns
  - — Military: 15/20ns
- Produced with advanced BiCEMOS™ high-performance technology
- Single 5V power supply
- Inputs and outputs directly TTL compatible
- Latched address inputs
- High-speed BiCEMOS process
- Available in 28-pin, 300 mil plastic and SOJ packages

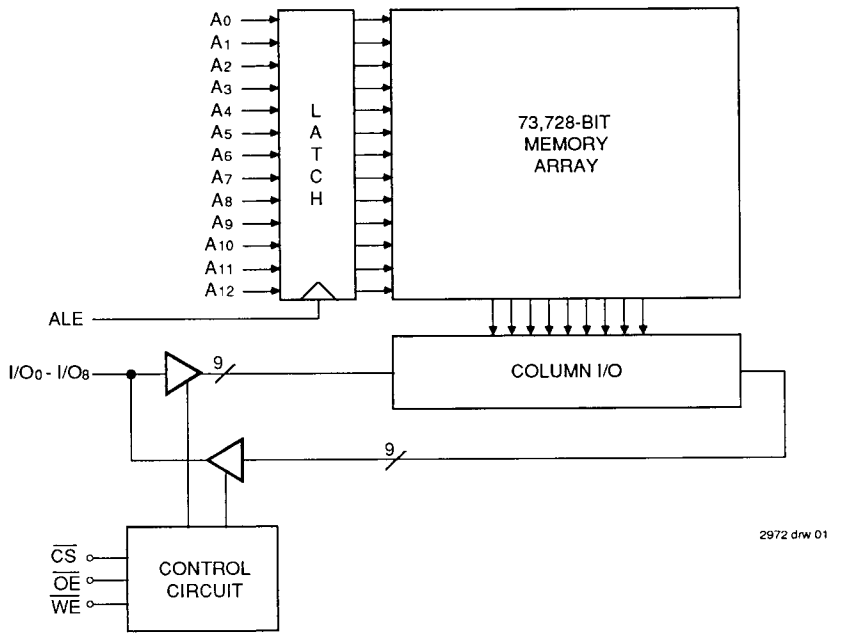
DESCRIPTION:

The IDT71B569 is a 73,728-bit high-speed static RAM, organized as 8K x 9, with address latches. It is fabricated using IDT's high-performance, high-reliability BiCEMOS technology.

The IDT71B569 offers address access times as fast as 12ns. The ninth bit is optimal for systems using parity. This device is ideally suited for cache memory applications.

All inputs and outputs of the IDT71B569 are TTL-compatible. The IDT71B569 is packaged in an industry standard 300-mil, 28-pin DIP and SOJ.

FUNCTIONAL BLOCK DIAGRAM



6

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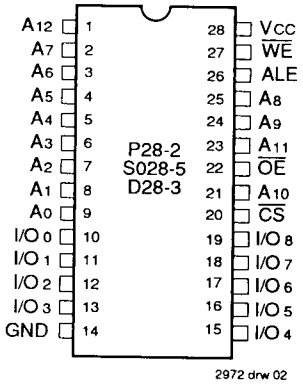
PIN CONFIGURATION



2972 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2972 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2972 tbl 04

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2972 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2972 tbl 05

1. 1.5V undershoots are allowed for 10ns once per cycle.

TRUTH TABLE

ALE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	Hi-Z	Deselect chip
H	X	X	X	X	Address Latch Transparent
L	X	X	X	X	Address Latch Closed
H	L	L	H	DOUT	Read From Current Address
L	L	L	H	DOUT	Read From Latched Address
H	L	X	L	DIN	Write To Current Adress
L	L	X	L	DIN	Write To Latched Adress
X	L	H	H	Hi-Z	Outputs Disabled

NOTE: 2972 tbl 01

1. H = VIH, L = VIL, X = Don't Care

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B569S12		71B569S15		71B569S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}(2)	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	170	—	170	190	150	170	mA

2972 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B569S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2972 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2972 tbl 07

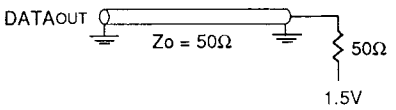
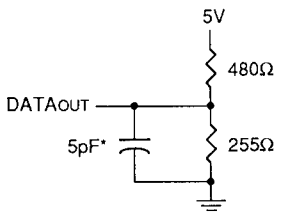


Figure 1A. AC Test Load

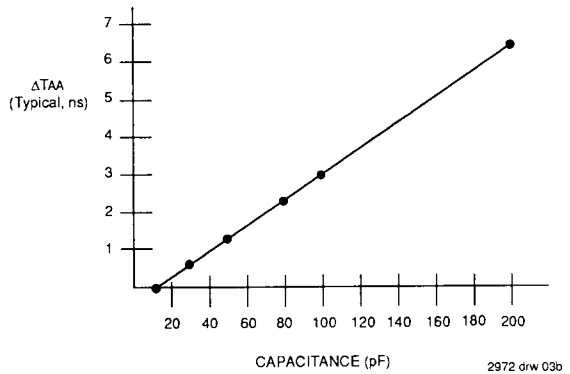
2972 drw 03a



2972 drw 04

*Includes jig and scope capacitance.

Figure 1B.



2972 drw 03b

Figure 1C. Lumped Capacitive Load, Typical Derating

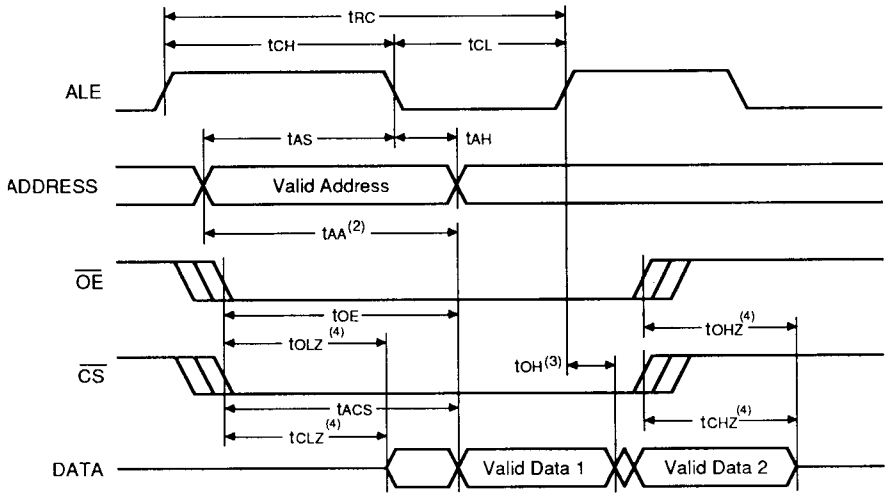
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B569S12[1]		71B569S15		71B569S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time[3]	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t_{CLZ}	Chip Select to Output in Low Z[2]	2	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	7	ns
t_{OLZ}	Output Enable to Output in Low Z[2]	2	—	3	—	3	—	ns
t_{CHZ}	Chip Deselect to Output High Z[2]	—	6	—	7	—	10	ns
t_{OHZ}	Output Disable to Output in High Z[2]	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{CH}	ALE High Time[2]	6	—	7	—	10	—	ns
t_{CL}	ALE Low Time[2]	6	—	7	—	10	—	ns
t_{AS}	Address Set-up Time to Address Latch Enable	3	—	3	—	5	—	ns
t_{AH}	Address Hold Time to Address Latch Enable	2	—	2	—	5	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	10	—	12	—	20	—	ns
t_{CW}	Chip Select to End of Write	10	—	12	—	15	—	ns
t_{ASW}	Address Set-up Time[3]	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	11	—	15	—	ns
t_{WR}	Write Recovery Time[3]	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z[2]	—	6	—	7	—	10	ns
t_{DW}	Data to Write Time Overlap	6	—	8	—	11	—	ns
t_{DH}	Data Hold Time from Write Time	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write[2]	2	—	3	—	5	—	ns
t_{CH}	ALE High Time	6	—	7	—	10	—	ns
t_{CL}	ALE Low Time	6	—	7	—	10	—	ns
t_{AS}	Address Set-up Time to Address Latch Enable	3	—	3	—	5	—	ns
t_{AH}	Address Hold Time to Address Latch Enable	2	—	2	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.
3. This measurement depends on the combination of ALE high plus an address change. This combination may either happen at the rising edge of ALE, or during an address change after ALE has become high.

2972 tbl 09

TIMING WAVEFORM OF READ CYCLE (1)



NOTES:
1. $\overline{WE}$ is high throughout a read cycle.
2. The parameter tAA is measured either from the first low to high transition of ALE after the read address has become valid, or from the stabilization of the read address during the period when ALE is high, which ever occurs last.
3. The parameter tOH is measured either from the first low to high transition of ALE after an address change, or from an address change during the period when ALE is high, whichever occurs first.
4. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

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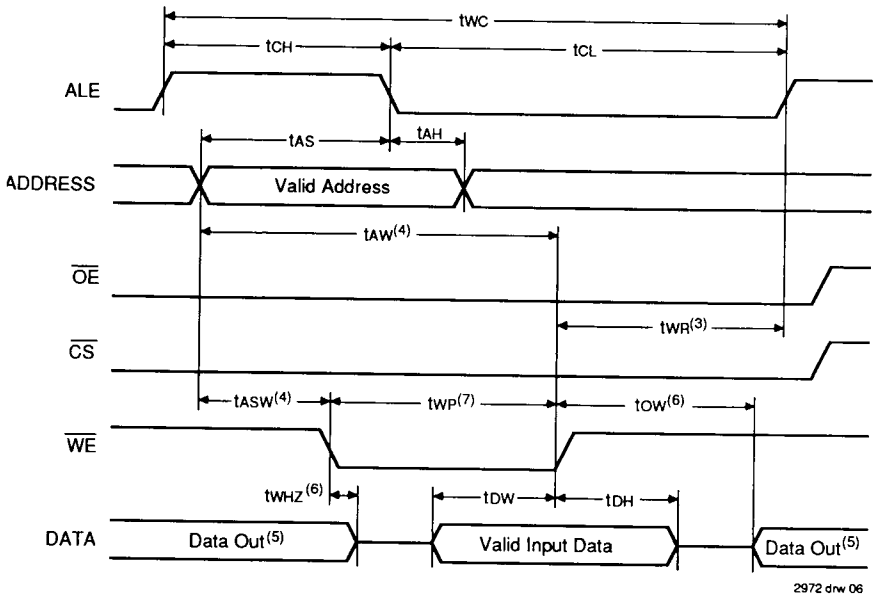
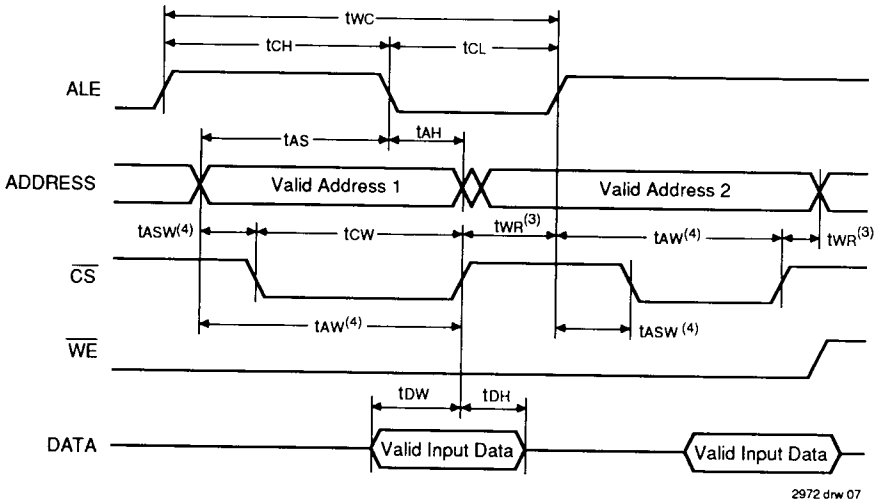
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1,2)



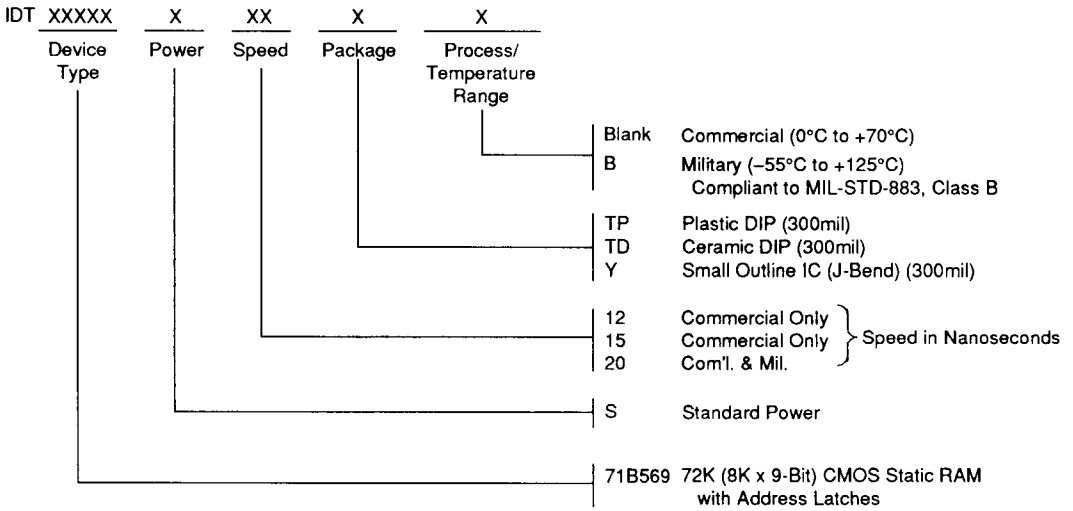
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,2)



NOTES:

1. $\overline{WE}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tBW, tCW or tWP) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. The parameter tWR is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high either to the first low to high transition of ALE after an address change, or to an address change during the period when ALE is high, whichever occurs last.
4. The parameters tASW and tAW are measured either from the first low to high transition of ALE after an address change has become valid, or from the stabilization of the valid write address during the period when ALE is high, whichever occurs first.
5. During this period, the I/O pins are in the output state so that the input signals must not be applied.
6. This transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWP.

ORDERING INFORMATION



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