IH5025-IH5038
Positive Signal Analog Switch

GENERAL DESCRIPTION

The IH5025 series of analog switches was designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver.

The entire family is designed to be driven from TTL open collector logic (15V), but can be driven from 5V logic if signal input is less than 1V. Alternatively, 20V switching is readily obtainable if TTL supply voltage is +25V. Normally, only positive signals can be switched; however, up to ±10V can be handled by the addition of a PNP stage (Figure 14) or by capacitor isolation (Figure 13). Each channel is a SPST switch. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

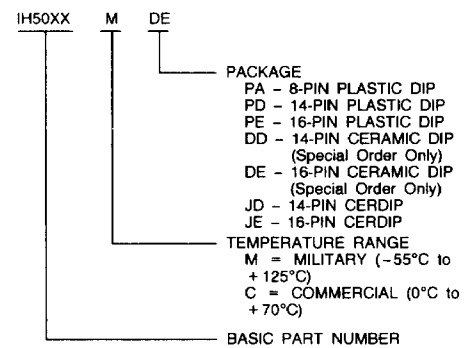
FEATURES

- **Switches Up to +20V Into High Impedance Loads (i.e. Non-Inverting Input of Operational Amp.)**
- **Driven From TTL Open Collector Logic**
- **$I_{D(OFF)}$ < 50pA**
- **$r_{DS(ON)}$ < 150Ω**
- **$r_{DS(ON)}$ Match < 50Ω Channel to Channel**
- **Switching Speeds < 100ns**

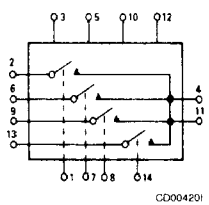
ORDERING INFORMATION

BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5025	4	+15	JD,DD,PD
IH5026	4	+5	JD,DD,PD
IH5027	4	+15	JE,DE,PE
IH5028	4	+5	JE,DE,PE
IH5029	3	+15	JD,DD,PD
IH5030	3	+5	JD,DD,PD
IH5031	3	+15	JE,DE,PE
IH5032	3	+5	JE,DE,PE
IH5033	2	+15	JD,DD,PA
IH5034	2	+5	JD,DD,PA
IH5035	2	+15	JE,DE,PA
IH5036	2	+5	JE,DE,PA
IH5037	1	+15	JD,DD,PA
IH5038	1	+5	JD,DD,PA

NOTE: Mil-Temperature range (−55°C to +125°C) available in ceramic packages only.

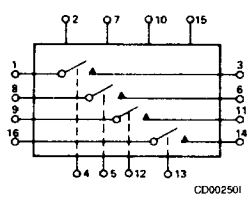


IH5025 ($r_{DS(ON)}$ ≤ 100Ω)
IH5026 ($r_{DS(ON)}$ ≤ 150Ω)
14 PIN DIP



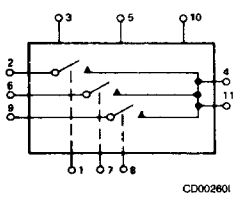
CD00420I

IH5027 ($r_{DS(ON)}$ ≤ 100Ω)
IH5028 ($r_{DS(ON)}$ ≤ 150Ω)
16 PIN DIP



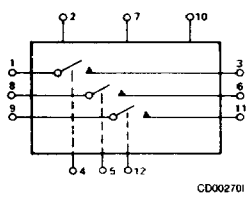
CD00250I

IH5029 ($r_{DS(ON)}$ ≤ 100Ω)
IH5030 ($r_{DS(ON)}$ ≤ 150Ω)
14 PIN DIP



CD00260I

IH5031 ($r_{DS(ON)}$ ≤ 100Ω)
IH5032 ($r_{DS(ON)}$ ≤ 150Ω)
16 PIN DIP

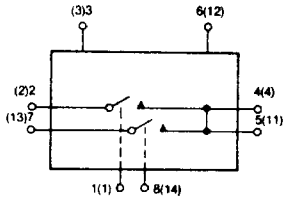


CD00270I

Figure 1: Pin Connections

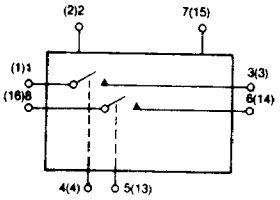
Note: All typical values have been guaranteed by characterization and are not tested.

IH5033 ($r_{DS(ON)} \leq 100\Omega$)
IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



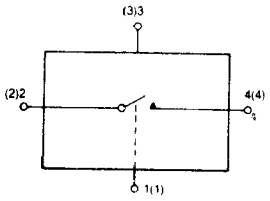
CD00280I

IH5035 ($r_{DS(ON)} \leq 100\Omega$)
IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



CD00290I

IH5037 ($r_{DS(ON)} \leq 100\Omega$)
IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



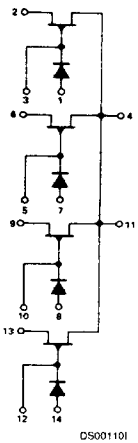
CD00410I

NUMBERS IN PARENTHESES INDICATE CERAMIC PACKAGE PIN-OUT

Figure 1: Pin Connections (Cont.)

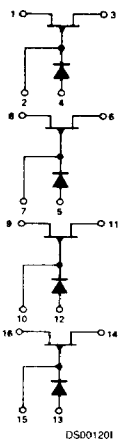
FOUR CHANNEL

IH5025 ($r_{DS(ON)} \leq 100\Omega$)
IH5026 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



DS00110I

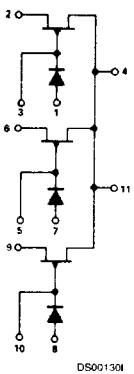
IH5027 ($r_{DS(ON)} \leq 100\Omega$)
IH5028 ($r_{DS(ON)} \leq 150\Omega$)
14PIN DIP



DS00120I

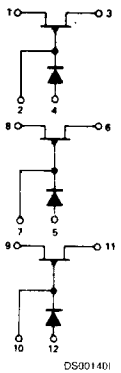
THREE CHANNEL

IH5029 ($r_{DS(ON)} \leq 100\Omega$)
IH5030 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



DS00130I

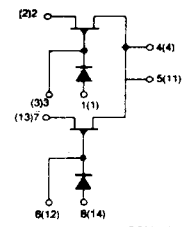
IH5031 ($r_{DS(ON)} \leq 100\Omega$)
IH5032 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



DS00140I

TWO CHANNEL

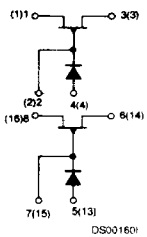
IH5033 ($r_{DS(ON)} \leq 100\Omega$) IH5034 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00150I

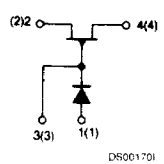
SINGLE CHANNEL

IH5035 ($r_{DS(ON)} \leq 100\Omega$) IH5036 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00160I

IH5037 ($r_{DS(ON)} \leq 100\Omega$) IH5038 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



DS00170I

Numbers in parentheses indicate CERAMIC PACKAGE LAYOUT

Figure 2: Device Schematics

Note: All typical values have been guaranteed by characterization and are not tested.

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 25V
Negative Analog Signal Voltage ..... -0.5VDC
Drain Current 25mA
Power Dissipation (Note) 500mW
Storage Temperature ..... -65°C to +150°C

Operating Temperature
5025C Series ..... 0°C to +70°C
5025M Series ..... -55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

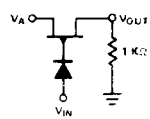
NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5m/W°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE	TEST CONDITIONS	SPECIFICATION LIMIT				UNIT MIN/MAX
				-55°C (M) 0°C (C)	25°C TYP	25°C MIN/MAX	+125°C (M) +70°C (C)	
$I_{IN(ON)}$	Input Current-ON	All	V_{IN} = 0V		0.30	1.0	100 (M) 25 (C)	nA (max)
$I_{IN(OFF)}$	Input Current-OFF	All	V_{IN} = 15V		0.20	1.0	50 (M) 50 (C)	nA (max)
$V_{IN(ON)}$	Channel Control Voltage-ON	All	See Figure 3	1.5		1.5	1.5	V (max)
$V_{IN(OFF)}$	Channel Control Voltage-OFF	All	See Figure 3	14.0		14.0	14.0	V (min)
$I_{D(OFF)}$	Leakage Current-OFF	All	See Figure 5		0.06	0.5	100 (M) 50 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Odd Nos.	See Figure 6		1.00	10.0	5000 (M) 250 (C)	nA (max)
$I_{D(ON)}$	Leakage Current-ON	Even Nos.	See Figure 6		0.10	1.0	500 (M) 25 (C)	nA (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	V_{IN} = 0.5V, I_D = 1mA	100	60.00	100.0	250 (M) 150 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	V_{IN} = 0.5V, I_D = 1mA	150	90.00	150.0	385 (M) 240 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.	V_{IN} = 1.0V, I_D = 1mA	160	85.00	160.0	420 (M) 250 (C)	Ω (max)
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.	V_{IN} = 1.0V, I_D = 1mA		110.00	200.0	400 (M) 250 (C)	Ω (max)
$t_{(on)}$	Turn-ON Time	All	See Figure 4		0.10	0.2	0.4	μs (max)
$t_{(off)}$	Turn-OFF Time	All	See Figure 4		0.10	0.2	0.4	μs (max)
$Q_{(INJ)}$	Charge Injection	All	See Figure 5		7.0	20.0		mV_{p-p} (max)
$V_{A(OFF)}$	Cross Coupling Rejection	All	See Figure 6		0.10	1.0		mV_{p-p} (max)
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	All	V_{IN} = 0.5V, I_D = 1mA		25.00			Ω (max)

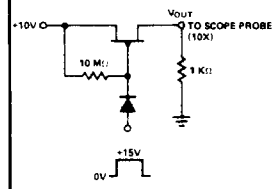
Note 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.



FET "ON" FOR $V_{IN} \leq 1.5V$
FET "OFF" FOR $V_{IN} \geq 14.0V$

TC00450I

Figure 3: Test Circuits



TC00460I

Figure 4: Test Circuits

Note: All typical values have been guaranteed by characterization and are not tested.

IH5025-IH5038

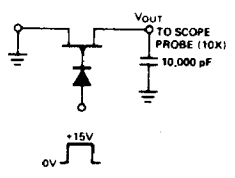


Figure 5: Test Circuits

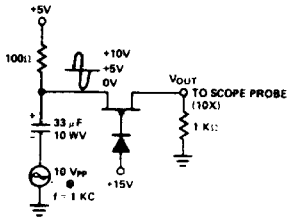
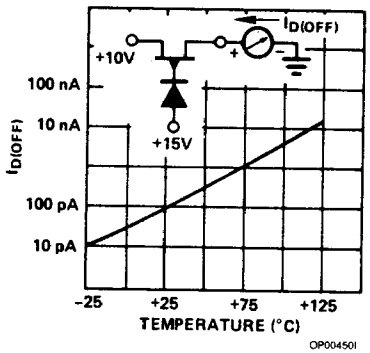


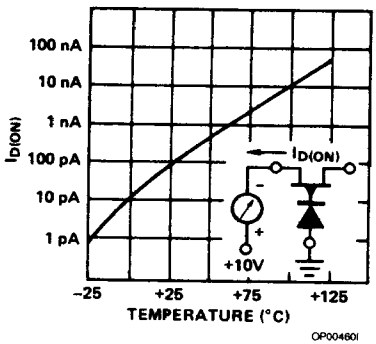
Figure 6: Test Circuits

TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

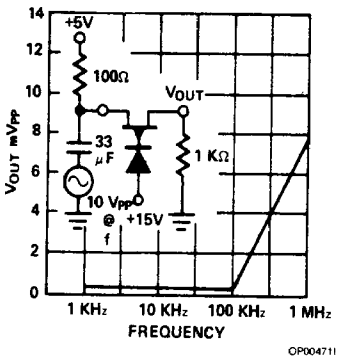
$I_{D(OFF)}$ VS. TEMPERATURE



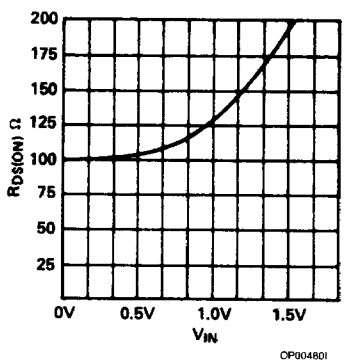
$I_{D(ON)}$ VS. TEMPERATURE



CROSS COUPLING REJECTION VS. FREQUENCY



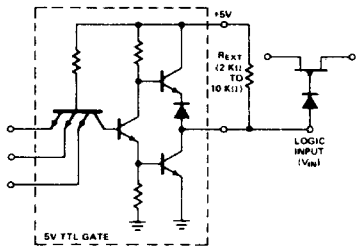
$R_{DS(ON)}$ VS. V_{IN}



Note: All typical values have been guaranteed by characterization and are not tested.

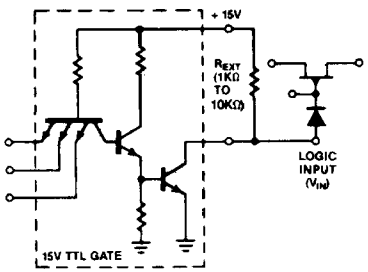
LOGIC INTERFACE CIRCUITS

When operating with TTL logic it is necessary to use pull-up resistors as shown in Figures 6 and 7. This ensures the necessary positive voltages for proper gating action.



LC000301

Figure 7: Interfacing with +5V Logic



LC000411

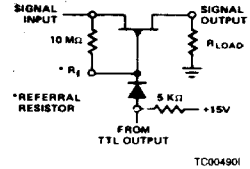
Figure 8: Interfacing with +15V Open Collector Logic

THEORY OF OPERATION

The IH5025 series differs from the IH5009 series in that they may be driven by floating outputs. This family is generally used when operating into the non-inverting input of an operational amplifier, while the IH5009 series is used in operations where the output feeds into the inverting (virtual ground) input.

The IH5025 model is a basic charge area switching device, in that proper gating action depends upon the capacitance vs. voltage relationship for the diode junctions. This C vs. V, when integrated, produces total charge Q. It is Q total which is switched between the series diode and the gate to source and gate to drain junctions. The charge area (C vs. V) for the diode has been chosen to be a minimum of four (4) times the area of the gate to source junction, thus providing adequate safety margins to insure proper switching action.

If normal logical voltage levels of ground to +15V (open collector TTL) are used, only signals which are between 0V and +10V can be switched. The pinch-off range of the P-Channel FET has been selected between 2.0V and 3.9V; thus with +15V at the logical input, and a +10V signal input, 1.1V of margin exists for turn-off. When the IH5025 is used with 5V TTL logic, a maximum of +1V can be switched. The gate of each FET has been brought out so that a "referral resistor" can be placed between gate and source. This is used to minimize charge injection effects. The connection is shown below:

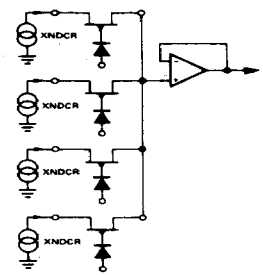


TC004901

Figure 9

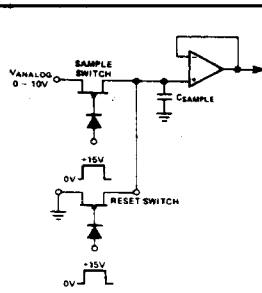
For switching levels > +10V, the +15V power supply must be increased so that there is a minimum of 5V of difference between supply and signal. For example, to switch +15V level, +20V TTL supply is required. Up to +20V levels can be gated.

APPLICATIONS



AF001201

Figure 10: Multiplexer from Positive Output Transducers



AF001301

Figure 11: Sample and Hold Switch

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS (CONT.)

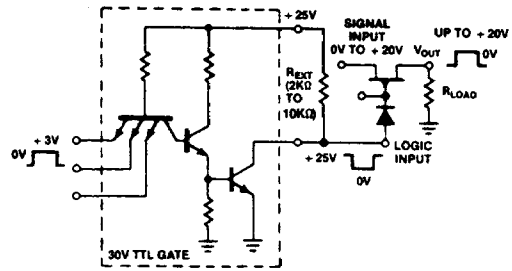


Figure 12: Switching up to +20V Signals with TTL Logic

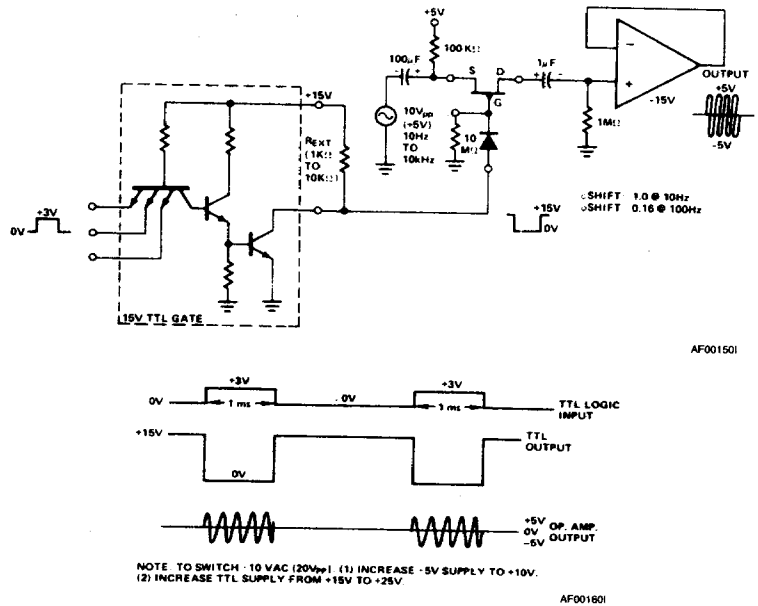
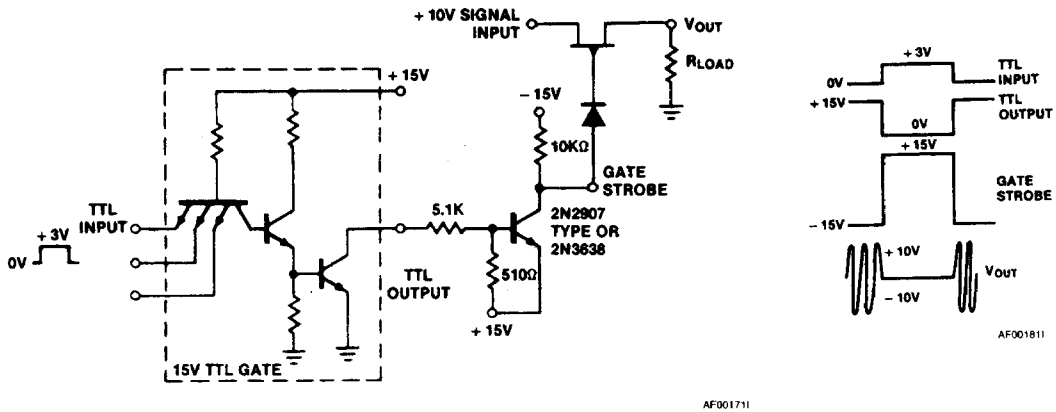


Figure 13: Switching Bipolar Signals with TTL Logic

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS (CONT.)



ADVANTAGES OVER FIGURE NO. 10 METHOD

A. DC LEVELS OF UP TO ±10V CAN BE SWITCHED, AS WELL AS AC SIGNALS UP TO 100kHz; NO. 10 METHOD SWITCHES ONLY AC RANGE OF 10MHz TO 10kHz.

B. CKT IS NOW BREAK BEFORE MAKE

DISADVANTAGES

A. PNP CKT DRAWS 3mA, WHEN ON; THUS ADDS 3mA x 30V = 90mW POWER DISS.

B. t_{ON} TIME WILL BE CONSIDERABLY SLOWED DOWN FROM 100ns (BEFORE IN FIGURE NO. 13 TO) 1–2μs NOW.

Figure 14: Switching Bipolar Signals with TTL Logic (Alternate Method)

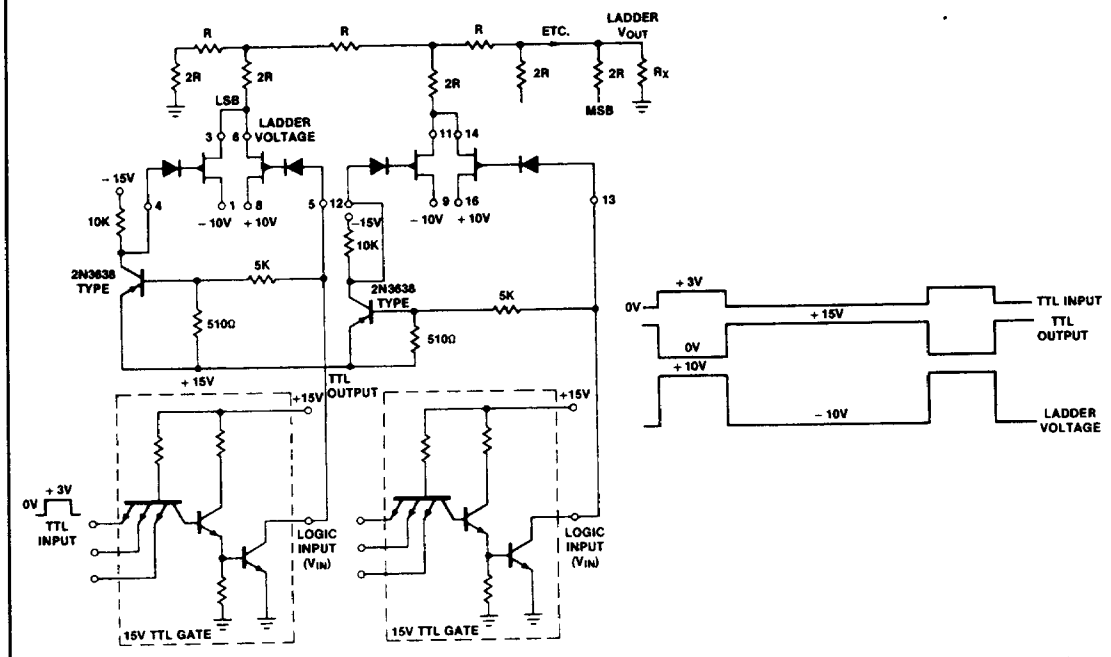


Figure 15: Using the IH5028 as a Dual SPDT Switch to Drive Ladder Networks for Bipolar Switching (up to ±10V)

Note: All typical values have been guaranteed by characterization and are not tested.

APPLICATIONS (CONT.)

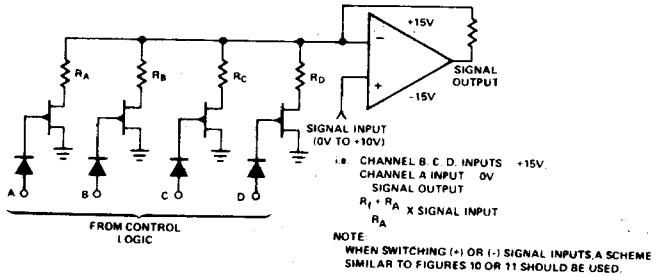


Figure 16: Gain Control with High Input Impedance

Note: All typical values have been guaranteed by characterization and are not tested.