REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Changed figure 1; Removed note 3 for case outlines X and Y. Added vendor cage 88379 for device types 01 through 04. -sld	99-03-29	K. A. Cottongim
E	Added device type 05. Updated drawing to the latest requirements of MIL-PRF-38534. -sld	03-03-17	Raymond Monnin
F	Figure 1; case outline X, changed the dimension "D" min from 1.654 inches to 1.6 inches. Added cage 0EU86 for device types 01 through 04. Editorial changes troughout. -sld	04-10-21	Raymond Monnin
G	Added device type 06. Added case outline Z. Editorial changes throughout. -sld	05-02-18	Raymond Monnin

REV																				
SHEET																				
REV	G	G	G	G	G	G														
SHEET	15	16	17	18	19	20														

REV STATUS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Steve L. Duncan

CHECKED BY
Michael C. Jones

APPROVED BY
Kendall A. Cottongim

DRAWING APPROVAL DATE
96-04-22

REVISION LEVEL
G

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, FLASH EPROM, 512K x 8-BIT, MONOLITHIC SILICON

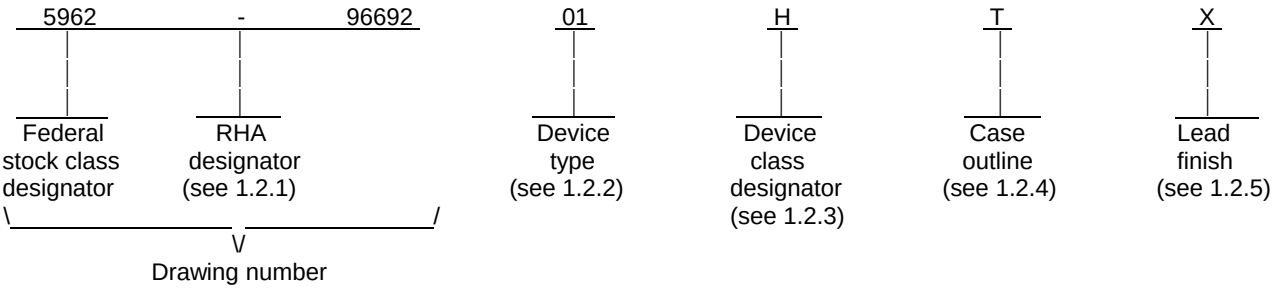
SIZE	CAGE CODE	
A	**67268**	**5962-96692**

SHEET 1 OF 20

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	F512K8-150, F040-150	EPROM, FLASH, 512K x 8-bit	150 ns
02	F512K8-120, F040-120	EPROM, FLASH, 512K x 8-bit	120 ns
03	F512K8-090, F040-90	EPROM, FLASH, 512K x 8-bit	90 ns
04	F512K8-070, F040-70	EPROM, FLASH, 512K x 8-bit	70 ns
05	F512K8-060, F040-60	EPROM ,FLASH, 512K x 8-bit	60 ns
06	F040-55	EPROM, FLASH, 512K x 8-bit	55 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	32	Ceramic flatpack, lead formed
U	See figure 1	32	Ceramic flatpack
X	See figure 1	32	Co-fired ceramic, single cavity
Y	See figure 1	32	Co-fired ceramic, single cavity, SOJ
Z	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) 2/	-2.0 V dc to +7.0 V dc
Signal voltage range (any pin except A9) 2/	-2.0 V dc to +7.0 V dc
Power dissipation (P_D)	0.33 W maximum at 5 MHz
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Data retention	10 years minimum
Endurance (write/erase cycles)	10,000 cycles minimum
A9 voltage for sector protect (V_{ID}) 3/	-2.0 V dc to +14.0 V dc

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.0 V dc to V_{CC} + 0.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
A9 voltage for sector protect (V_{ID})	+11.5 V dc to +12.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Minimum DC voltage on input or I/O pins is -0.5 V dc. During voltage transitions, input may overshoot V_{SS} to -2.0 V dc for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V dc. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V dc for periods of up to 20 ns.

3/ Minimum DC input voltage on A9 pin is -0.5 V dc. During voltage transitions, A9 may overshoot V_{SS} to -2.0 V dc for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V dc which may overshoot to +14.0 V dc for periods up to 20 ns.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4, 5, and 6 .

3.2.5 Block diagram. The block diagram shall be as specified on figure 7.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 8.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Programming procedure. The programming procedure shall be as specified by the manufacturer and shall be available upon request.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.7 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.8 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.9 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the initial characterization and after any design process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DC parameters							
Input leakage current	I_{LI}	V_{CC} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	µA
Output leakage current	I_{LO}	V_{CC} = 5.5 V dc, V_{IN} = GND to V_{CC}	1,2,3	All		10	µA
V_{CC} active current for read	I_{CC1}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V_{CC} = 5.5 V dc	1,2,3	All		35	mA
V_{CC} active current for program or erase 3/	I_{CC2}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, V_{CC} = 5.5 V dc	1,2,3	All		50	mA
V_{CC} standby current	I_{SB}	V_{CC} = 5.5 V dc , $\overline{CS} = V_{IH}$, f = 5 MHz	1,2,3	All		1.6	mA
Input low level 3/	V_{IL}		1,2,3	All		0.8	V
Input high level 3/	V_{IH}		1,2,3	All	2.0		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA	1,2,3	All		0.45	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.5 mA	1,2,3	All	0.85 x V_{CC}		V
Dynamic characteristics							
Address capacitance 3/	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25° C	4	All		15	pF
Output enable 3/ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25° C	4	All		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Dynamic characterisitics - Continued							
Write enable capacitance 3/	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25° C	4	All		15	pF
Chip select capacitance 3/	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25° C	4	All		15	pF
Data I/O capacitance 3/	$C_{I/O}$	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25° C	4	All		15	pF
Functional testing							
Functional tests		See 4.3.1c	7, 8A,8B	All			
Read cycle AC timing characteristics							
Read cycle time 3/	t_{RC}	See figure 4	9,10,11	01 02 03 04 05 06	150 120 90 70 60 55		ns
Address access time	t_{ACC}	See figure 4	9,10,11	01 02 03 04 05 06		150 120 90 70 60 55	ns
Chip select access time	t_{CE}	See figure 4	9,10,11	01 02 03 04 05 06		150 120 90 70 60 55	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics - Continued							
Output enable to output valid	t_{OE}	See figure 4	9,10,11	01 02 03,04 05,06		55 50 35 30	ns
Output hold from address, $\overline{CS}$ or $\overline{OE}$ change, whichever is first 3/	t_{OH}	See figure 4	9,10,11	All	0		ns
Write/Erase/Program AC timing characteristics $\overline{WE}$ controlled							
Write cycle time 3/	t_{WC}	See figure 5	9,10,11	01 02 03 04 05 06	150 120 90 70 60 55		ns
Chip select setup time	t_{CS}	See figure 5	9,10,11	All	0		ns
Write enable pulse width	t_{WP}	See figure 5	9,10,11	01,02 03,04 05 06	50 45 40 35		ns
Address setup time	t_{AS}	See figure 5	9,10,11	All	0		ns
Data setup time	t_{DS}	See figure 5	9,10,11	01,02 03,04 05 06	50 45 40 30		ns
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		ns
Address hold time	t_{AH}	See figure 5	9,10,11	01,02 03,04 05 06	50 45 45 40		ns
Write enable pulse high 3/	t_{WPH}	See figure 5	9,10,11	All	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write/Erase/Program AC timing characteristics $\overline{CS}$ controlled.							
Write cycle time 3/	t_{WC}	See figure 6	9,10,11	01 02 03 04 05 06	150 120 90 70 60 55		ns
Write enable setup time	t_{WS}	See figure 6	9,10,11	All	0		ns
Chip select pulse width	t_{CP}	See figure 6	9,10,11	01,02 03,04 05 06	50 45 40 35		ns
Address setup time	t_{AS}	See figure 6	9,10,11	All	0		ns
Data hold time	t_{DH}	See figure 6	9,10,11	All	0		ns
Data setup time	t_{DS}	See figure 6	9,10,11	01,02 03,04 05 06	50 45 40 30		ns
Address hold time	t_{AH}	See figure 6	9,10,11	01,02 03,04 05 06	50 45 45 40		ns
Chip select pulse width high 3/	t_{CPH}	See figure 6	9,10,11	All	20		ns

1/ Unless otherwise specified, 4.5 V dc $\le V_{CC} \le$ 5.5 V dc and V_{SS} = 0 V.

2/ Unless otherwise specified, the DC test conditions are as follows:
Input pulse levels: $V_{IH} = V_{CC}$ - 0.3 V and V_{IL} = 0.3 V.
Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V.
Output load circuit as specified in figure 8.

3/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be tested to the limits specified in table I for all lots not specifically tested.

Case outline T.

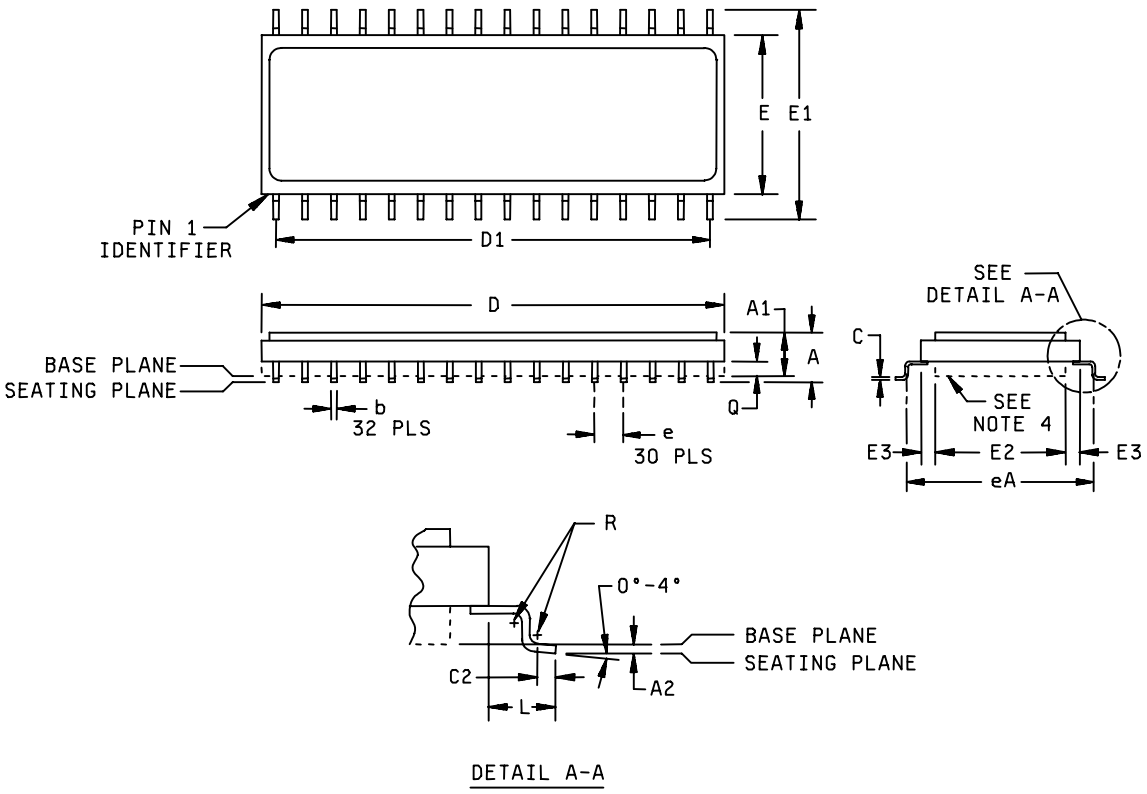


FIGURE 1. Case outlines.

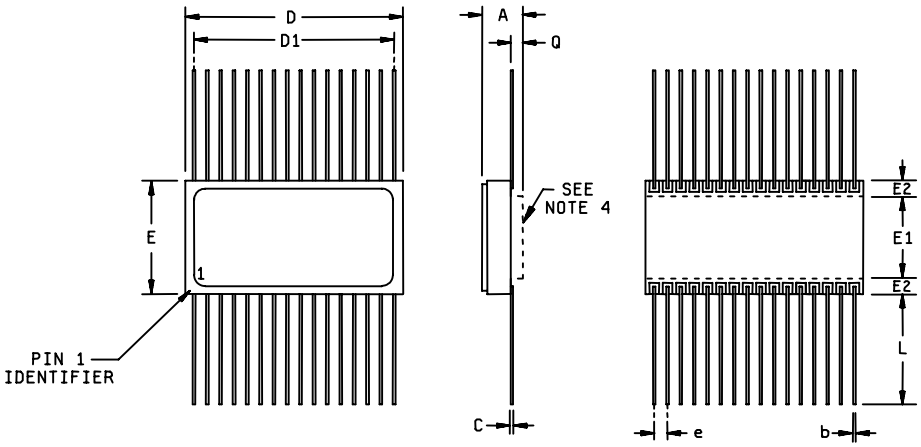
Case outline T - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.35		.132
A1	2.41	3.18	.095	.125
A2	0.08	0.18	.003	.007
b	0.38	0.48	.015	.019
C	0.10	0.18	.004	.007
C2	0.76 TYP		.030 TYP	
D	20.57	21.08	.810	.830
D1	19.05 TYP		.750 TYP	
E	10.29	10.54	.405	.415
E1	13.34	13.59	.525	.535
E2	7.75	8.00	.305	.315
E3	1.27 TYP		.050 TYP	
eA	11.07 TYP		.436 TYP	
e	1.27 TYP		.050 TYP	
L	1.52 TYP		.060 TYP	
Q	0.56	0.71	.022	.028
R	0.18 TYP		.007 TYP	

NOTES:
1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.
4. The case outline T is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline T.

FIGURE 1. Case outlines - Continued.

Case outline U.

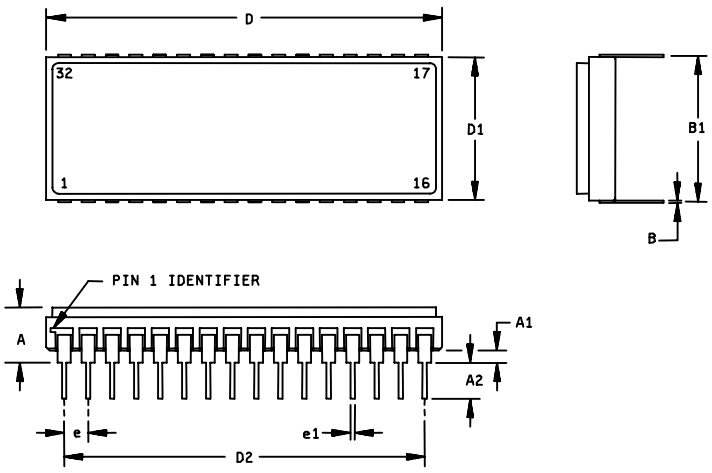


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.18		.125
b	0.38	0.48	.015	.019
C	0.10	0.18	.004	.007
D	20.57	21.08	.810	.830
D1	19.05 TYP		.750 TYP	
E	10.29	10.54	.405	.415
E1	7.75	8.00	.305	.315
E2	1.27 TYP		.050 TYP	
e	1.27 TYP		.050 TYP	
L	9.65	10.67	.380	.420
Q	0.56	0.71	.022	.028

NOTES:
1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions b and C will increase by +.003 inches (+0.08 mm).
3. Pin numbers are for reference only.
4. The case outline U is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline U.

FIGURE 1. Case outlines - Continued.

Case outline X.

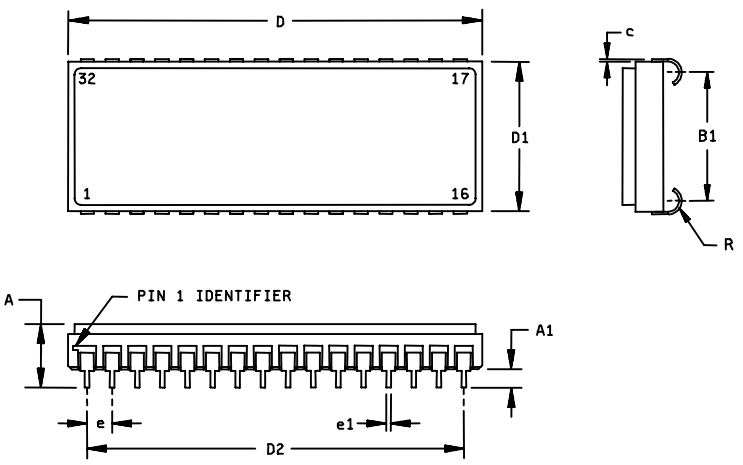


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.56	5.08	.140	.200
A1	0.48	1.19	.019	.047
A2	3.18	4.90	.125	.193
B	0.20	0.30	.009	.012
B1	14.94	15.67	.588	.617
D	40.64	42.82	1.6	1.686
D1	14.73	15.37	.580	.605
D2	37.90	38.30	1.492	1.508
e	2.54 BSC		.100 BSC	
e1	0.41	0.51	.016	.020

NOTES:
1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions B and e1 will increase by +.003 inches (+0.08mm).
3. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Case outline Y.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.67	4.06	.105	.160
A1	1.02	1.52	.040	.060
B1	9.30	9.80	.366	.386
c	0.15	0.25	.006	.010
D	20.83	21.35	.820	.840
D1	10.80	11.05	.425	.435
D2	18.85	19.25	.742	.758
e	1.27 BSC		.050 BSC	
e1	0.38	0.48	.015	.019
R	8.89 BSC		.350 BSC	

NOTES:
1. The U.S preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines- Continued.

Device types	All	Device types	All
Case outlines	All	Case outlines	All
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A18	17	I/O3
2	A16	18	I/O4
3	A15	19	I/O5
4	A12	20	I/O6
5	A7	21	I/O7
6	A6	22	$\overline{CS}$
7	A5	23	A10
8	A4	24	$\overline{OE}$
9	A3	25	A11
10	A2	26	A9
11	A1	27	A8
12	A0	28	A13
13	I/O0	29	A14
14	I/O1	30	A17
15	I/O2	31	$\overline{WE}$
16	Ground	32	V_{CC}

FIGURE 2. Terminal connections.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	MODE
V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Read
V_{IL}	V_{IH}	V_{IL}	D_{IN}	Write
V_{IH}	X	X	High Z	Standby
V_{IL}	V_{IH}	V_{IH}	High Z	Output disable

NOTES:

1. $H = V_{IH}$ = High Logic Level
2. $L = V_{IL}$ = Low Logic Level
3. X = Do not care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth table.

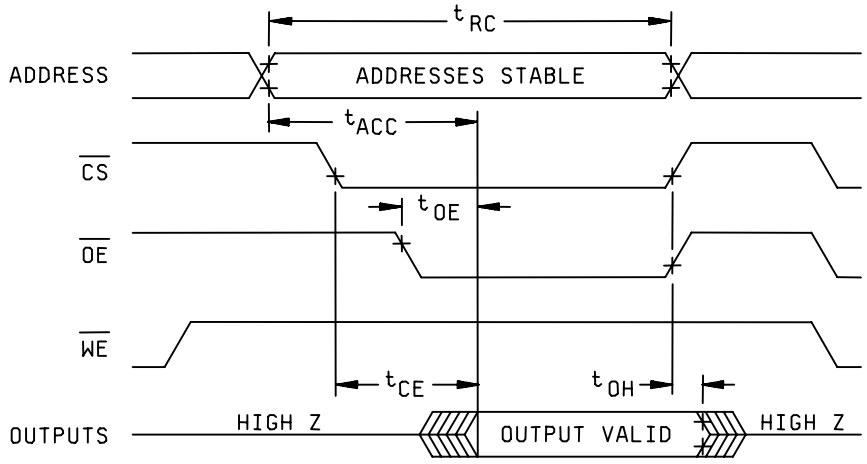


FIGURE 4. Read cycle timing diagram.

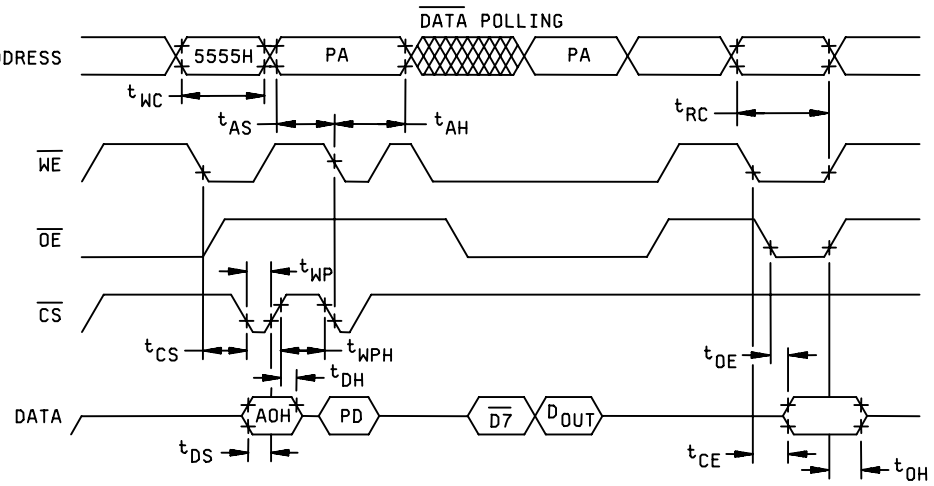


FIGURE 5. Write/Erase/Program operations, $\overline{WE}$ controlled.

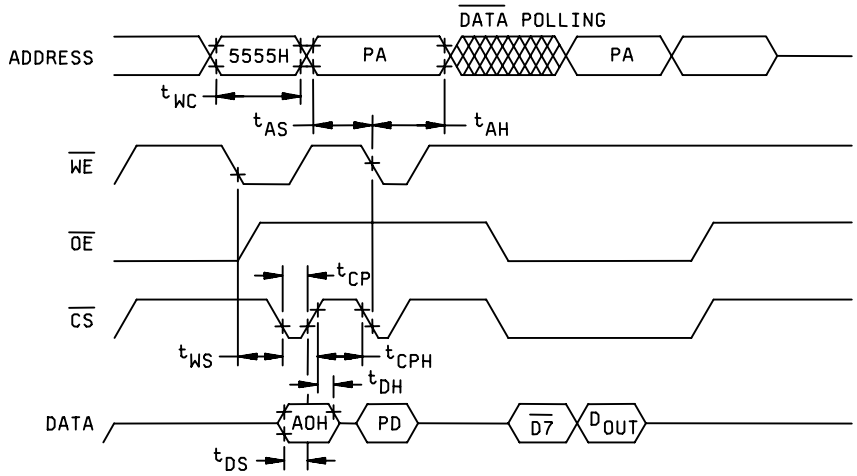


FIGURE 6. Write/Erase/Program operations, $\overline{CS}$ controlled.

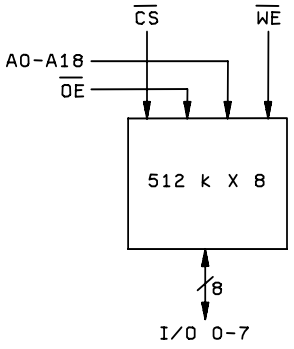
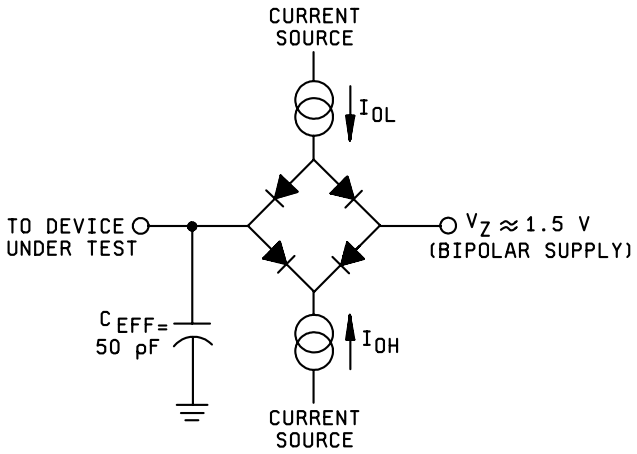


FIGURE 7. Block diagram .



Parameter	Typ.	Unit
Input pulse level	0 - 3.0	V
Input rise and fall	5	ns
Input and output reference level	1.5	V
Output load capacitance	50	pF

NOTES:
1. V_Z is programmable from -2 V to +7 V.
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is Z_O = 75 ohms.
4. V_Z is typically the midpoint of V_{OL} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 8. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7, 8A, and 8B shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) The checkerboard data pattern shall be verified after burn-in as part of end-point electrical testing.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-02-18

Approved sources of supply for SMD 5962-96692 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9669201HTA	0EU86	AS29F040DCG-150/Q
5962-9669201HTA	54230	WMF512K8-150FFQ5
5962-9669201HTA	88379	ACT-F512K8N-150F7Q
5962-9669201HTC	0EU86	AS29F040DCG-150/Q
5962-9669201HTC	54230	WMF512K8-150FFQ5
5962-9669201HTC	88379	ACT-F512K8N-150F7Q
5962-9669201HUA	0EU86	AS29F040F-150/Q
5962-9669201HUA	54230	WMF512K8-150FEQ5
5962-9669201HUA	88379	ACT-F512K8N-150F6Q
5962-9669201HUC	0EU86	AS29F040F-150/Q
5962-9669201HUC	54230	WMF512K8-150FEQ5
5962-9669201HUC	88379	ACT-F512K8N-150F6Q
5962-9669201HXA	0EU86	AS29F040CW-150/Q
5962-9669201HXA	54230	WMF512K8-150CQ5
5962-9669201HXA	88379	ACT-F512K8N-150P4Q
5962-9669201HXC	0EU86	AS29F040CW-150/Q
5962-9669201HXC	54230	WMF512K8-150CQ5
5962-9669201HXC	88379	ACT-F512K8N-150P4Q
5962-9669201HYA	54230	WMF512K8-150DEQ5
5962-9669201HYC	54230	WMF512K8-150DEQ5
5962-9669201HZA	0EU86	AS29F040ECA-150/Q
5962-9669201HZC	0EU86	AS29F040ECA-150/Q
5962-9669202HTA	0EU86	AS29F040DCG-120/Q
5962-9669202HTA	54230	WMF512K8-120FFQ5
5962-9669202HTA	88379	ACT-F512K8N-120F7Q
5962-9669202HTC	0EU86	AS29F040DCG-120/Q
5962-9669202HTC	54230	WMF512K8-120FFQ5
5962-9669202HTC	88379	ACT-F512K8N-120F7Q
5962-9669202HUA	0EU86	AS29F040F-120/Q
5962-9669202HUA	54230	WMF512K8-120FEQ5
5962-9669202HUA	88379	ACT-F512K8N-120F6Q
5962-9669202HUC	0EU86	AS29F040F-120/Q
5962-9669202HUC	54230	WMF512K8-120FEQ5
5962-9669202HUC	88379	ACT-F512K8N-120F6Q
5962-9669202HXA	0EU86	AS29F040CW-120/Q
5962-9669202HXA	54230	WMF512K8-120CQ5
5962-9669202HXA	88379	ACT-F512K8N-120P4Q
5962-9669202HXC	0EU86	AS29F040CW-120/Q
5962-9669202HXC	54230	WMF512K8-120CQ5
5962-9669202HXC	88379	ACT-F512K8N-120P4Q
5962-9669202HYA	54230	WMF512K8-120DEQ5
5962-9669202HYC	54230	WMF512K8-120DEQ5
5962-9669202HZA	0EU86	AS29F040ECA-120/Q
5962-9669202HZC	0EU86	AS29F040ECA-120/Q

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9669203HTA	0EU86	AS29F040DCG-90/Q
5962-9669203HTA	54230	WMF512K8-90FFQ5
5962-9669203HTA	88379	ACT-F512K8N-090F7Q
5962-9669203HTC	0EU86	AS29F040DCG-90/Q
5962-9669203HTC	54230	WMF512K8-90FFQ5
5962-9669203HTC	88379	ACT-F512K8N-090F7Q
5962-9669203HUA	0EU86	AS29F040F-90/Q
5962-9669203HUA	54230	WMF512K8-90FEQ5
5962-9669203HUA	88379	ACT-F512K8N-090F6Q
5962-9669203HUC	0EU86	AS29F040F-90/Q
5962-9669203HUC	54230	WMF512K8-90FEQ5
5962-9669203HUC	88379	ACT-F512K8N-090F6Q
5962-9669203HXA	0EU86	AS29F040CW-90/Q
5962-9669203HXA	54230	WMF512K8-90CQ5
5962-9669203HXA	88379	ACT-F512K8N-090P4Q
5962-9669203HXC	0EU86	AS29F040CW-90/Q
5962-9669203HXC	54230	WMF512K8-90CQ5
5962-9669203HXC	88379	ACT-F512K8N-090P4Q
5962-9669203HYA	54230	WMF512K8-90DEQ5
5962-9669203HYC	54230	WMF512K8-90DEQ5
5962-9669203HZA	0EU86	AS29F040ECA-90/Q
5962-9669203HZC	0EU86	AS29F040ECA-90/Q
5962-9669204HTA	0EU86	AS29F040DCG-70/Q
5962-9669204HTA	54230	WMF512K8-70FFQ5
5962-9669204HTA	88379	ACT-F512K8N-070F7Q
5962-9669204HTC	0EU86	AS29F040DCG-70/Q
5962-9669204HTC	54230	WMF512K8-70FFQ5
5962-9669204HTC	88379	ACT-F512K8N-070F7Q
5962-9669204HUA	0EU86	AS29F040F-70/Q
5962-9669204HUA	54230	WMF512K8-70FEQ5
5962-9669204HUA	88379	ACT-F512K8N-070F6Q
5962-9669204HUC	0EU86	AS29F040F-70/Q
5962-9669204HUC	54230	WMF512K8-70FEQ5
5962-9669204HUC	88379	ACT-F512K8N-070F6Q
5962-9669204HXA	0EU86	AS29F040CW-70/Q
5962-9669204HXA	54230	WMF512K8-70CQ5
5962-9669204HXA	88379	ACT-F512K8N-070P4Q
5962-9669204HXC	0EU86	AS29F040CW-70/Q
5962-9669204HXC	54230	WMF512K8-70CQ5
5962-9669204HXC	88379	ACT-F512K8N-070P4Q
5962-9669204HYA	54230	WMF512K8-70DEQ5
5962-9669204HYC	54230	WMF512K8-70DEQ5
5962-9669204HZA	0EU86	AS29F040ECA-70/Q
5962-9669204HZC	0EU86	AS29F040ECA-70/Q

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9669205HTA	0EU86	AS29F040DCG-60/Q
5962-9669205HTA	54230	WMF512K8-60FFQ5
5962-9669205HTC	0EU86	AS29F040DCG-60/Q
5962-9669205HTC	54230	WMF512K8-60FFQ5
5962-9669205HUA	0EU86	AS29F040F-60/Q
5962-9669205HUA	54230	WMF512K8-60FEQ5
5962-9669205HUC	0EU86	AS29F040F-60/Q
5962-9669205HUC	54230	WMF512K8-60FEQ5
5962-9669205HXA	0EU86	AS29F040CW-60/Q
5962-9669205HXA	54230	WMF512K8-60CQ5
5962-9669205HXA	88379	ACT-F512K8N-060P4Q
5962-9669205HXC	0EU86	AS29F040CW-60/Q
5962-9669205HXC	54230	WMF512K8-60CQ5
5962-9669205HXC	88379	ACT-F512K8N-060P4Q
5962-9669205HYA	54230	WMF512K8-60DEQ5
5962-9669205HYC	54230	WMF512K8-60DEQ5
5962-9669205HZA	0EU86	AS29F040ECA-60/Q
5962-9669205HZC	0EU86	AS29F040ECA-60/Q
5962-9669206HTA	0EU86	AS29F040DCG-55/Q
5962-9669206HTC	0EU86	AS29F040DCG-55/Q
5962-9669206HUA	0EU86	AS29F040F-55/Q
5962-9669206HUC	0EU86	AS29F040F-55/Q
5962-9669206HXA	0EU86	AS29F040CW-55/Q
5962-9669206HXC	0EU86	AS29F040CW-55/Q
5962-9669206HZA	0EU86	AS29F040ECA-55/Q
5962-9669206HZC	0EU86	AS29F040ECA-55/Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor for its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor, Incorporated 8701 Cross Park Drive Austin, TX 78754-4566
54230	White Electronic Designs Corporation 3601 East University Drive Phoenix, AZ 85034-7217
88379	Aeroflex Circuit Technology 35 South Service Road Plainview NY, 11803-4193