HARRIS SEMICONDUCTOR

HS-5104ARH

Radiation Hardened Low Noise Quad Operational Amplifier

October 1997

Features

- QML Qualified Per MIL-PRF-38535 Requirements
- Radiation Environment
  - Gamma Dose (γ) . . . . . 1×10^5 RAD(Si)
- Low Noise
  - At 1kHz . . . . . $4.3nV/\sqrt{Hz}$ (Typ)
  - At 1kHz . . . . . $0.6pA/\sqrt{Hz}$ (Typ)
- Low Offset Voltage. . . . . 3.0mV (Max)
- High Slew Rate . . . . . 2.0V/μs (Typ)
- Gain Bandwidth Product . . . . . 8.0MHz (Typ)

Applications

- High Q, Active Filters
- Voltage Regulators
- Integrators
- Signal Generators
- Voltage References
- Space Environments

Description

The HS-5104ARH is a radiation hardened, monolithic quad operational amplifier that provides highly reliable performance in harsh radiation environments. Its excellent noise characteristics coupled with an unique array of dynamic specifications make this amplifier well-suited for a variety of satellite system applications. Dielectrically isolated, bipolar processing makes this device immune to Single Event Latch-up.

The HS-5104ARH shows almost no change in offset voltage after exposure to 100K RAD(Si) gamma radiation, with only a minor increase in current. Complementing these specifications is a post radiation open loop gain in excess of 40K.

This quad operational amplifier is available in an industry standard pinout, allowing for immediate interchangeability with most other quad operational amplifiers.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). SMD numbers must be used when ordering.

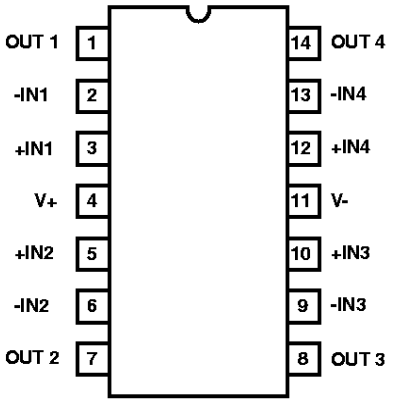
Detailed Electrical Specifications for this are contained in SMD 5962-95690. A "hot-link" is provided on our homepage with instructions for downloading. http://www.semi.harris.com/data/sm/index.htm

Ordering Information

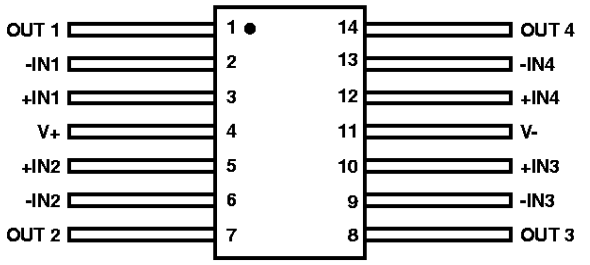
SMD PART NUMBER	HARRIS PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	CASE OUTLINE
5962R9569001VCC	HS1-5104ARH-Q	-55 to 125	14 Ld SBDIP	CDIP2-T14
N/A	HS1-5104ARH/Proto	-55 to 125	14 Ld SBDIP	CDIP2-T14
N/A	HS1-5104ARH/Sample	25	14 Ld SBDIP	CDIP2-T14
5962R9569001VXC	HS9-5104ARH-Q	-55 to 125	14 Ld Flatpack	CDFP3-F14
N/A	HS9-5104ARH/Proto	-55 to 125	14 Ld Flatpack	CDFP3-F14
N/A	HS9-5104ARH/Sample	25	14 Ld Flatpack	CDFP3-F14

Pinouts

HS-5104ARH (SBDIP)
TOP VIEW



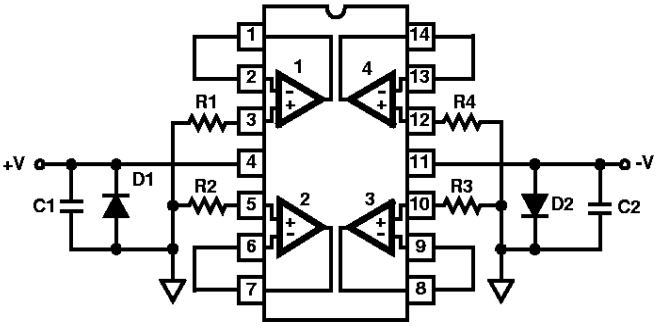
HS-5104ARH (FLATPACK)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

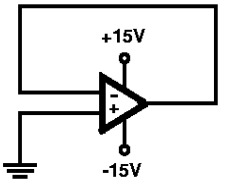
File Number **3025.2**

Burn-In Circuit



NOTES:
R1 = R2 = R3 = R4 = 1MΩ, 5%, 1/4W (Min)
C1 = C2 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
D1 = D2 = IN4002 or Equivalent/Board
|(V+) - (V-)| = 31V ±1V

Irradiation Circuit



(ONE OF FOUR)

NOTES:
+V = 15V
-V = -15V
Group E Sample Size = 4 Die Per Wafer

Metallization Mask Layout

DIE DIMENSIONS:
95 mils x 99 mils x 19 mils ±1 mils
(2420µm x 2530µm x 483µm ±25.4µm)

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up): Unbiased

BACKSIDE FINISH: Silicon

PASSIVATION:
Type: Nitride (SI3N4) over Silox (SIO2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5$ A/cm^2

TRANSISTOR COUNT: 175

PROCESS: Bipolar Dielectric Isolation