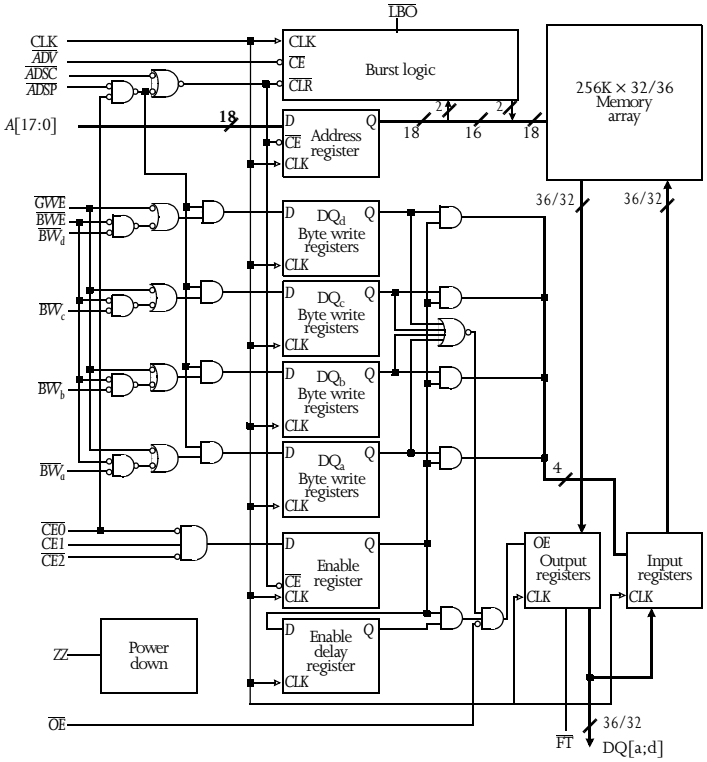
3.3V 256K × 32/36 pipeline burst synchronous SRAM

Features

- Organization: 262,144 words × 32 or 36 bits
- Fast clock speeds to 166 MHz in LVTTL/LVCMOS
- Fast clock to data access: 3.5/3.8/4.0/5.0 ns
- Fast $\overline{OE}$ access time: 3.5/3.8/4.0/5.0 ns
- Fully synchronous register-to-register operation
- Single register "Flow-through" option
- Dual-cycle deselect
  - Single-cycle deselect also available (AS7C33256PFS32A/ AS7C33256PFS36A)
- Available in both 2 chip enable and 3 chip enable
  - 2 CE part number is AS7C33256PFD32A2 or AS7C33256PFD36A2
- Pentium®[1] compatible architecture and timing
- Asynchronous output enable control
- Available in 100-pin TQFP and 119-pin BGA packages
- Byte write enables
- 3.3V core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- 30 mW typical standby power in power down mode
- NTD™[1] pipeline architecture available (AS7C33256NTD32A/ AS7C33256NTD36A)

1 *Pentium® is a registered trademark of Intel Corporation. NTD™ is a trademark of Alliance Semiconductor Corporation. All trademarks mentioned in this document are the property of their respective owners

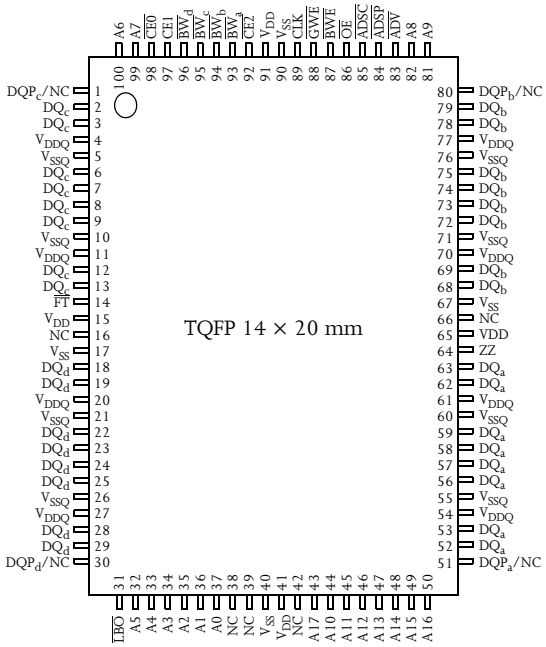
Logic block diagram



Selection guide

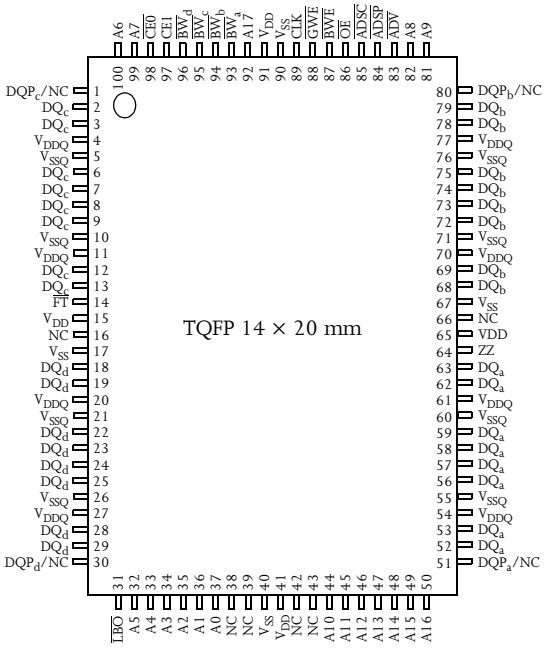
	−166	−150	−133	−100	Units
Minimum cycle time	6	6.6	7.5	10	ns
Maximum pipelined clock frequency	166	150	133	100	MHz
Maximum pipelined clock access time	3.5	3.8	4	5	ns
Maximum operating current	475	450	425	325	mA
Maximum standby current	130	110	100	90	mA
Maximum CMOS standby current (DC)	30	30	30	30	mA

Pin Arrangment for TQFP 3 Chip Enable



Note: Pins 1, 30, 51, 80 are NC for ×32

Pin Arrangment for TQFP 2 Chip Enable



Note: Pins 1, 30, 51, 80 are NC for ×32

Ball assignment for 119-ball BGA[1]

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE1	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_C	DQPc	V_{SS}	NC	V_{SS}	DQpb	DQb
E	DQ_C	DQc	V_{SS}	$\overline{CE0}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQ_C	DQc	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb	DQb
H	DQ_C	DQc	V_{SS}	$\overline{GWE}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{BWE}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1[2]	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A0[2]	V_{SS}	DQPa	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

1 Note 2D, 2P, 6D and 6P are NC for x32
2 A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

Functional description

The AS7C33256PFD32A and 7C33256PFD36A are high-performance CMOS 8-Mbit synchronous Static Random Access Memory (SRAM) devices organized as 262,144 words × 32 or 36 bits, and incorporate a two-stage register-register pipeline for highest frequency on any given technology.

Timing for these devices is compatible with existing Pentium® synchronous cache specifications. This architecture is suited for ASIC, DSP (TMS320C6X), and PowerPC™[1]-based systems in computing, datacomm, instrumentation, and telecommunications systems.

Fast cycle times of 6/6.6/7.5/10 ns with clock access times (t_{CD}) of 3.5/3.8/4.0/5.0 ns enable 166, 150, 133 and 100 MHz bus frequencies. Two-chip enable and three-chip enable ($\overline{CE}$) inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ($\overline{ADSC}$), or the processor address strobe ($\overline{ADSP}$). The burst advance pin ($\overline{ADV}$) allows subsequent internally generated burst addresses.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register when $\overline{ADSP}$ is sampled Low, the chip enables are sampled active, and the output buffer is enabled with $\overline{OE}$. In a read operation the data accessed by the current address, registered in the address registers by the positive edge of CLK, are carried to the data-out registers and driven on the output pins on the next positive edge of CLK. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when $\overline{ADV}$ is sampled Low, and both address strobes are High. Burst mode is selectable with the $\overline{LBO}$ input. With $\overline{LBO}$ unconnected or driven High, burst operations use a Pentium® count sequence. With $\overline{LBO}$ driven LOW, the device uses a linear count sequence suitable for PowerPC™ and many other applications.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting a write command. A global write enable $\overline{GWE}$ writes all 32/36 bits regardless of the state of individual $\overline{BW[a:d]}$ inputs. Alternately, when $\overline{GWE}$ is High, one or more bytes may be written by asserting $\overline{BWE}$ and the appropriate individual byte $\overline{BWn}$ signal(s).

$\overline{BWn}$ is ignored on the clock edge that samples $\overline{ADSP}$ Low, but is sampled on all subsequent clock edges. Output buffers are disabled when $\overline{BWn}$ is sampled LOW (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{BWn}$ is sampled Low. Address is incremented internally to the next burst address if $\overline{BWn}$ and $\overline{ADV}$ are sampled Low.

Read or write cycles may also be initiated with $\overline{ADSC}$ instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ follow.

- $\overline{ADSP}$ must be sampled HIGH when $\overline{ADSC}$ is sampled LOW to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$ signals are sampled on the clock edge that samples $\overline{ADSC}$ LOW (and $\overline{ADSP}$ High).
- Master chip enable $\overline{CE0}$ blocks $\overline{ADSP}$, but not $\overline{ADSC}$.

AS7C33256PFD32A and AS7C33256PFD36A family operates from a core 3.3V power supply. I/Os use a separate power supply that can operate at 2.5V or 3.3V. These devices are available in 100-pin 14 × 20 mm TQFP package and 119-pin 14 x 20 mm BGA package.

Capacitance

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	Address and control pins	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	V_{IN} = V_{OUT} = 0V	7	pF

Write enable truth table (per byte)

$\overline{GWE}$	$\overline{BWE}$	$\overline{BWn}$	$\overline{WEn}$
L	X	X	T
H	L	L	T
H	H	X	F*
H	L	H	F*

Key: X = Don't Care, L = Low, H = High, T = True, F = False; *= Valid read; n = a, b, c, d; $\overline{WE}$, $\overline{WEn}$ = internal write signal.

Burst order table

	Interleaved Burst Order $\overline{LBO}$=1					Linear Burst Order $\overline{LBO}$=0			
Starting Address	00	01	10	11	Starting Address	00	01	10	11
First increment	01	00	11	10	First increment	01	10	11	00
Second increment	10	11	00	01	Second increment	10	11	00	01
Third increment	11	10	01	00	Third increment	11	00	01	10

1 PowerPC™ is a trademark International Business Machines Corporation.

Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$, $\overline{FT}$, ZZ, $\overline{LBO}$ are synchronous to this clock.
A0–A17	I	SYNC	Address. Sampled when all chip enables are active and $\overline{ADSC}$ or $\overline{ADSP}$ are asserted.
DQ[a,b,c,d]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$	I	SYNC	Master chip enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE0}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the Synchronous Truth Table for more information.
CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Active HIGH and active Low, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE0}$ and $\overline{ADSP}$ are active.
$\overline{ADSP}$	I	SYNC	Address strobe processor. Asserted LOW to load a new bus address or to enter standby mode.
$\overline{ADSC}$	I	SYNC	Address strobe controller. Asserted LOW to load a new address or to enter standby mode.
$\overline{ADV}$	I	SYNC	Advance. Asserted LOW to continue burst read/write.
$\overline{GWE}$	I	SYNC	Global write enable. Asserted LOW to write all 32/36 bits. When High, $\overline{BWE}$ and $\overline{BW[a:d]}$ control write enable.
$\overline{BWE}$	I	SYNC	Byte write enable. Asserted LOW with $\overline{GWE}$ = HIGH to enable effect of $\overline{BW[a:d]}$ inputs.
$\overline{BW[a,b,c,d]}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE}$ = HIGH and $\overline{BWE}$ = Low. If any of $\overline{BW[a:d]}$ is active with $\overline{GWE}$ = HIGH and $\overline{BWE}$ = LOW the cycle is a write cycle. If all $\overline{BW[a:d]}$ are inactive the cycle is a read cycle.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is in read mode.
$\overline{LBO}$	I	STATIC	Count mode. When driven High, count sequence follows Intel XOR convention. When driven Low, count sequence follows linear convention. This signal is internally pulled High.
$\overline{FT}$	I	STATIC	Flow-through mode.When low, enables single register flow-through mode. Connect to V_{DD} if unused or for pipelined operation.
ZZ	I	ASYNC	Snooze. Places device in low power mode; data is retained. Connect to GND if unused.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	−0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	−0.5	V_{DD} + 0.5	V
Input voltage relative to GND (I/O pins)	V_{IN}	−0.5	V_{DDQ} + 0.5	V
Power dissipation	P_D	–	1.8	W
DC output current	I_{OUT}	–	50	mA
Storage temperature (plastic)	T_{stg}	−65	+150	°C
Temperature under bias	T_{bias}	−65	+135	°C

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Synchronous truth table

$\overline{CE0}$	CE1	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WEn}$[1]	$\overline{OE}$	Address accessed	CLK	Operation	DQ
H	X	X	X	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	L	X	L	X	X	X	X	NA	L to H	Deselect	Hi–Z
L	L	X	H	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	X	H	L	X	X	X	X	NA	L to H	Deselect	Hi–Z
L	X	H	H	L	X	X	X	NA	L to H	Deselect	Hi–Z
L	H	L	L	X	X	X	L	External	L to H	Begin read	Hi–Z[2]
L	H	L	L	X	X	X	H	External	L to H	Begin read	Hi–Z
L	H	L	H	L	X	F	L	External	L to H	Begin read	Hi–Z[2]
L	H	L	H	L	X	F	H	External	L to H	Begin read	Hi–Z
X	X	X	H	H	L	F	L	Next	L to H	Cont. read	Q
X	X	X	H	H	L	F	H	Next	L to H	Cont. read	Hi–Z
X	X	X	H	H	H	F	L	Current	L to H	Suspend read	Q
X	X	X	H	H	H	F	H	Current	L to H	Suspend read	Hi–Z
H	X	X	X	H	L	F	L	Next	L to H	Cont. read	Q
H	X	X	X	H	L	F	H	Next	L to H	Cont. read	Hi–Z
H	X	X	X	H	H	F	L	Current	L to H	Suspend read	Q
H	X	X	X	H	H	F	H	Current	L to H	Suspend read	Hi–Z
L	H	L	H	L	X	T	X	External	L to H	Begin write	D[3]
X	X	X	H	H	L	T	X	Next	L to H	Cont. write	D
H	X	X	X	H	L	T	X	Next	L to H	Cont. write	D
X	X	X	H	H	H	T	X	Current	L to H	Suspend write	D
H	X	X	X	H	H	T	X	Current	L to H	Suspend write	D

1 See "Write enable truth table"on page 4 for more information.
2 Q in "flow through" mode
3 For WRITE operation following a READ, $\overline{OE}$ must be HIGH before the input data set up time and held HIGH throughout the input hold time.

Key: X = Don't Care, L = Low, H = High.

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{DD}	3.135	3.3	3.465	V
		V_{SS}	0.0	0.0	0.0	
3.3V I/O supply voltage		V_{DDQ}	3.135	3.3	3.465	V
		V_{SSQ}	0.0	0.0	0.0	
2.5V I/O supply voltage		V_{DDQ}	2.35	2.5	2.9	V
		V_{SSQ}	0.0	0.0	0.0	
Input voltages[1]	Address and control pins	V_{IH}	2.0	–	V_{DD} + 0.3	V
		V_{IL}	–0.5[2]	–	0.8	
	I/O pins	V_{IH}	2.0	–	V_{DDQ} + 0.3	V
		V_{IL}	–0.5[2]	–	0.8	
Ambient operating temperature		T_A	0	–	70	°C

1 Input voltage ranges apply to 3.3V I/O operation. For 2.5V I/O operation, contact factory for input specifications.
2 V_{IL} min = –2.0V for pulse width less than 0.2 × t_{RC}.

TQFP thermal resistance

Description	Conditions		Symbol	Typical
Thermal resistance (junction to ambient)[1]	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	1–layer	θ_{JA}	40
		4–layer	θ_{JA}	22
Thermal resistance (junction to top of case)[1]			θ_{JC}	8

1 This parameter is sampled.

DC electrical characteristics

Parameter	Symbol	Test conditions	–166		–150		–133		–100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current[1]	$\lvert I_{LI} \rvert$	V_{DD} = Max, V_{IN} = GND to V_{DD}	–	2	–	2	–	2	–	2	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{OE} \geq V_{IH}$, V_{DD} = Max, V_{OUT} = GND to V_{DD}	–	2	–	2	–	2	–	2	µA
Operating power supply current	I_{CC}[2] (Pipelined)	$\overline{CE0} = V_{IL}$, CE1 = V_{IH}, $\overline{CE2} = V_{IL}$, f = f_{Max}, I_{OUT} = 0 mA	–	475	–	450	–	425	–	325	mA
Operating power supply current	I_{CC}[2] (Flow-through)	$\overline{CE0} = V_{IL}$, CE1 = V_{IH}, $\overline{CE2} = V_{IL}$, f = f_{Max}, I_{OUT} = 0 mA	–	325	–	325	–	300	–	300	mA
Standby power supply current	I_{SB}	Deselected, f = f_{Max}, ZZ ≤ V_{IL}	–	130	–	110	–	100	–	90	mA
	I_{SB1}	Deselected, f = 0, ZZ ≤ 0.2V all V_{IN} ≤ 0.2V or ≥ V_{DD} – 0.2V	–	30	–	30	–	30	–	30	
	I_{SB2}	Deselected, f = f_{Max}, ZZ ≥ V_{DD} – 0.2V All V_{IN} ≤ V_{IL} or ≥ V_{IH}	–	30	–	30	–	30	–	30	
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 3.465V	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.135V	2.4	–	2.4	–	2.4	–	2.4	–	

1 $\overline{LBO}$ pin has an internal pull-up and input leakage = ±10 µA.
2 I_{CC} given with no output loading. I_{CC} increases with faster cycles times and greater output loading.

DC electrical characteristics for 2.5V I/O operation

Parameter	Symbol	Test conditions	–166		–150		–133		–100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{OE} \geq V_{IH}$, V_{DD} = Max, V_{OUT} = GND to V_{DD}	–1	1	–1	1	–1	1	–1	1	µA
Output voltage	V_{OL}	I_{OL} = 2 mA, V_{DDQ} = 2.65V	–	0.7	–	0.7	–	0.7	–	0.7	V
	V_{OH}	I_{OH} = –2 mA, V_{DDQ} = 2.35V	1.7	–	1.7	–	1.7	–	1.7	–	

Timing characteristics over operating range

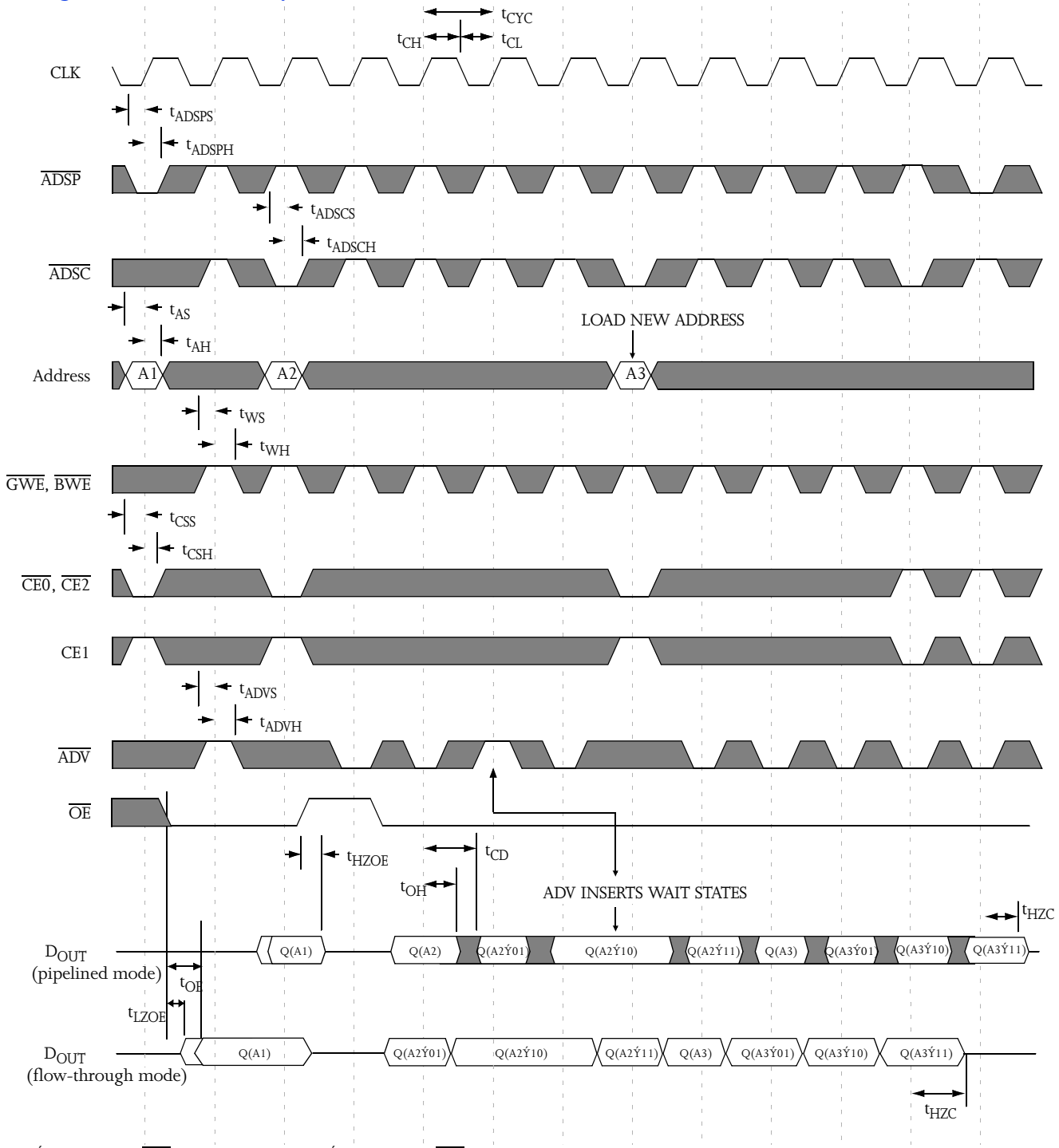
Parameter	Symbol	–166		–150		–133		–100		Unit	Notes[1]
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock frequency	f_{Max}	–	166	–	150	–	133	–	100	MHz	
Cycle time (pipelined mode)	t_{CYC}	6	–	6.6	–	7.5	–	10	–	ns	
Cycle time (flow-through mode)	t_{CYCF}	10	–	10	–	12	–	12	–	ns	
Clock access time (pipelined mode)- 3.3V VDDQ	t_{CD} 3.3V	-	3.5	-	3.8	-	4.0	-	5.0	ns	
Clock access time (pipelined mode)- 2.5V VDDQ	t_{CD} 2.5V	-	4.0	-	4.3	-	4.5	-	5.0	ns	
Clock access time (flow-through mode)	t_{CDF}	–	9	–	10	–	10	–	12	ns	
Output enable LOW to data valid	t_{OE}	–	3.5	–	3.8	–	4.0	–	5.0	ns	
Clock HIGH to output Low Z	t_{LZC}	0	–	0	–	0	–	0	–	ns	2,3,4
Data output invalid from clock HIGH	t_{OH}	1.5	–	1.5	–	1.5	–	1.5	–	ns	2
Output enable LOW to output Low Z	t_{LZOE}	0	–	0	–	0	–	0	–	ns	2,3,4
Output enable HIGH to output High Z	t_{HZOE}	–	3.5	–	3.8	–	4.0	–	4.5	ns	2,3,4
Clock HIGH to output High Z	t_{HZC}	–	3.5	–	3.8	–	4.0	–	5.0	ns	2,3,4
Output enable HIGH to invalid output	t_{OHOE}	0	–	0	–	0	–	0	–	ns	
Clock HIGH pulse width	t_{CH}	2.4	–	2.5	–	2.5	–	3.5	–	ns	5
Clock LOW pulse width	t_{CL}	2.4	–	2.5	–	2.5	–	3.5	–	ns	5
Address setup to clock HIGH	t_{AS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
Data setup to clock HIGH	t_{DS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
Write setup to clock HIGH	t_{WS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6,7
Chip select setup to clock HIGH	t_{CSS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6,8
Address hold from clock HIGH	t_{AH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6
Data hold from clock HIGH	t_{DH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6
Write hold from clock HIGH	t_{WH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6,7
Chip select hold from clock HIGH	t_{CSH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6,8
$\overline{ADV}$ setup to clock HIGH	t_{ADVS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
$\overline{ADSP}$ setup to clock HIGH	t_{ADSPS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
$\overline{ADSC}$ setup to clock HIGH	t_{ADSCS}	1.5	–	1.5	–	1.5	–	2.0	–	ns	6
$\overline{ADV}$ hold from clock HIGH	t_{ADVH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6
$\overline{ADSP}$ hold from clock HIGH	t_{ADSPH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6
$\overline{ADSC}$ hold from clock HIGH	t_{ADSCH}	0.5	–	0.5	–	0.5	–	0.5	–	ns	6

1 See “notes” on page 12

Key to switching waveforms

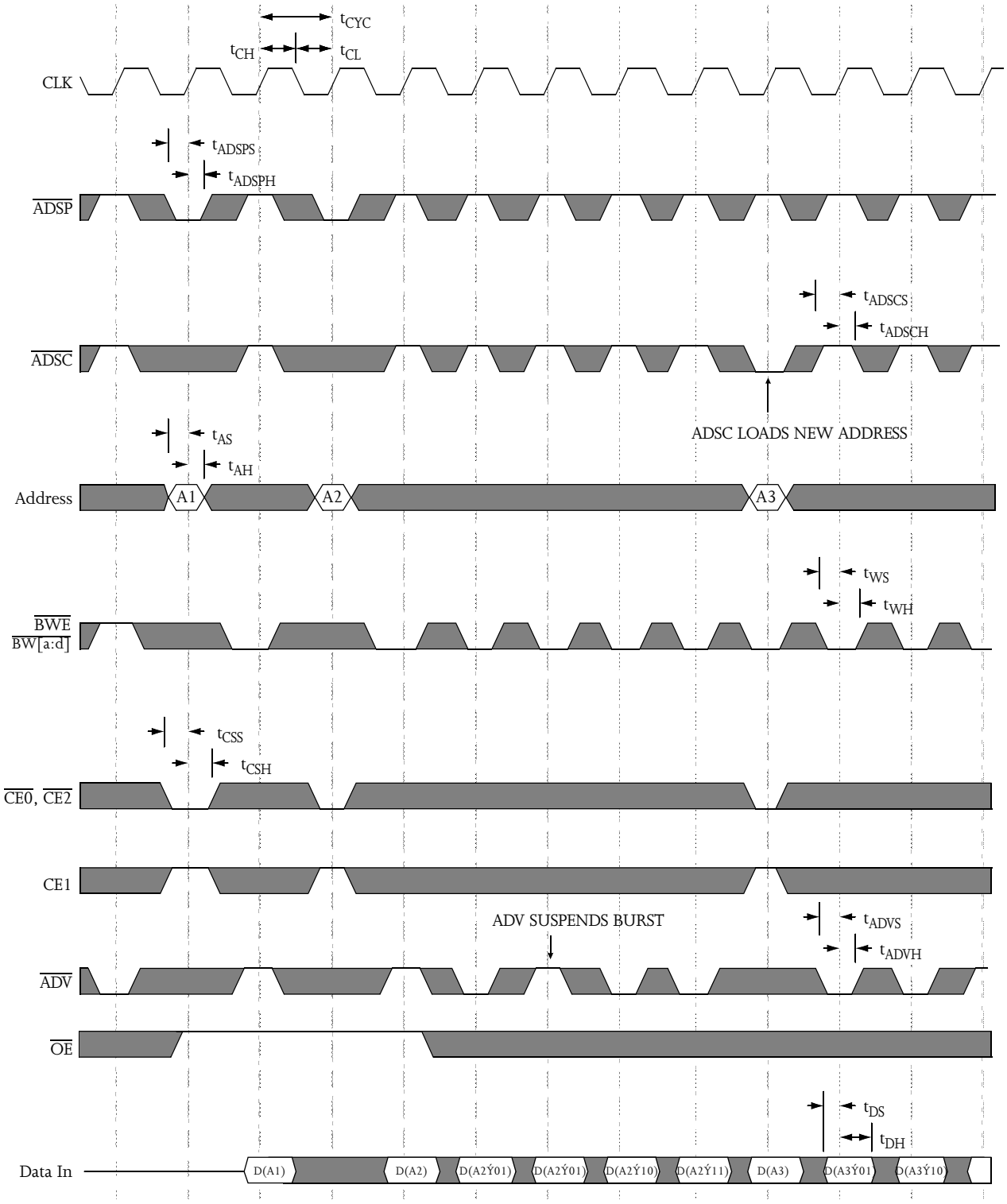
Rising input Falling input Undefined/don't care

Timing waveform of read cycle



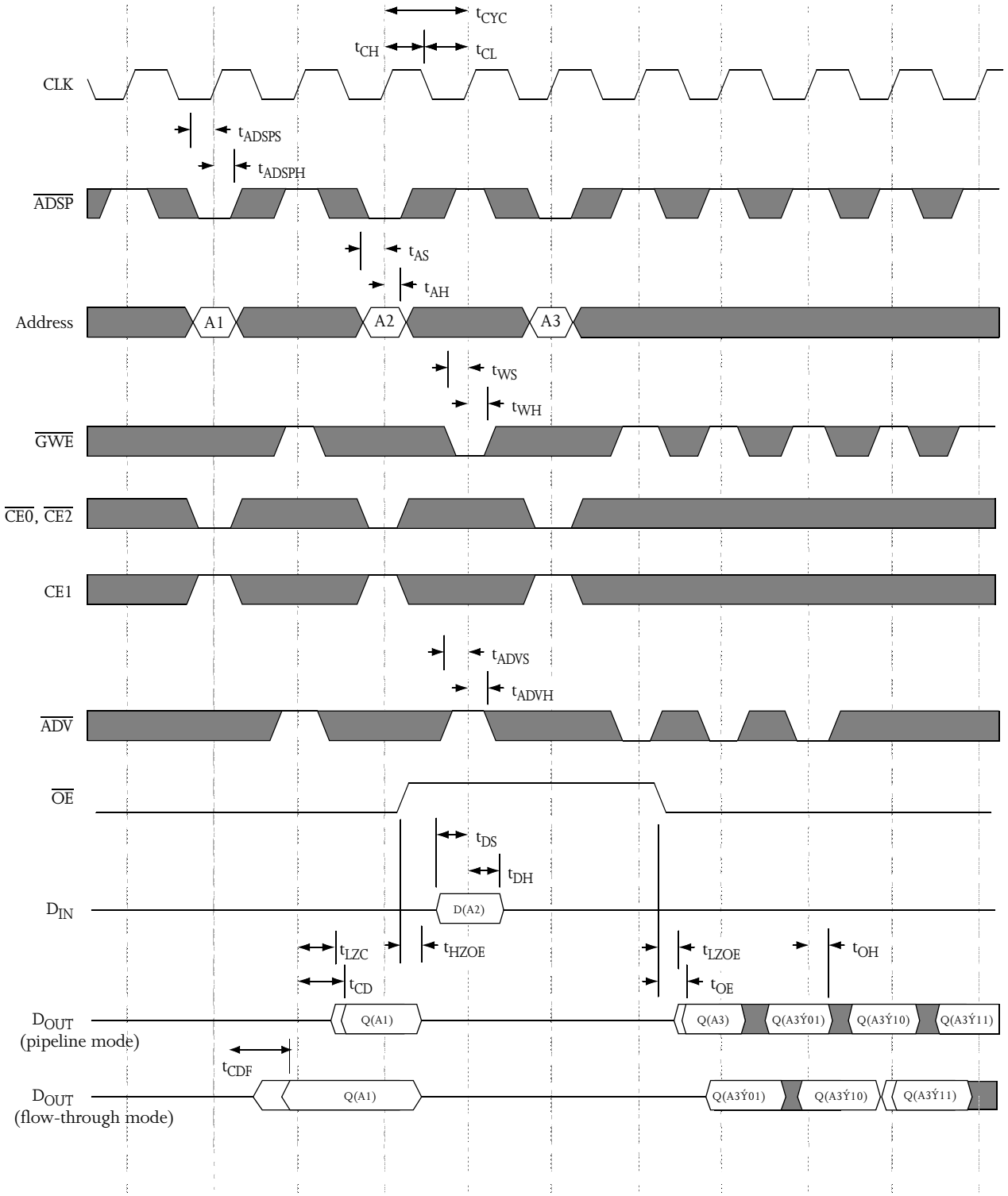
Note: Ý = XOR when $\overline{LBO}$ = HIGH/No Connect; Ý = ADD when $\overline{LBO}$ = LOW.
$\overline{BW[a:d]}$ is don't care.

Timing waveform of write cycle



Note: Ý = XOR when $\overline{LBO}$ = HIGH/No Connect; Ý = ADD when $\overline{LBO}$ = LOW.

Timing waveform of read/write cycle



Note: Ý = XOR when $\overline{LBO}$ = HIGH/No Connect; Ý = ADD when $\overline{LBO}$ = LOW.

AC test conditions

- Output load: see Figure B, except for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC}, see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

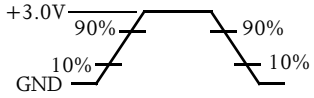


Figure A: Input waveform

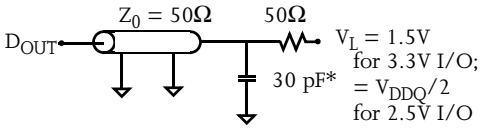


Figure B: Output load (A)

Thevenin equivalent:

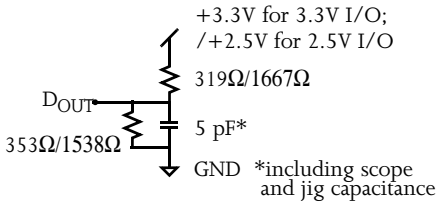


Figure C: Output load(B)

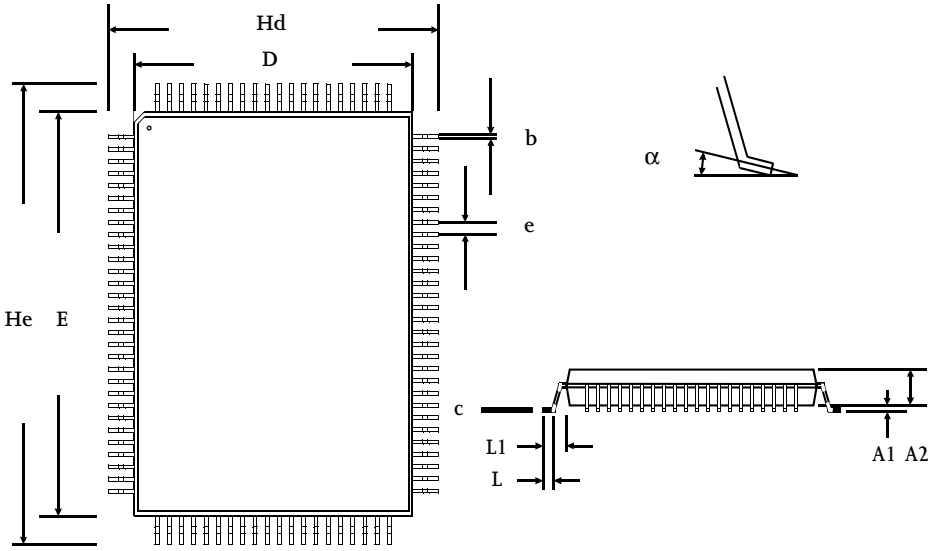
Notes

1 For test conditions, see *AC Test Conditions*, Figures A, B, C.
2 This parameter measured with output load condition in Figure C.
3 This parameter is sampled, but not 100% tested.
4 t_{HZOE} is less than t_{LZOE}; and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
5 tCH measured as HIGH above VIH and tCL measured as LOW below VIL.
6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.
7 Write refers to $\overline{\text{GWE}}$, $\overline{\text{BWE}}$, $\overline{\text{BW[a:d]}}$.
8 Chip select refers to $\overline{\text{CE0}}$, CE1, $\overline{\text{CE2}}$.

Package Dimensions

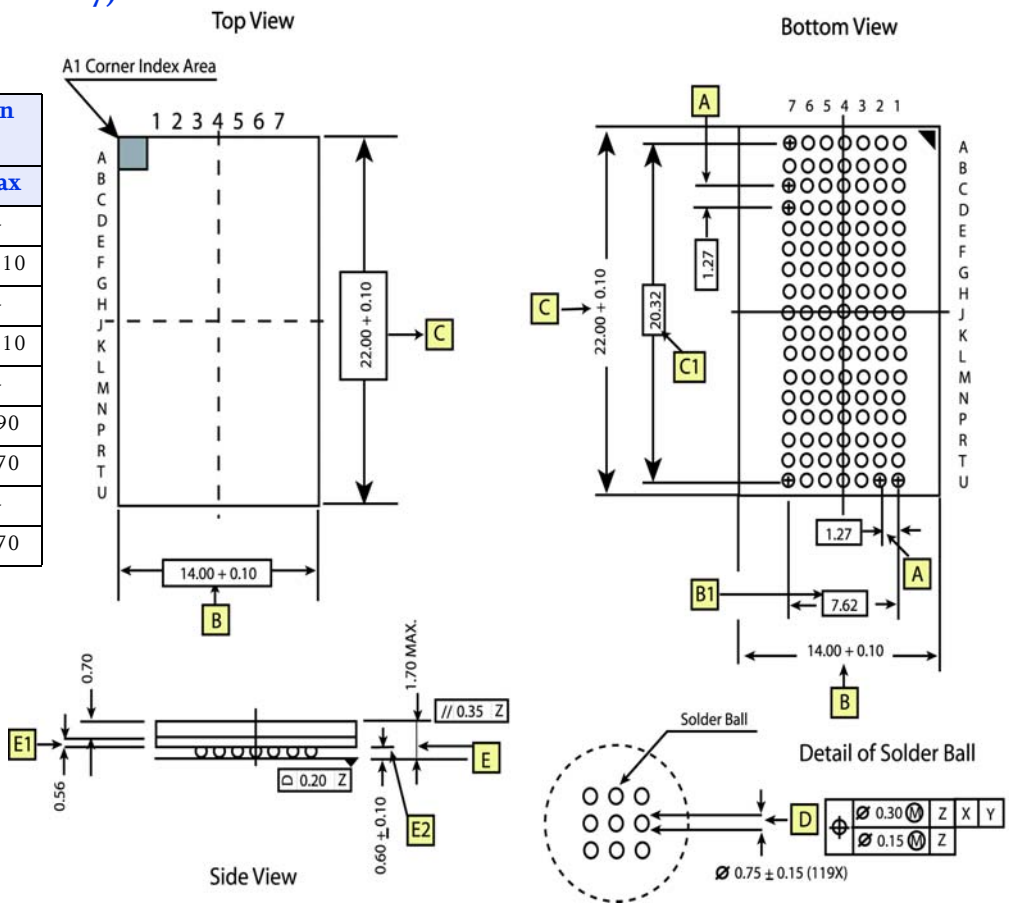
100-pin quad flat pack (TQFP)

	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.90	14.10
E	19.90	20.10
e	0.65 nominal	
Hd	15.90	16.10
He	21.90	22.10
L	0.45	0.75
L1	1.00 nominal	
α	0°	7°
Dimensions in millimeters		



119-ball BGA (ball grid array)

All measurements are in mm.			
	Min	Typ	Max
A	-	1.27	-
B	13.90	14.00	14.10
B1	-	7.62	-
C	21.90	22.00	22.10
C1	-	20.32	-
D	0.60	0.75	0.90
E	-	-	1.70
E1	-	0.56	-
E2	0.50	0.60	0.70



Ordering information

Packages	–166 MHz	–150 MHz	–133 MHz	–100 MHz
x32 TQFP	AS7C33256PFD32A-166TQC	AS7C33256PFD32A-150TQC	AS7C33256PFD32A-133TQC	AS7C33256PFD32A-100TQC
x32 BGA	AS7C33256PFD32A2-166BC	AS7C33256PFD32A2-150BC	AS7C33256PFD32A2-133BC	AS7C33256PFD32A2-100BC
x32 TQFP	AS7C33256PFD32A-166TQI	AS7C33256PFD32A-150TQI	AS7C33256PFD32A-133TQI	AS7C33256PFD32A-100TQI
x32 BGA	AS7C33256PFD32A2-166BI	AS7C33256PFD32A2-150BI	AS7C33256PFD32A2-133BI	AS7C33256PFD32A2-100BI
x36 TQFP	AS7C33256PFD36A-166TQC	AS7C33256PFD36A-150TQC	AS7C33256PFD36A-133TQC	AS7C33256PFD36A-100TQC
x36 BGA	AS7C33256PFD36A2-166BC	AS7C33256PFD36A2-150BC	AS7C33256PFD36A2-133BC	AS7C33256PFD36A2-100BC
x36 TQFP	AS7C33256PFD36A-166TQI	AS7C33256PFD36A-150TQI	AS7C33256PFD36A-133TQI	AS7C33256PFD36A-100TQI
x36 BGA	AS7C33256PFD36A2-166BI	AS7C33256PFD36A2-150BI	AS7C33256PFD36A2-133BI	AS7C33256PFD36A2-100BI
x32 TQFP (2 CE)	AS7C33256PFD32A2-166TQC	AS7C33256PFD32A2-150TQC	AS7C33256PFD32A2-133TQC	AS7C33256PFD32A2-100TQC
x32 TQFP (2 CE)	AS7C33256PFD32A2-166TQI	AS7C33256PFD32A2-150TQI	AS7C33256PFD32A2-133TQI	AS7C33256PFD32A2-100TQI
x36 TQFP (2 CE)	AS7C33256PFD36A2-166TQC	AS7C33256PFD36A2-150TQC	AS7C33256PFD36A2-133TQC	AS7C33256PFD36A2-100TQC
x36 TQFP (2 CE)	AS7C33256PFD36A2-166TQI	AS7C33256PFD36A2-150TQI	AS7C33256PFD36A2-133TQI	AS7C33256PFD36A2-100TQI

Part numbering guide

AS7C	33	256	PF	D	32/36	A	blank or 2	–XXX	TQ or B	C/I
1	2	3	4	5	6	7	8	9	10	11

1.Alliance Semiconductor SRAM prefix
2.Operating voltage: 33=3.3V
3.Organization: 256=256K
4.Pipeline-Flowthrough (each device has both options)
5.Deselect: D=Dual cycle deselect
6.Organization: 32=x32; 36=x36
7.Production version: A=first production version
8. Blank = the default:3 CE (chip enable), 2 = 2 CE (2 chip enable)
9.Clock speed (MHz)
10.Package type: TQ=TQFP, B=BGA
11.Operating temperature: C=Commercial (0° C to 70° C); I=Industrial (-40° C to 85° C)