



Integrated Device Technology, Inc.

# CMOS STATIC RAM 1 MEG (256K x 4-BIT)

IDT71028

## FEATURES:

- 256K x 4 advanced high-speed CMOS static RAM
- Equal access and cycle times
  - Commercial: 12/15/17/20ns
- One Chip Select plus one Output Enable pin
- Bidirectional data Inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 400 mil Plastic SOJ package

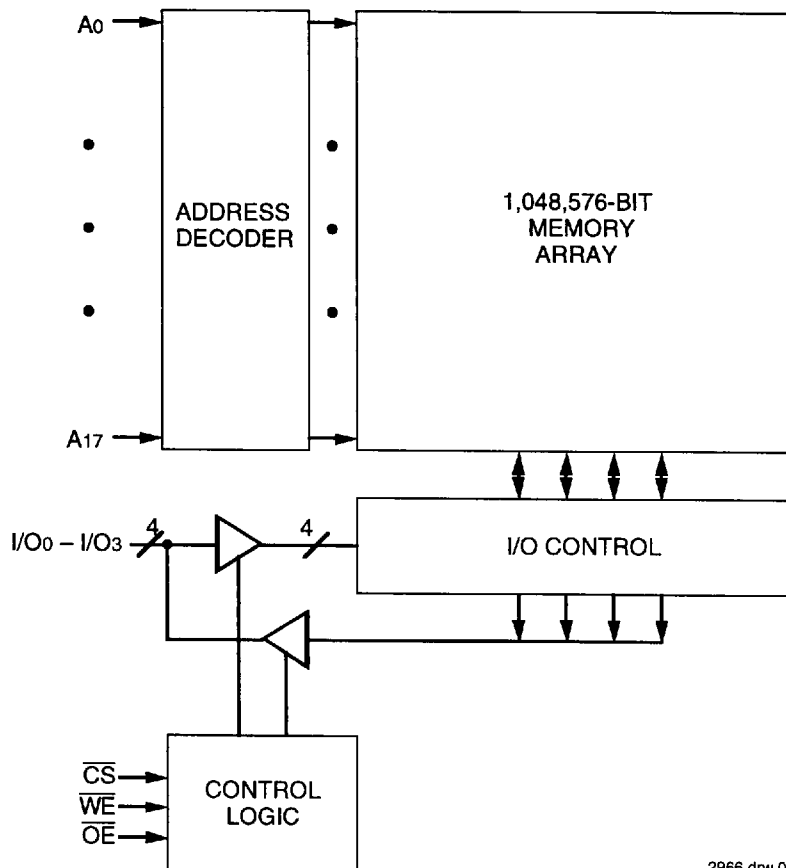
## DESCRIPTION:

The IDT71028 is a 1,048,576-bit high-speed static RAM organized as 256K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71028 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71028 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71028 is packaged in 28-pin 400 mil Plastic SOJ package.

## FUNCTIONAL BLOCK DIAGRAM



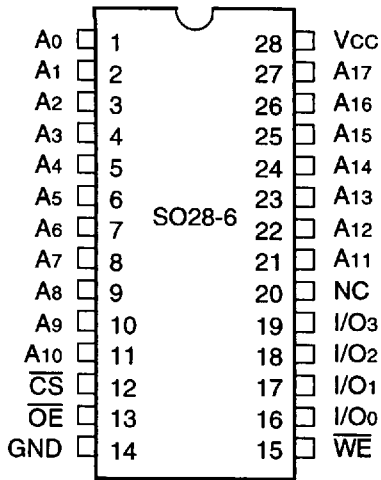
2966 drw 01

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**COMMERCIAL TEMPERATURE RANGE**

**AUGUST 1996**

**PIN CONFIGURATION**



SOJ  
TOP VIEW

2966 drw 02

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Com'l.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	1.25	W
IOUT	DC Output Current	50	mA

**NOTES:**

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 0.5V.

**TRUTH TABLE<sup>(1,2)</sup>**

CS	OE	WE	I/O	Function
L	L	H	DATAOUT	Read Data
L	X	L	DATAIN	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I <sub>SB</sub> )
V <sub>HC</sub> <sup>(3)</sup>	X	X	High-Z	Deselected - Standby (I <sub>SB1</sub> )

**NOTES:**

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- H = V<sub>IH</sub>, L = V<sub>IL</sub>, x = Don't care.
- V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V.
- Other inputs ≥ V<sub>HC</sub> or ≤ V<sub>LC</sub>.

**CAPACITANCE**

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	8	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	8	pF

**NOTE:**

2966 tbl 03

- This parameter is guaranteed by device characterization, but not production tested.

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:**

2966 tbl 04

- V<sub>IL</sub> (min.) = -1.5V for pulse width less than 10ns, once per cycle.

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71028		Unit
			Min.	Max.	
I <sub>I</sub> L <sub>I</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	—	5	μA
I <sub>O</sub> L <sub>O</sub>	Output Leakage Current	V <sub>CC</sub> = Max., CS = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	—	V

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### DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$ )

Symbol	Parameter	71028S12 <sup>(3)</sup>		71028S15		71028S17		71028S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I <sub>CC</sub>	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{MAX}^{(2)}$	155	—	150	—	145	—	145	—	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL Level), $\overline{CS} \geq V_{IH}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{MAX}^{(2)}$	35	—	35	—	35	—	35	—	mA
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = 0^{(2)}$ , $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	10	—	10	—	10	—	10	—	mA

**NOTES:**

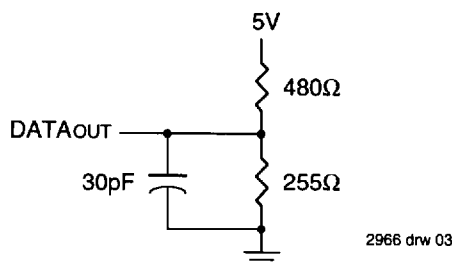
- All values are maximum guaranteed values.
- $f_{MAX} = 1/t_{RC}$  (all address inputs are cycling at  $f_{MAX}$ );  $f = 0$  means no address input lines are changing.
- 12ns specification is preliminary.

2966 tbl 06

### AC TEST CONDITIONS

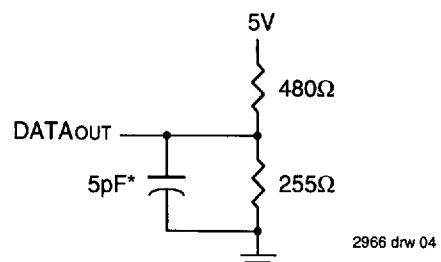
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2966 tbl 07



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Figure 1. AC Test Load



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\*Including jig and scope capacitance.

Figure 2. AC Test Load  
(for t<sub>CLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ</sub>, t<sub>OHZ</sub>, t<sub>OW</sub>, and t<sub>WHZ</sub>)

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ , Commercial Temperature Range)

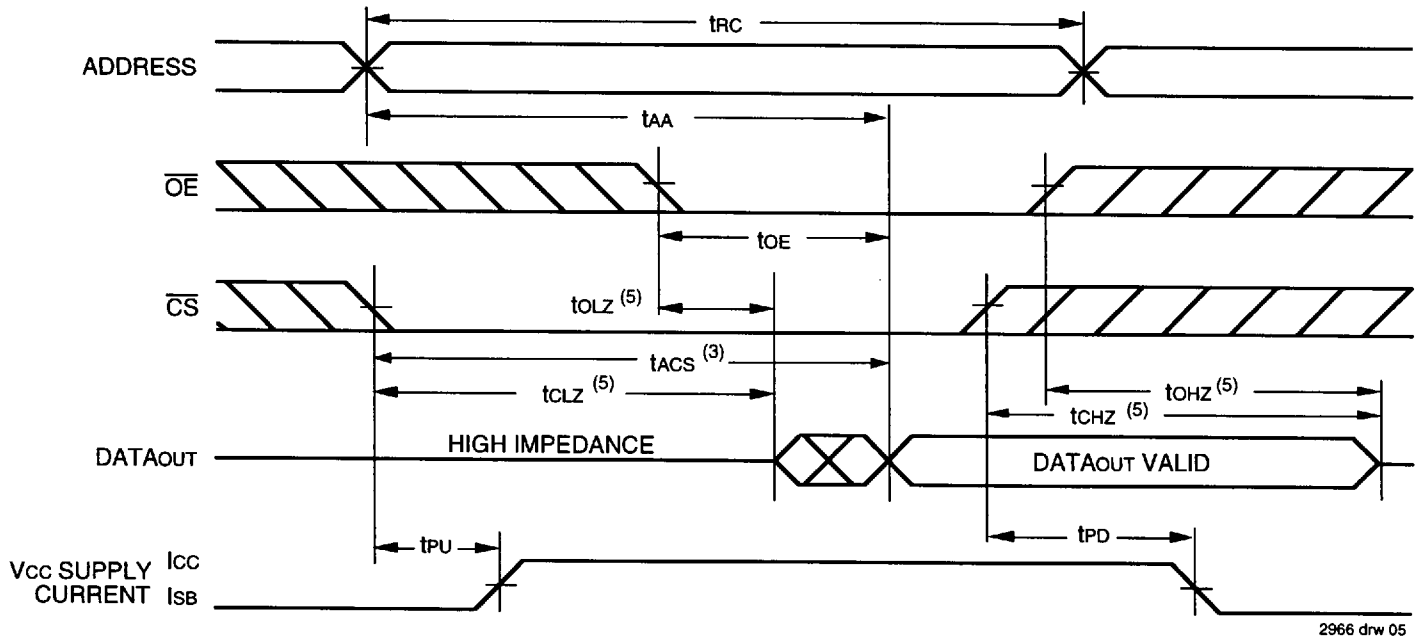
Symbol	Parameter	71028S12 <sup>(1)</sup>		71028S15		71028S17		71028S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	12	—	15	—	17	—	20	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	15	—	17	—	20	ns
t <sub>ACS</sub>	Chip Select Access Time	—	12	—	15	—	17	—	20	ns
t <sub>CLZ</sub> <sup>(2)</sup>	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t <sub>CHZ</sub> <sup>(2)</sup>	Chip Deselect to Output in High-Z	0	6	0	7	0	8	0	8	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	6	—	7	—	8	—	8	ns
t <sub>OLZ</sub> <sup>(2)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(2)</sup>	Output Disable to Output in High-Z	0	5	0	5	0	6	0	7	ns
t <sub>OH</sub>	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t <sub>PU</sub> <sup>(2)</sup>	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(2)</sup>	Chip Deselect to Power Down Time	—	12	—	15	—	17	—	20	ns
<b>Write Cycle</b>										
t <sub>WC</sub>	Write Cycle Time	12	—	15	—	17	—	20	—	ns
t <sub>AW</sub>	Address Valid to End of Write	10	—	12	—	13	—	15	—	ns
t <sub>CW</sub>	Chip Select to End of Write	10	—	12	—	13	—	15	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	10	—	12	—	13	—	15	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data Valid to End of Write	7	—	8	—	9	—	9	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(2)</sup>	Output Active from End of Write	3	—	3	—	3	—	4	—	ns
t <sub>WHZ</sub> <sup>(2)</sup>	Write Enable to Output in High-Z	0	5	0	5	0	7	0	8	ns

**NOTES:**

- 12ns specification is preliminary.
- This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

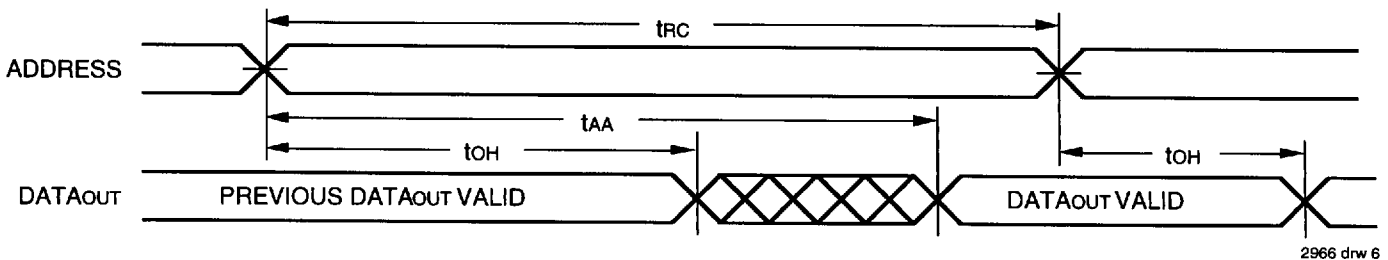
2966 tbl 08

**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**



2966 drw 05

**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1,2,4)</sup>**

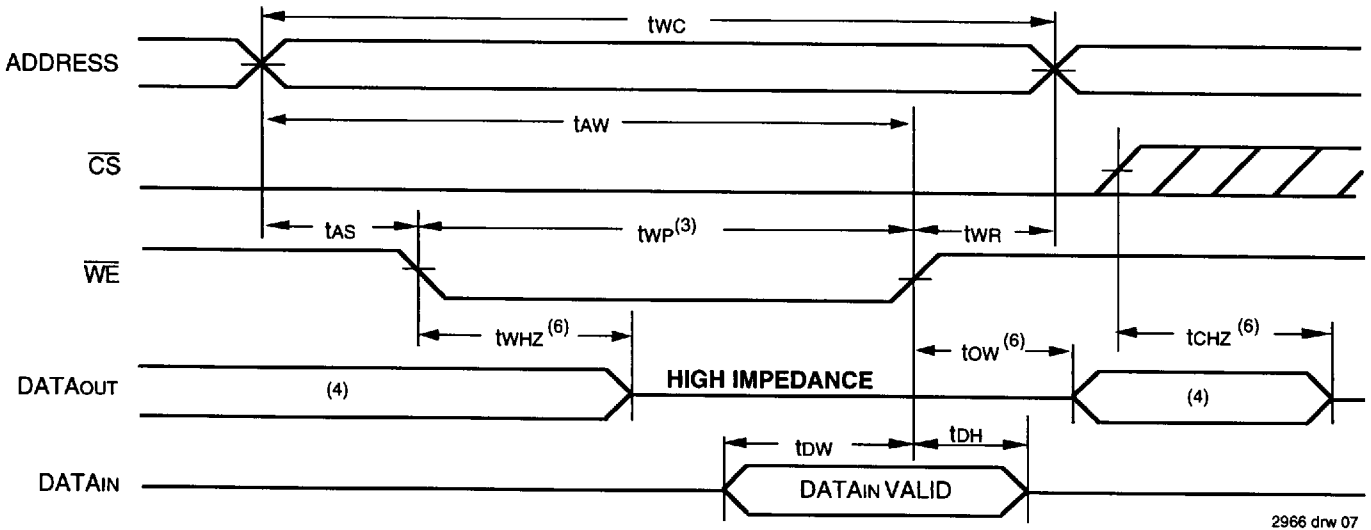


2966 drw 6

**NOTES:**

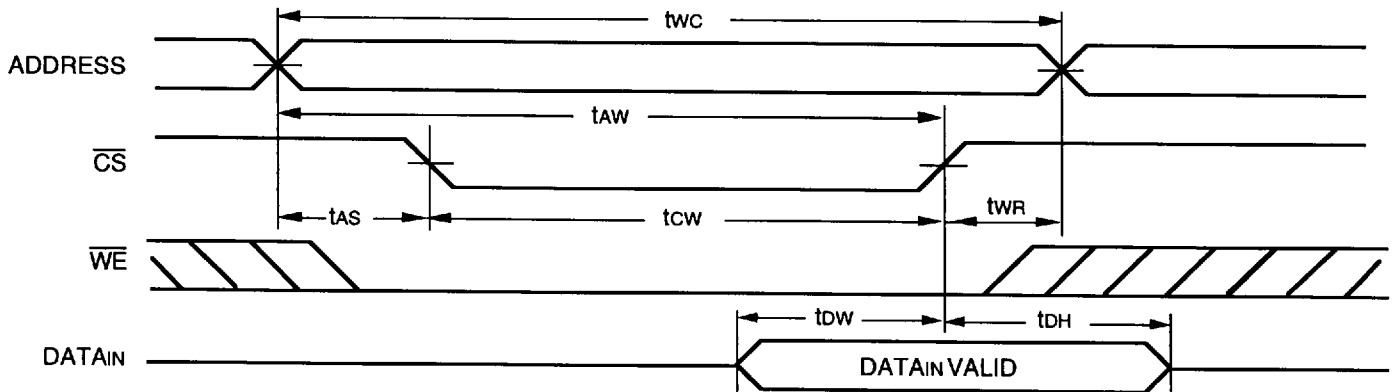
1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected,  $\overline{CS}$  is LOW.
3. Address must be valid prior to or coincident with the later of  $\overline{CS}$  transition LOW; otherwise  $t_{AA}$  is the limiting parameter.
4.  $\overline{OE}$  is LOW.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

**TIMING WAVEFORM OF WRITE CYCLE NO.1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1,2,3,5)</sup>**



2966 drw 07

**TIMING WAVEFORM OF WRITE CYCLE NO.2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1,2,5)</sup>**

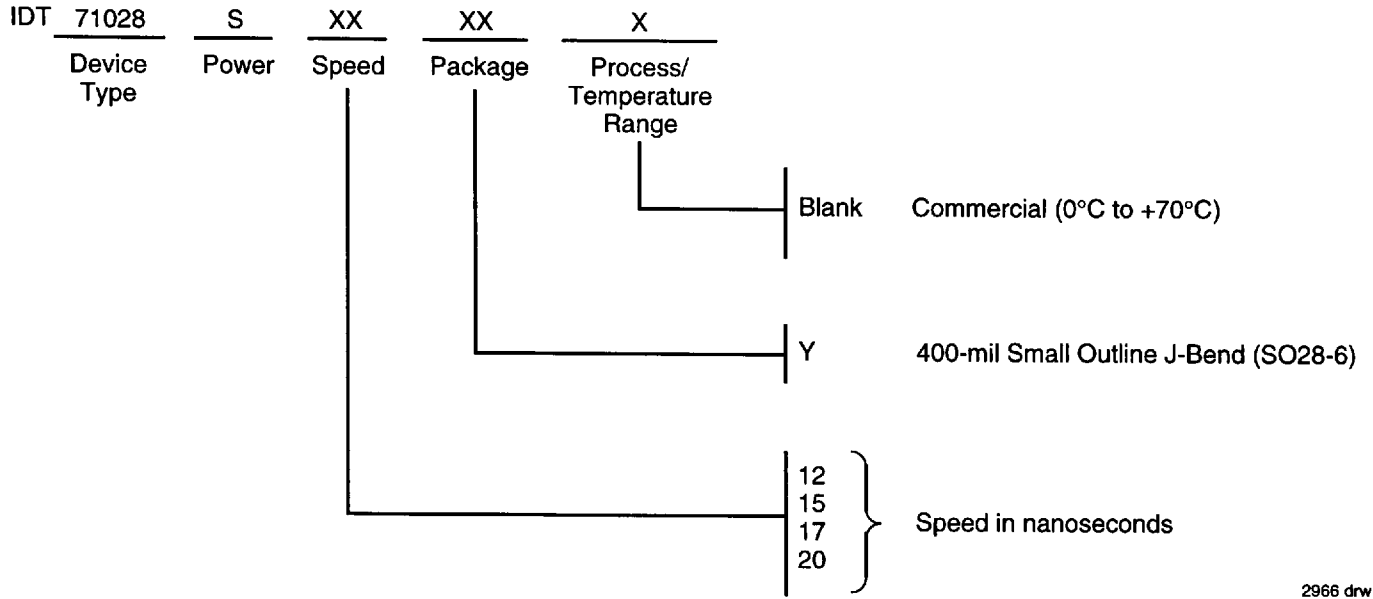


2966 drw 08

**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $\overline{OE}$  is continuously HIGH. If during a  $\overline{WE}$  controlled write cycle  $\overline{OE}$  is LOW,  $t_{WP}$  must be greater than or equal to  $t_{WHZ} + t_{OW}$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified  $t_{WP}$ .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured  $\pm 200mV$  from steady state.

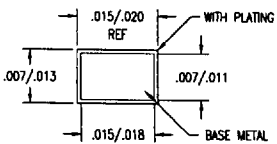
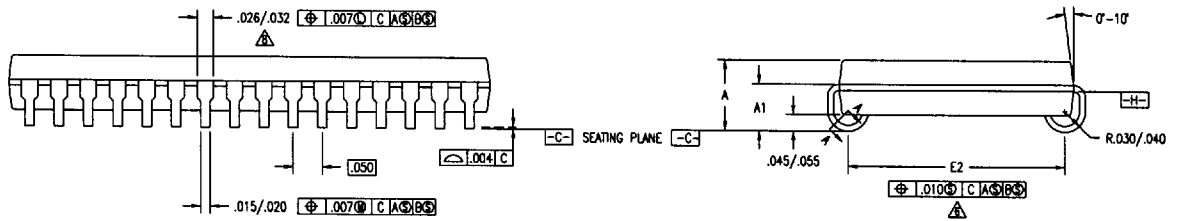
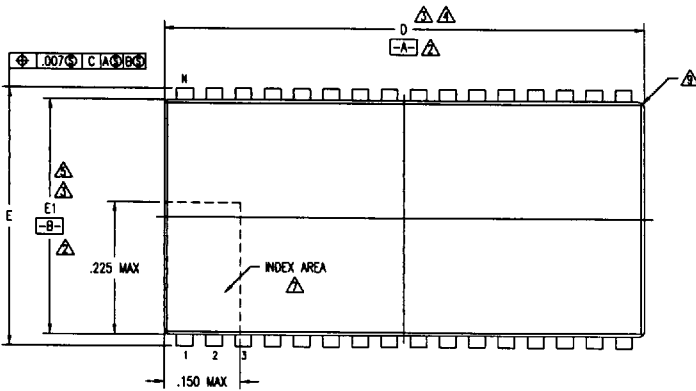
### ORDERING INFORMATION



2966 drw 09

PACKAGE DIAGRAM OUTLINES  
SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20287	00	INITIAL RELEASE	04/11/91	A. KATZ
21863	01	ADD 28 LD	01/24/92	T. VU
27321	02	ADD A2 DIM	11/14/94	T. VU
27645	03	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
27945	04	ADD 44 LD	06/25/95	



SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stonder Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 492-8674 TWC: 910-338-2070
DECIMAL	ANGULAR	
XX±	±	
XXXX		
XXXX±		
APPROVALS	DATE	TITLE
DRWN <i>dt</i>	02/15/96	PB PACKAGE OUTLINE 400" BODY WIDTH SOJ .050" PITCH
CHECKED		
SIZE	DRAWING NO.	REV
C	PSC-4033	04
DO NOT SCALE DRAWING		

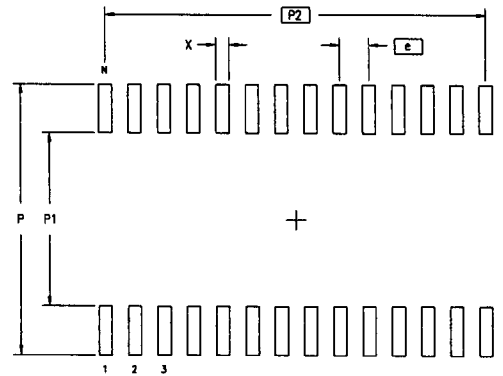


PACKAGE DIAGRAM OUTLINES  
SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20267	00	INITIAL RELEASE	04/11/91	A. KATZ
21863	01	ADD 28 LD	01/24/92	T. WU
27321	02	ADD A2 DIM	11/14/94	T. WU
27645	03	REDRAW TO JEDEC FORMAT	03/15/95	T. WU
27945	04	ADD 44 LD	06/25/95	

SYMBOL	JEDEC #			S028-6			JEDEC #			S032-3			JEDEC #			S044-1		
	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE		
	AA	MIN	NOM		MAX	AB	MIN		NOM	MAX	AE		MIN	NOM	MAX			
A	.131	.138	.145		.131	.138	.145		.131	.138	.145		.131	.138	.145			
A1	.082	-	-		.082	-	-		.082	-	-		.082	-	-			
D	.720	.725	.730	3,4	.820	.825	.830	3,4	1.120	1.125	1.130	3,4	1.120	1.125	1.130	3,4		
E	.435	.440	.445		.435	.440	.445		.435	.440	.445		.435	.440	.445			
E1	.395	.400	.405	3,5	.395	.400	.405	3,5	.395	.400	.405	3,5	.395	.400	.405	3,5		
E2	.360	.370	.380	6	.360	.370	.380	6	.360	.370	.380	6	.360	.370	.380	6		
N	28				32				44				44					

LAND PATTERN DIMENSIONS



NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- DIMENSION E2 TO BE DETERMINED AT SEATING PLANE **-C-** CONTACT POINT
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .005 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-061, VARIATION AA, AB & AE

	MIN	MAX	MIN	MAX	MIN	MAX
P	.458	.466	.458	.466	.458	.466
P1	.290	.294	.290	.294	.290	.294
P2	.650 BSC		.750 BSC		1.050 BSC	
X	.018	.026	.018	.026	.018	.026
e	.050 BSC		.050 BSC		.050 BSC	
N	28		32		44	

TOLERANCES UNLESS SPECIFIED		 Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 482-8874 TWR: 910-338-2070
DECIMAL	ANGULAR	
±	±	
APPROVALS	DATE	TITLE
DRAWN <i>Ad</i>	02/15/98	PB PACKAGE OUTLINE
CHECKED		.400" BODY WIDTH SOJ
		.050" PITCH
		SIZE
		C
		DRAWING No.
		PSC-4033
		REV
		04
DO NOT SCALE DRAWING		