



**MOTOROLA**

**Military 54F175**

# Quad D-Type Positive Edge-Triggered Flip-Flop

**ELECTRICALLY TESTED PER:  
MIL-M-38510/34104**



The 54F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset
- True and Complement Output

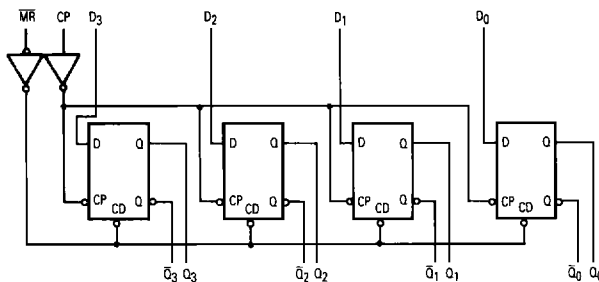
**AVAILABLE AS:**

- 1) JAN: JM38510/34104BXA
- 2) SMD: \*
- 3) 883C: 54F175/BXAJC

**X = CASE OUTLINE AS FOLLOWS:**  
**PACKAGE: CERDIP: E**  
**CERFLAT: F**  
**LCC: 2**

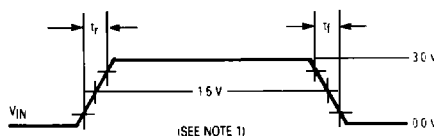
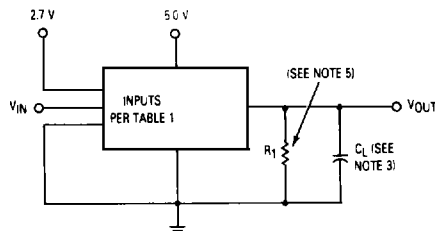
\*Call Factory for latest update

**LOGIC DIAGRAM**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

**AC TEST CIRCUIT**



**PIN ASSIGNMENTS**

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
MR	1	1	2	GND
Q <sub>0</sub>	2	2	3	OPEN
Q <sub>0</sub>	3	3	4	OPEN
D <sub>0</sub>	4	4	5	V <sub>CC</sub>
D <sub>1</sub>	5	5	7	V <sub>CC</sub>
Q <sub>1</sub>	6	6	8	OPEN
Q <sub>1</sub>	7	7	9	OPEN
GND	8	8	10	GND
CP	9	9	12	V <sub>CC</sub>
Q <sub>2</sub>	10	10	13	OPEN
Q <sub>2</sub>	11	11	14	OPEN
D <sub>2</sub>	12	12	15	V <sub>CC</sub>
D <sub>3</sub>	13	13	17	V <sub>CC</sub>
Q <sub>3</sub>	14	14	18	OPEN
Q <sub>3</sub>	15	15	19	OPEN
V <sub>CC</sub>	16	16	20	V <sub>CC</sub>

**BURN-IN CONDITIONS:**  
**V<sub>CC</sub> = 5.0 V MIN/6.0 V MAX**

# 54F175

## FUNCTIONAL DESCRIPTION

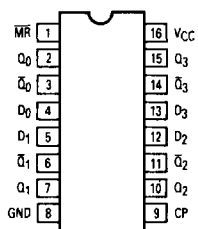
The F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH clock (CP) transition, causing individual Q and  $\bar{Q}$  outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs. The F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

## TRUTH TABLE

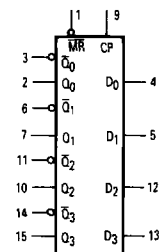
Inputs		Outputs	
$\text{at } t_n, \text{MR} = \text{H}$		$\text{at } t_n + 1$	
$D_n$		$Q_n$	$\bar{Q}_n$
L		L	H
H		H	L

$t_n$  = Bit time before clock pulse  
 $t_n + 1$  = Bit time after clock pulse  
 H = HIGH Voltage Level  
 L = LOW Voltage Level

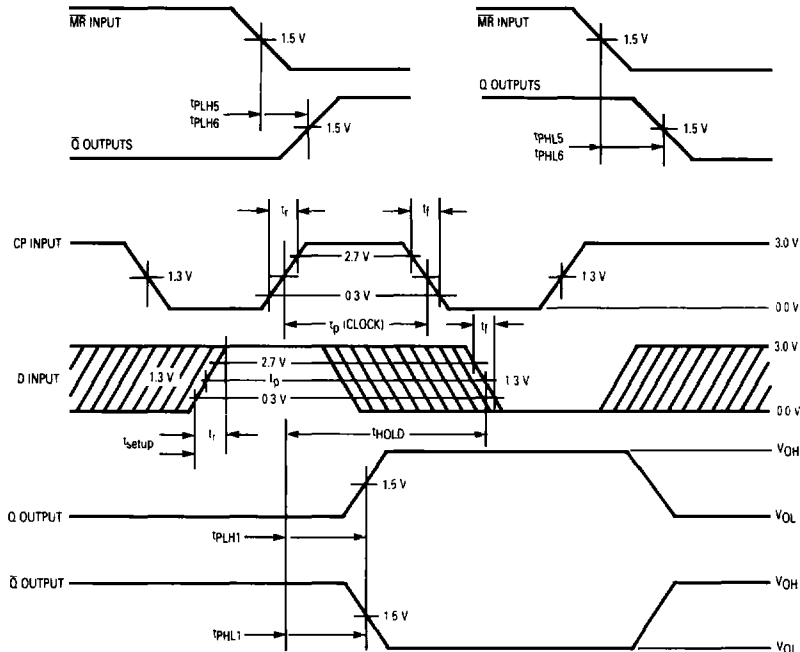
## CONNECTION DIAGRAM



## LOGIC SYMBOL



## WAVEFORMS



The shaded areas indicate when the input is permitted to change for predictable output performance

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1.0 mA, V <sub>IN</sub> = 2.0 V or 0.8 V per truth table.
V <sub>OL</sub>	Logical "0" Output Voltage		0.5		0.5		0.5	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA, V <sub>IN</sub> = 2.0 V or 0.8 V per truth table.
V <sub>IC</sub>	Input Clamping Voltage		-1.2					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V, other inputs are open.
I <sub>IHH</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 7.0 V, other inputs are open.
I <sub>IL</sub>	Logical "0" Input Current (MR, CP, D)	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.5 V, other inputs are open.
I <sub>OD</sub>	Diode Current	60		60		60		mA	V <sub>CC</sub> = 4.5 V, MR = 0 V, other inputs are open, V <sub>OUT</sub> = 2.5 V.
I <sub>OS</sub>	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN(D)</sub> = 0 V, other data inputs are open, MR & CR = (See Note 9), V <sub>OUT</sub> = 0 V.
I <sub>CC</sub>	Power Supply Current		34		34		34	mA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, CP = (See Note 10), other inputs are open.
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.
V <sub>IL</sub>	Logical "0" Input Voltage		0.8		0.8		0.8	V	V <sub>CC</sub> = 4.5 V.
t <sub>s</sub> (H) t <sub>s</sub> (L)	Set Up Time, D High or Low to CP	3.0		3.0		3.0		ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF. (Information only, No Testing Required).
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, D High or Low to CP	1.0		1.0		1.0		ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF. (Information only, No Testing Required).
t <sub>rec</sub>	Recovery Time MR to CP	5.0		5.0		5.0		ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF. (Information only, No Testing Required).
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 4.5 V, (Repeat at) V <sub>CC</sub> = 5.5 V, V <sub>INL</sub> = 0.5 V, and V <sub>INH</sub> = 2.5 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
tPHL1	Propagation Delay Data-Output Clock to Q <sub>n</sub>	4.0	8.5	3.5	10.5	3.5	10.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.
tPLH1	Propagation Delay Data-Output Clock to Q <sub>n</sub>	4.0	6.5	3.5	8.5	3.5	8.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.
tPHL2	Propagation Delay Data-Output Clock to Q̄ <sub>n</sub>	4.0	8.5	3.5	10.5	3.5	10.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.
tPLH2	Propagation Delay Data-Output Clock to Q̄ <sub>n</sub>	4.0	6.5	3.5	8.5	3.5	8.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.
tPHL5	Propagation Delay Data-Output MR to Q <sub>n</sub>	4.5	11.5	4.5	15	4.5	15	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.
tPLH5	Propagation Delay Data-Output MR to Q <sub>n</sub>	4.0	8.0	4.0	10	4.0	10	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.
tPHL6	Propagation Delay Data-Output MR to Q̄ <sub>n</sub>	4.5	11.5	4.5	15	4.5	15	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.
tPLH6	Propagation Delay Data-Output MR to Q̄ <sub>n</sub>	4.0	8.0	4.0	10	4.0	10	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.
f <sub>MAX</sub>	Maximum Clock Frequency	100		80		80		MHz	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 499 Ω ± 5.0%.

## NOTES:

- V<sub>IN</sub> = Input pulse has the following characteristics:  
t<sub>r</sub> = t<sub>f</sub> ≈ 2.5 ns, PRR ≤ 1.0 MHz, or as specified in table 1, PRR (Subgroups 10 and 11) have a duty cycle 50 ± 15%, t<sub>p</sub> = 5.0 ns (Min).
- Inputs not under test are at GND. (See Note 8).
- C<sub>L</sub> = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
- Voltage measurements are to be made with respect to network ground terminal.
- R<sub>1</sub> = 499 Ω ± 5.0%.
- f<sub>MAX</sub> minimum limit specified is the input pulse. The output frequency shall be 1:2 the input frequency.
- Clock, Clear and Set inputs need to be in the proper configuration for specified output conditions.
- Terminal conditions (pins not designated may be High ≥ 2.0 V, Low ≤ 0.8 V, or open).
- Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to MR, then apply 3.0 V, 0 V, 3.0 V to CP, then make measurement.
- Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to CP, then make measurement.