



Features

- FCC approved method of EMI attenuation.
- Generates a 1X low EMI spread spectrum clock of the input frequency.
- Input frequency range: 15MHz – 27MHz.
- Internal loop filter minimizes external components and board space.
- Frequency deviation: -2.5%
- Low inherent cycle-to-cycle jitter.
- 3.3V operating voltage.
- TTL or CMOS compatible inputs and outputs.
- Ultra-low power CMOS design.
 - TBD mA @ 3.3V, 24MHz
- Pinout compatible with Cypress CY25811. Products are available for industrial temperature range.
- Available in 8-pin SOIC and TSSOP.

Product Description

The ASM3P2821B is a versatile spread spectrum frequency modulator designed specifically for input clock frequencies in the range of 15MHz - 27MHz. The ASM3P2821B can generate an EMI reduced clock from a ceramic resonator or system clock. The ASM3P2821B offers a percentage deviation of -2.5%.

The ASM3P2821B reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The ASM3P2821B allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

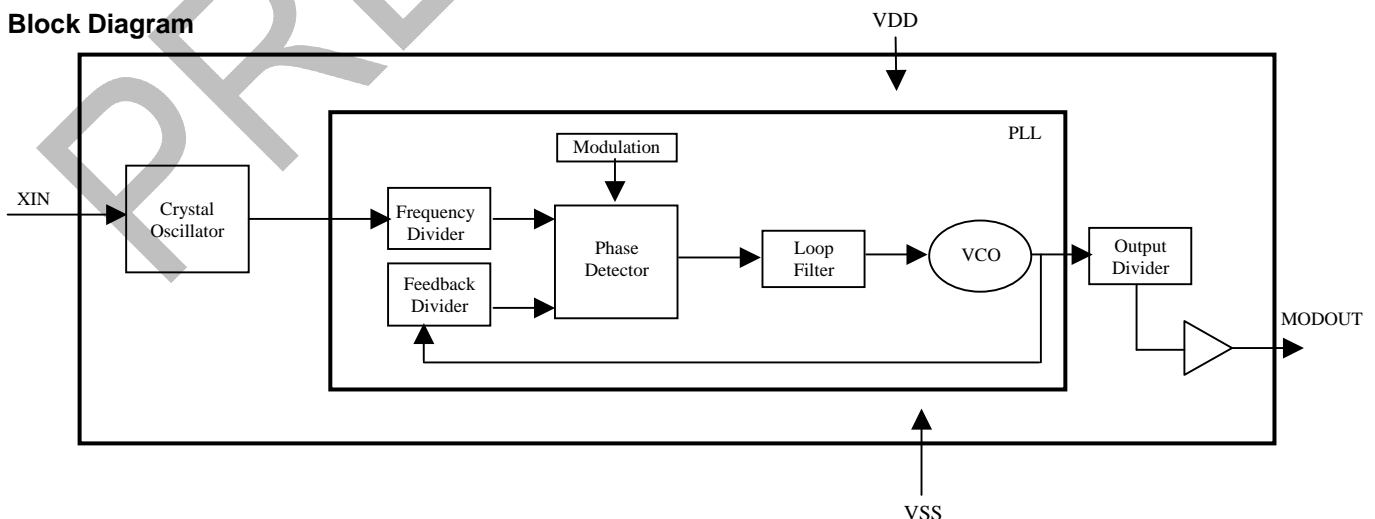
The ASM3P2821B uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

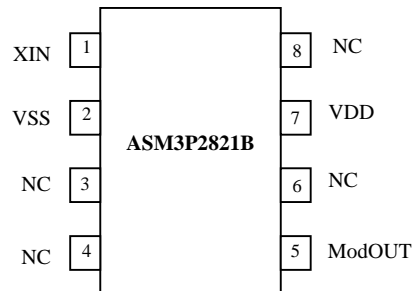
The ASM3P2821B modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

Applications

The ASM3P2821B is targeted towards EMI management for high speed digital applications such as PC peripheral devices, consumer electronics and embedded controller systems.

Block Diagram



**Pin Configuration****Pin Description**

| Pin# | Pin Name | Type | Description |
|------|----------|------|--|
| 1 | XIN | I | External reference clock input. |
| 2 | VSS | P | Ground to entire chip. |
| 3 | NC | | No Connect. |
| 4 | NC | | No Connect. |
| 5 | MODOUT | O | Spread spectrum low EMI output. |
| 6 | NC | | No Connect. |
| 7 | VDD | P | Power supply for the entire chip (3.3V). |
| 8 | NC | | No Connect. |

**Absolute Maximum Ratings**

| Symbol | Parameter | Rating | Unit |
|----------|--|---------------|------|
| VDD, VIN | Voltage on any pin with respect to GND | -0.5 to + 7.0 | V |
| TSTG | Storage temperature | -65 to +125 | °C |
| TA | Operating temperature | 0 to 70 | °C |

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|---|-----------|-----|-----------------------|------|
| V _{IL} | Input low voltage | GND – 0.3 | - | TBD | V |
| V _{IH} | Input high voltage | TBD | - | V _{DD} + 0.3 | V |
| I _{IL} | Input low current | | TBD | | µA |
| I _{IH} | Input high current | | TBD | | µA |
| V _{OL} | Output low voltage (V _{DD} = 3.3V, I _{OL} = 4mA) | | TBD | | V |
| V _{OH} | Output high voltage (V _{DD} = 3.3V, I _{OH} = 4mA) | | TBD | | V |
| I _{CC} | Dynamic supply current normal mode (3.3V and 10pF loading) | | TBD | | mA |
| I _{DD} | Static supply current standby mode | | TBD | | µA |
| V _{DD} | Operating voltage | TBD | 3.3 | TBD | V |
| t _{ON} | Power up time (first locked clock cycle after power up) | - | TBD | - | mS |
| Z _{OUT} | Clock out impedance | - | TBD | - | Ω |



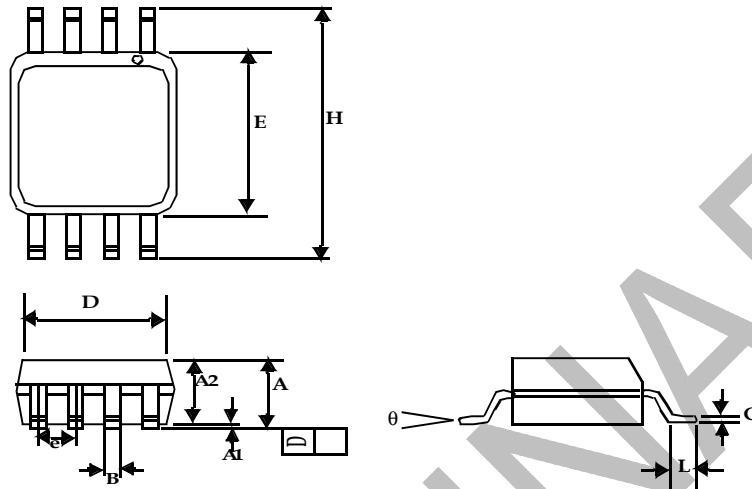
AC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|-----|-----|-----|------|
| XIN | Input frequency | 15 | 24 | 27 | MHz |
| MODOUT | Output frequency | 15 | 24 | 27 | MHz |
| t_{LH}^* | Output rise time (measured at 0.8V to 2.0V) | | TBD | | ns |
| t_{HL}^* | Output fall time (measured at 2.0V to 0.8V) | | TBD | | ns |
| t_{JC} | Jitter (cycle to cycle) | - | - | TBD | ps |
| t_D | Output duty cycle | - | TBD | - | % |
| * t_{LH} and t_{HL} are measured into a capacitive load of 15pF | | | | | |



Package Information

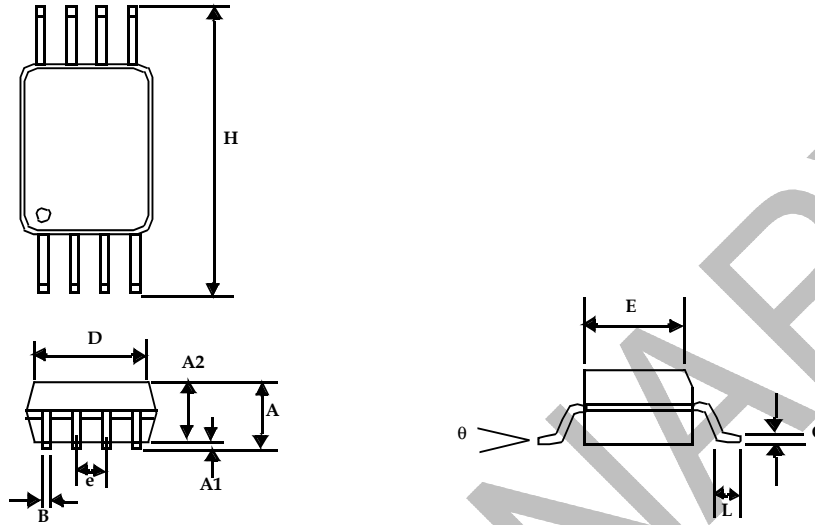
8-Pin SOIC



| Symbol | Dimensions in inches | | Dimensions in millimeters | |
|--------|----------------------|-------|---------------------------|------|
| | Min | Max | Min | Max |
| A | 0.057 | 0.071 | 1.45 | 1.80 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| A2 | 0.053 | 0.069 | 1.35 | 1.75 |
| B | 0.012 | 0.020 | 0.31 | 0.51 |
| C | 0.004 | 0.01 | 0.10 | 0.25 |
| D | 0.186 | 0.202 | 4.72 | 5.12 |
| E | 0.148 | 0.164 | 3.75 | 4.15 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.224 | 0.248 | 5.70 | 6.30 |
| L | 0.012 | 0.028 | 0.30 | 0.70 |
| □ | 0° | 8° | 0° | 8° |



8-Pin TSSOP



| Symbol | Dimensions in inches | | Dimensions in millimeters | |
|----------|----------------------|-------|---------------------------|------|
| | Min | Max | Min | Max |
| A | 0.047 | | | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.031 | 0.041 | 0.80 | 1.05 |
| B | 0.007 | 0.012 | 0.19 | 0.30 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.114 | 0.122 | 2.90 | 3.10 |
| E | 0.169 | 0.177 | 4.30 | 4.50 |
| e | 0.026 BSC | | 0.65 BSC | |
| H | 0.244 | 0.260 | 6.20 | 6.60 |
| L | 0.018 | 0.030 | 0.45 | 0.75 |
| θ | 0° | 8° | 0° | 8° |



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