HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTER

IDT74FCT821AT/CT

FEATURES:

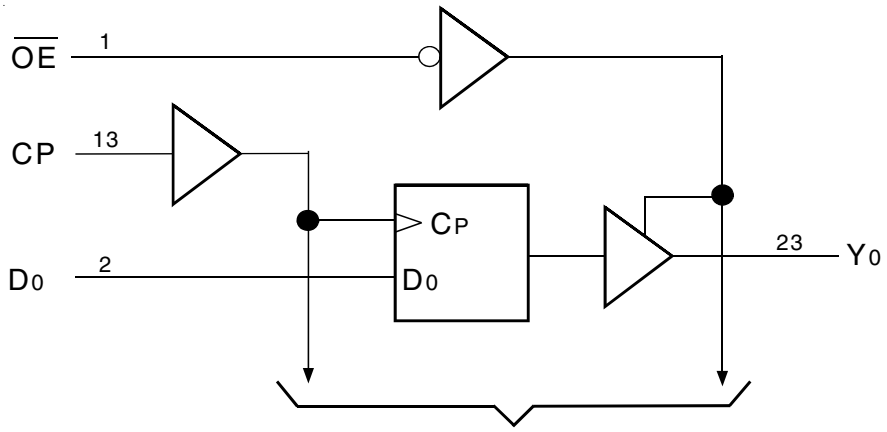
- **A and C grades**
- **Low input and output leakage ≤1µA (max.)**
- **CMOS power levels**
- **True TTL input and output compatibility:**
  - *V_{OH} = 3.3V (typ.)*
  - *V_{OL} = 0.3V (typ.)*
- **High Drive outputs (-15mA I_{OH}, 48mA I_{OL})**
- **Meets or exceeds JEDEC standard 18 specifications**
- **Power off disable outputs permit "live insertion"**
- **Available in SOIC and QSOP packages**

DESCRIPTION:

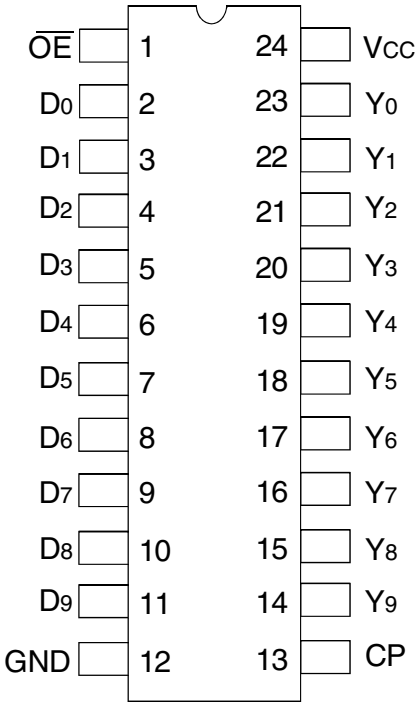
The 74FCT821T series is built using an advanced dual metal CMOS technology. The 74FCT821T series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The 74FCT821T is a buffered, 10-bit wide version of the popular 74FCT374T function.

The 74FCT821T high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Name	I/O	Description
Dx	I	D Flip-Flop Data Inputs
$\overline{CLR}$	I	When the clear input is LOW and $\overline{OE}$ is LOW, the Qx outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register. Enters data into the register on the LOW-to-HIGH transition
Yx	O	Register 3-State Outputs
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the Dx input is transferred to the Qx input on the LOW-to-HIGH transition. When the clock enable is HIGH, the Qx inputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Yx outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Yx outputs.

FUNCTION TABLE(1)

Inputs					Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	Dx	CP	Qx	Yx	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State output pins)(4)		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min, I_{IN} = -18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = –8mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	2	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 48mA	—	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}					
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
		$\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at fi = 5MHz	V_{IN} = 3.4V V_{IN} = GND	—	2	5.5	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
		$\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling at fi = 2.5MHz	V_{IN} = 3.4V V_{IN} = GND	—	6	16.3[5]	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Output Frequency
   N_i = Number of Outputs at f_i

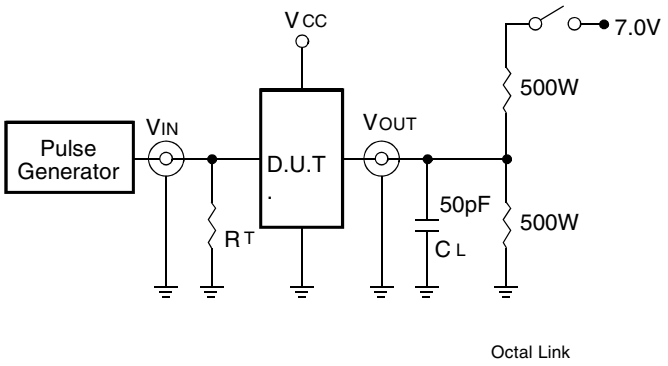
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	74FCT821AT		74FCT821CT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Yx ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	1.5	10	1.5	6	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	20	1.5	12.5	
t_{SU}	Set-up Time HIGH or LOW Dx or $\overline{EN}$ to CP	C_L = 50pF R_L = 500Ω	4	—	3	—	ns
t_H	Hold Time HIGH or LOW,	Dx to CP	2	—	1.5	—	ns
t_H	Hold Time HIGH or LOW,	$\overline{EN}$ to CP	2	—	0	—	ns
t_{PHL}	Propagation Delay, $\overline{CLR}$ to Yx		1.5	14	1.5	8	ns
t_{REM}	Recovery Time, $\overline{CLR}$ to CP		6	—	6	—	ns
t_W	Clock Pulse Width, HIGH or LOW		7	—	6	—	ns
t_W	$\overline{CLR}$ Pulse Width LOW		6	—	6	—	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{OE}$ to Yx	C_L = 50pF R_L = 500Ω	1.5	12	1.5	7	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	23	1.5	12.5	
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{OE}$ to Yx	C_L = 5pF[3] R_L = 500Ω	1.5	7	1.5	6	ns
		C_L = 50pF R_L = 500Ω	1.5	8	1.5	6.5	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This condition is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS



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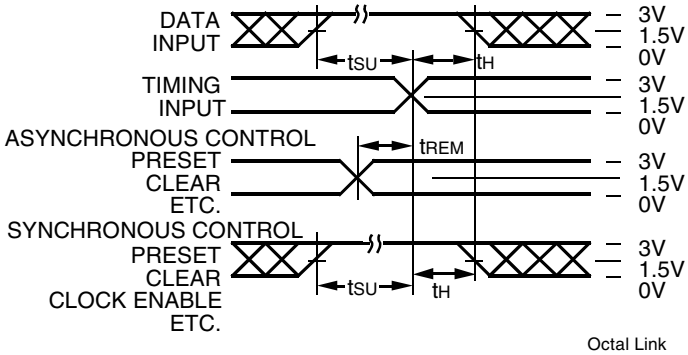
Test Circuits for All Outputs



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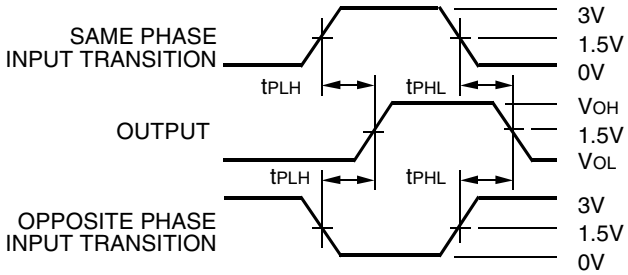
Set-Up, Hold, and Release Times



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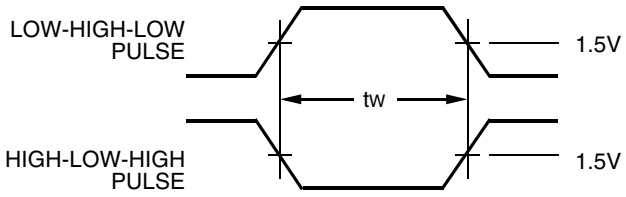
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

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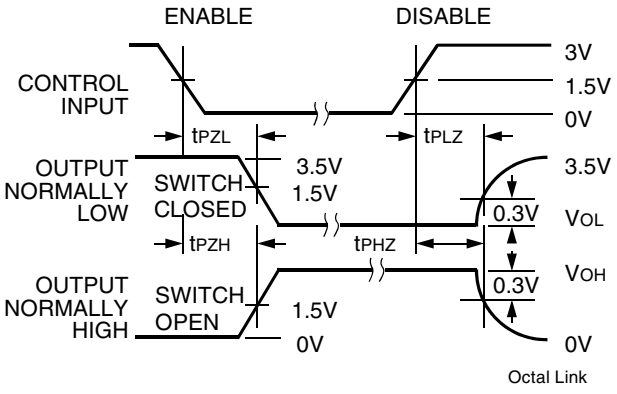

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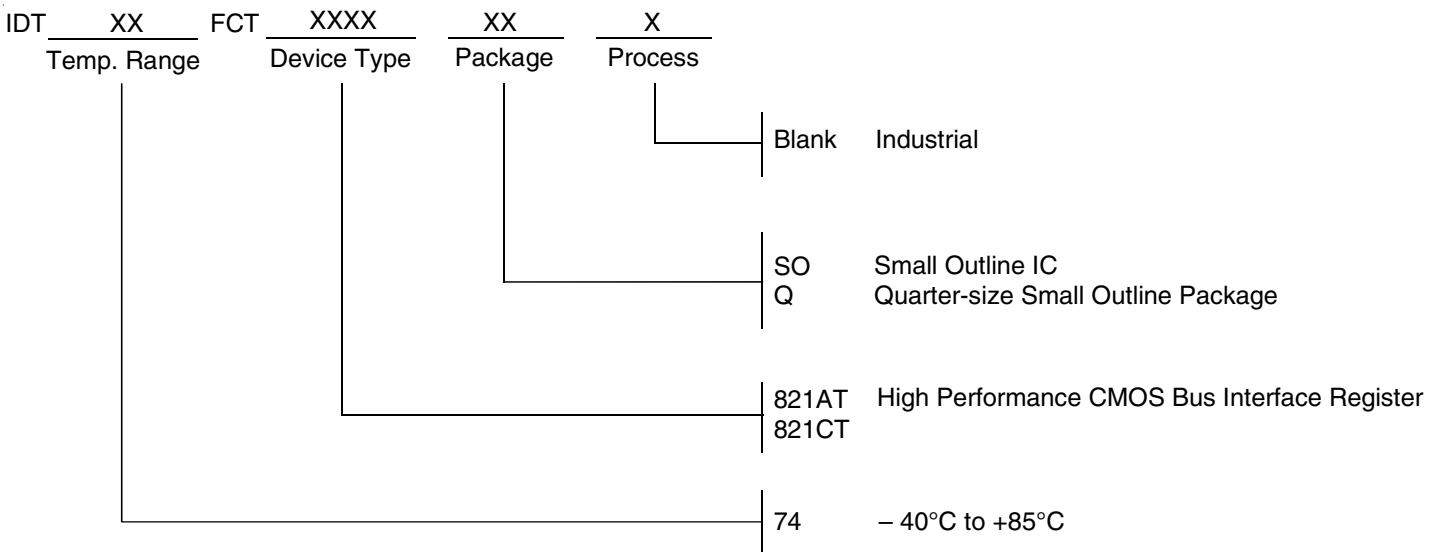
Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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