

Dual J-K Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS

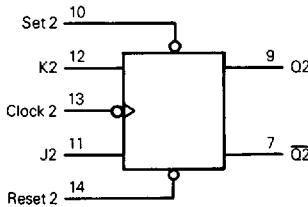
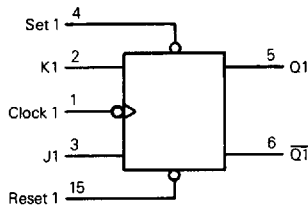
The MC54/74HC112 is identical in pinout to the LS112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

The HC112 is identical in function to the HC76, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Similar in Function to the LS112 Except When Set and Reset are Low Simultaneously
- Chip Complexity: 100 FETs or 25 Equivalent Gates

LOGIC DIAGRAM



Pin 16 = V_{CC}
 Pin 8 = GND

MC54/74HC112



**J SUFFIX
 CERAMIC
 CASE 620-09**



**N SUFFIX
 PLASTIC
 CASE 648-06**



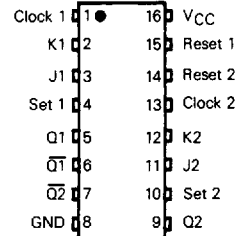
**D SUFFIX
 SOIC
 CASE 751B-04**

ORDERING INFORMATION

MC74HCXXXD SOIC
 MC74HCXXXN Plastic
 MC54HCXXXJ Ceramic

T_A = -55° to 125°C for all packages.
 Dimensions in Chapter 6.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs			
Set	Reset	Q	Q̄		
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L*	L*
H	H	~	L	L	No Change
H	H	~	L	H	L
H	H	~	H	L	H
H	H	~	H	H	Toggle
H	H	L	X	X	No Change
H	H	H	X	X	No Change
H	H	~	X	X	No Change

*Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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MC54/74HC112

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Reset to Q or \bar{Q} (Figures 2 and 4)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set to Q or \bar{Q} (Figures 2 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

SWITCHING WAVEFORMS

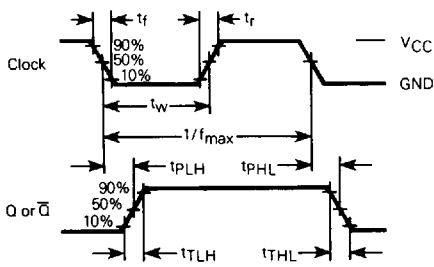


Figure 1.

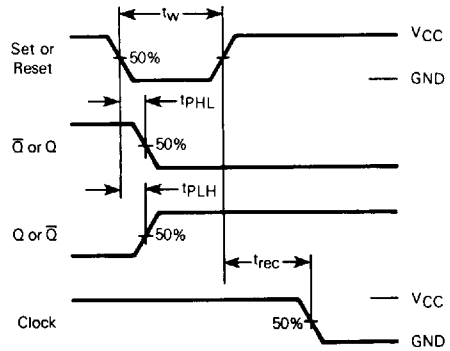


Figure 2.

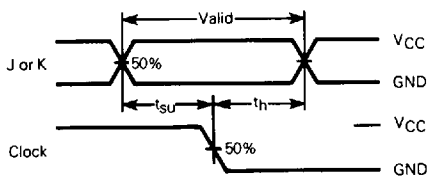
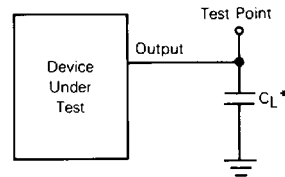


Figure 3.



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM

