TC74LCX16374AFT

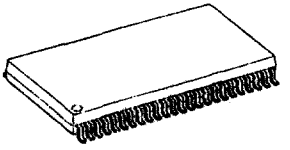
Low Voltage 16-Bit D-TYPE FLIP-FLOP with 5V Tolerant Inputs and Outputs

The TC74LCX16374AFT is a high performance CMOS 16-bit D-TYPE FLIP-FLOP. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaning the CMOS low power dissipation.

The device is designed for low voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This 16-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ($\overline{OE}$) which are common to each byte. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. When the $\overline{OE}$ input is high, the outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.

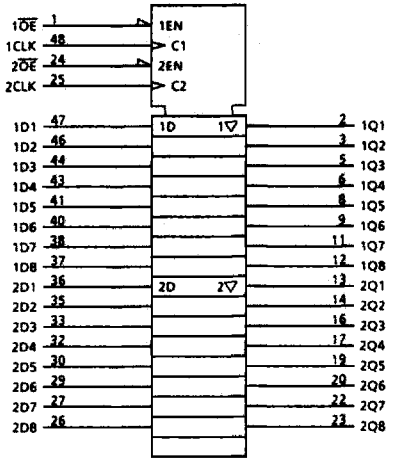


TSSOP48-P-61

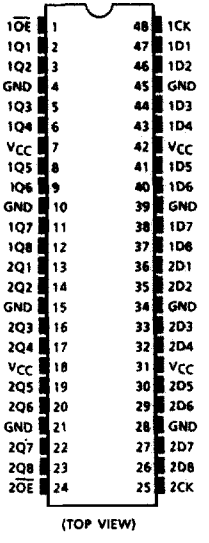
Weight : 0.25 g (Typ.)

Features

- Low Voltage Operation: V_{CC} = 2.0 ~ 3.6V
- High Speed: t_{pd} = 7.0ns (Max.) at V_{CC} = 3.0 ~ 3.6V
- Output Current: $|I_{OH}|/I_{OL}$ = 24mA (Min.) V_{CC} = 3.0V
- Latch up Performance: ±500mA
- Package: TSSOP (Thin Shrink Small Outline Package)
- Power down protection is provided on all inputs and outputs.



IEC Logic Symbol



(TOP VIEW)

Pin Assignment

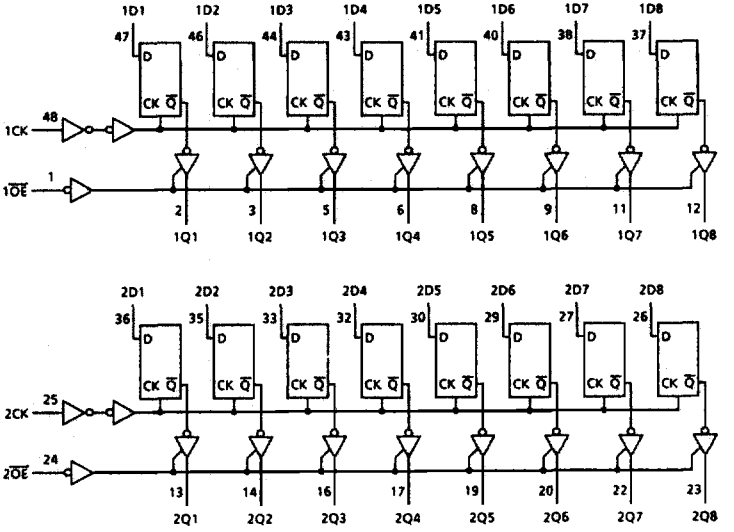
Truth Table

Input			Output
$1\overline{OE}$	1CK	1D1 - 1D8	1Q1 - 1Q8
H	X	X	Z
L	↑	X	Qn
L	↓	L	L
L	↓	H	H

Input			Output
$2\overline{OE}$	2CK	2D1 - 2D8	2Q1 - 2Q8
H	X	X	Z
L	↑	X	Qn
L	↓	L	L
L	↓	H	H

X : Don't Care
Z : High Impedance
Qn : No Change

System Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
DC Input Voltage	V_{IN}	-0.5 ~ 7.0	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5 ~ 7.0 (*1)	V
		-0.5 ~ V_{CC} + 0.5 (*2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	±50 (*3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	400	mW
DC V_{CC}/Ground Current Per Supply Pin	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	-65 ~ 150	°C

(*1) Off-State
(*2) High or Low State. I_{OUT} absolute maximum rating must be observed
(*3) V_{OUT} < GND, V_{OUT} > V_{CC}

Recommended Operating Range

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	2.0 ~ 3.6	V
		1.5 ~ 3.6 (*4)	
Input Voltage	V_{IN}	0 ~ 5.5	V
Bus I/O Voltage	$V_{I/O}$	0 ~ 5.5 (*5)	V
		0 ~ V_{CC} (*6)	
Output Current	I_{OH}/I_{OL}	±24 (*7)	mA
		±12 (*8)	
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	dt/dv	0 ~ 10 (*9)	ns/V

(*4) Data Retension Only
(*5) Off-State
(*6) High or Low State
(*7) V_{CC} = 3.0 ~ 3.6V
(*8) V_{CC} = 2.7 ~ 3.0V
(*9) V_{IN} = 0.8 ~ 2.0V, V_{CC} = 3.0V

Electrical Characteristics

DC Characteristics (Ta = -40 ~ 85°C)

Parameter		Symbol	Test Condition		V_{CC} (V)	Min.	Max.	Unit
Input Voltage	"H" Level	V_{IH}			2.7 ~ 3.6	2.0	–	V
	"L" Level	V_{IL}			2.7 ~ 3.6	–	0.8	V
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -100μA	2.7 ~ 3.6	V_{CC} - 0.2	–	V
				I_{OH} = -12mA	2.7	2.2	–	
				I_{OH} = -18mA	3.0	2.4	–	
				I_{OH} = -24mA	3.0	2.2	–	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7 ~ 3.6	–	0.2	V
				I_{OL} = 16mA	3.0	–	0.4	
				I_{OL} = 12mA	2.7	–	0.4	
				I_{OL} = 24mA	3.0	–	0.55	
Input Leakage Current		I_{IN}	V_{IN} = 0 ~ 5.5V		2.7 ~ 3.6	–	±5.0	μA
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{IN} = 0 ~ 5.5V		2.7 ~ 3.6	–	±5.0	μA
Power Off Leakage Current		I_{OFF}	V_{IN}/V_{OUT} = 5.5V		0	–	10.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		2.7 ~ 3.6	–	20.0	μA
			V_{IN}/V_{OUT} = 3.6 ~ 5.5V		2.7 ~ 3.6	–	±20.0	
Increase in I_{CC} per Input		ΔI_{CC}	V_{IH} = V_{CC} - 0.6V		2.7 ~ 3.6	–	500	μA

AC Electrical Characteristics (Ta = -40 ~85°C)

Parameter	Symbol	Test Condition	V_{CC} (V)	Min.	Max.	Unit
Maximum Clock Frequency	t_{pLH} t_{pHL}	(Fig. 1, 2)	2.7 3.3 ±0.3	– 170	– –	ns
Propagation Delay Time (CK - Q)	t_{pLH} t_{pHL}	(Fig. 1, 2)	2.7 3.3 ±0.3	– 1.5	8.0 7.0	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig. 1, 3)	2.7 3.3 ±0.3	– 1.5	8.2 7.2	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig. 1, 3)	2.7 3.3 ±0.3	– 1.5	8.2 7.2	ns
Minimum Pulse Width (CK)	$t_w(H)$ $t_w(L)$	(Fig. 1, 2)	2.7 3.3 ±0.3	3.0 3.0	– –	ns
Minimum Setup Time	t_s	(Fig. 1, 2)	2.7 3.3 ±0.3	2.5 2.5	– –	ns
Minimum Hold Time	t_h	(Fig. 1, 2)	2.7 3.3 ±0.3	1.5 1.5	– –	ns
Output to Output Skew	t_{osLH} t_{osHL}	(*10)	2.7 3.3 ±0.3	– –	– 1.0	ns

(*10) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics (Ta = 25°C, Input $t_r = t_f$ = 2.5ns, C_L = 50pF, R_L = 500Ω)

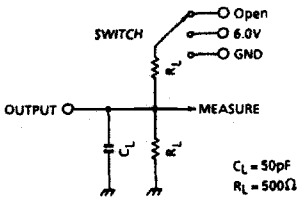
Parameter	Symbol	Test Condition	V_{CC} (V)	Typical	Unit
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Parameter	Symbol	Test Condition	V_{CC} (V)	Typical	Unit
Input Capacitance	C_{IN}	–	3.3	7	pF
Bus Input Capacitance	C_{OUT}		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (*11)	3.3	25	pF

(*11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC}/16 (per latch)

Fig.1 Test circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0V
t_{pHZ}, t_{pZH}	GND
t_W, t_S, t_h, t_{MAX}	Open

AC wave form

Fig.2 t_{pLH}, t_{pHL}, t_W, t_S, t_h

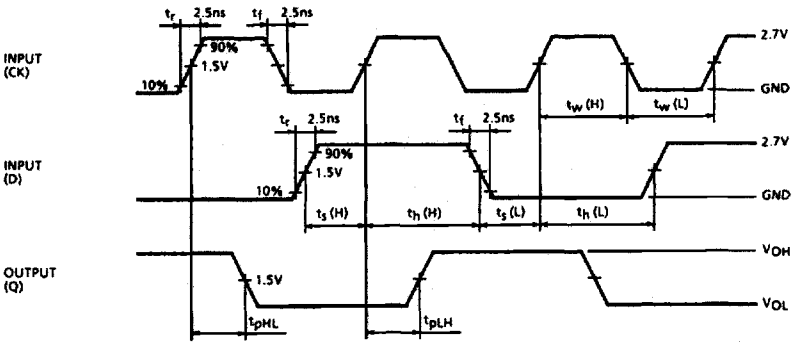
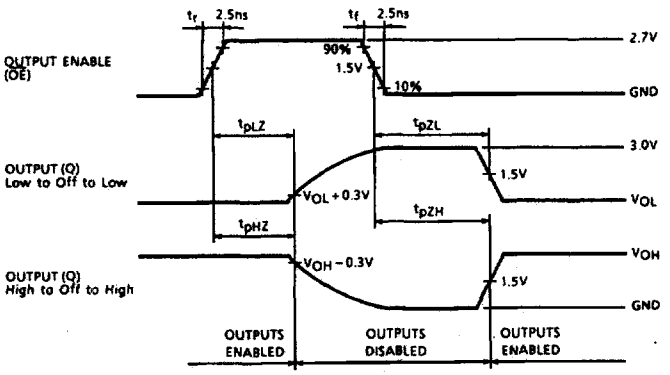


Fig.3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



1. This technical data may be controlled under U.S. Export Administration Regulations and may be subject to the approval of the U.S. Department of Commerce prior to export. Any export or re-export, directly or indirectly, in contravention of the U.S. Export Administration Regulations is strictly prohibited.
2. LIFE SUPPORT POLICY

   Toshiba products described in this document are not authorized for use as critical components in life support systems without the written consent of the appropriate officer of Toshiba America, Inc. Life support systems are either systems intended for surgical implant in the body or systems which sustain life.

   A critical component in any component of a life support system whose failure to perform may cause a malfunction of the life support system, or may affect its safety or effectiveness.
3. The information in this document has been carefully checked and is believed to be reliable; however no responsibility can be assumed for inaccuracies that may not have been caught. All information in this data book is subject to change without prior notice. Furthermore, Toshiba cannot assume responsibility for the use of any license under the patent rights of Toshiba or any third parties.