HI-REL DATA SHEET

HM 65779

8 k x 9
HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME : 35/45/55 ns**
- **LOW POWER CONSUMPTION**
  ACTIVE : 850 mW (max)
  STANDBY : 125 mW (max)
- **300 MILS WIDTH PACKAGE**
- **WIDE TEMPERATURE RANGE :**
  - 55° TO + 125°C
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

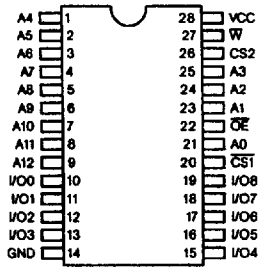
DESCRIPTION

The HM 65779 is a high speed CMOS static RAM organized as 8192 x 9 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 35 ns are available with maximum power consumption of only 850 mW.
The HM 65779 features fully static operation requiring no external clocks or timing strobes.The automatic power-down feature reduces the power consumption by 75 % when the circuit is deselected.
Easy memory expansion is provided by an active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65779 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65789 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

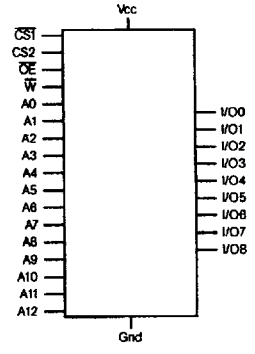
PACKAGES

Ceramic 300 mils, 28 pins, DIL.

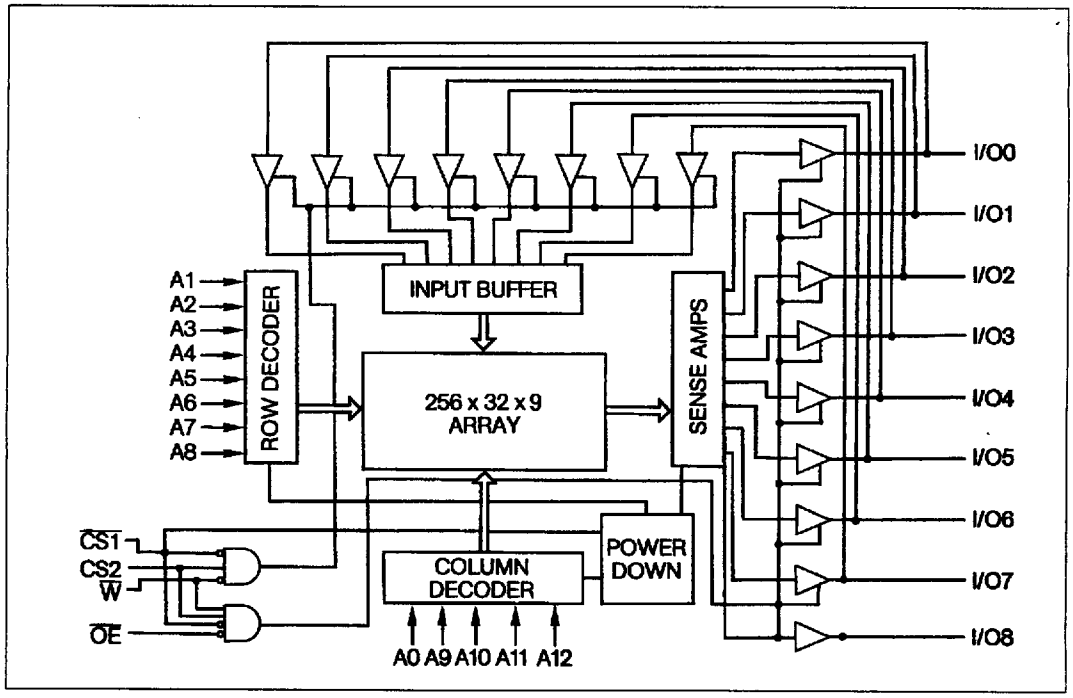
Pinout DIL 28 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A13 : Address inputs	$\overline{CS1}$: Chip Select 1
I/O0-I/O8 : Inputs/Outputs	CS2 : Chip Select 2
VCC : Power	$\overline{OE}$: Output enable
GND : Ground	$\overline{W}$: Write Enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect (power down)
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable
X	L	X	X	Z	Z	Deselect

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
DC input voltage : - 3.0 V to 7.0 V
DC output voltage in high Z state : - 0.5 V to + 7.0 V
Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2000 V
(MIL STD 883C method 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	5 V ± 10 %	- 55°C to + 125°C
Industrial	5 V ± 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS
DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65779 K	65779 M	65779 N	Unit	Value	Note 6
ICCSB (1)	Standby supply current	30	30	30	mA	Max	M
ICCOP (2)	Operating supply current	140	140	140	mA	Max	M
IIX (3)	Input leakage current	± 10	± 10	± 10	µA	Max	M
IOZ (3)	Output leakage current	± 10	± 10	± 10	µA	Max	M
VIL (4)	Input low voltage	0.8	0.8	0.8	V	Max	T
VIH (4)	Input low voltage	2.2	2.2	2.2	V	Min	T
VOL (5)	Output low voltage	0.4	0.4	0.4	V	Max	M
VOH (5)	Output high voltage	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	5	5	5	pF	Max	G
C OUT	Output capacitance	7	7	7	pF	Max	G

Notes : 1. $\overline{CS} \geq$ VIH, CS2 ≤ VIL a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB exceed values given.
2. Vcc max, Output current = 0 mA
3. Vcc max, Vin = Gnd to Vcc
4. VIL min = - 3.0V, VIH max = Vcc
5. Vcc min, IOL = 8 mA, IOH = - 4 mA
6. Including open/short test or inputs clamp voltage.
G - Guaranted - Not tested : Parameter measured at design validation and at any design change.
M - Measured : Parameter measured and data-log capability.
T - Tested : Parameter verification during testing.

AC TEST LOADS AND WAVEFORMS

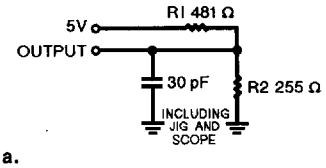


Fig.1a.

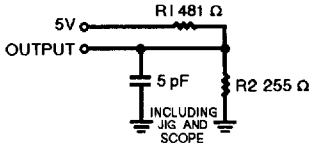
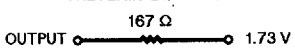


Fig.1b

Equivalent to : THEVENIN EQUIVALENT



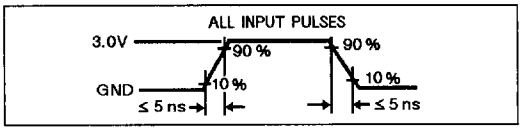


Fig.2 All input pulses

AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)

Conditions :

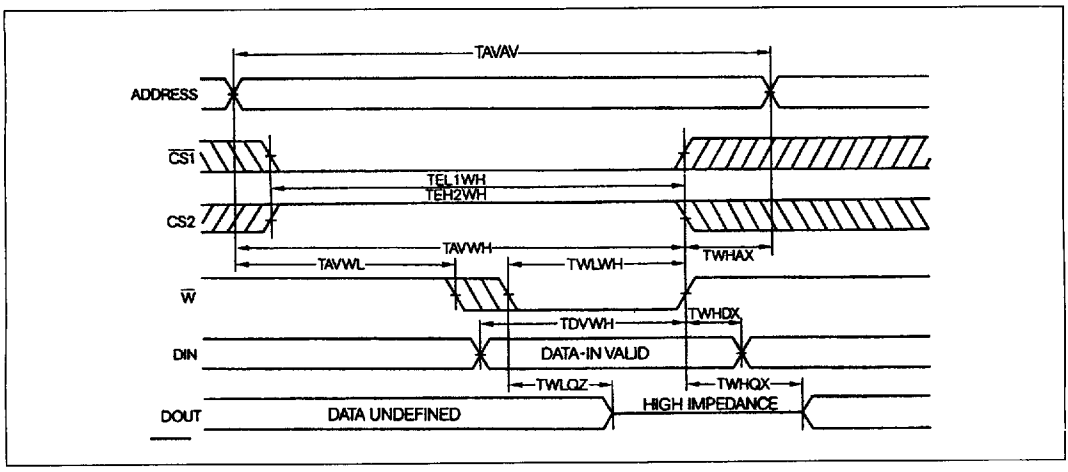
VCC	5V ± 10 %
Input pulse levels	Gnd to 3.0V
Input rise	5 ns
Input timing reference levels	1.5V
Output loading IOL / IOH	+ 30 pF
Operating temperature	- 55°C to + 125°C

WRITE CYCLE :

SYMBOL	PARAMETER (8)	65779 K	65779 M	65779 N	UNIT	VALUE
TAVAV	Write cycle time	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	30	40	50	ns	min
TDVWH	Data set-up time	20	25	30	ns	min
TEL1WH	$\overline{CS1}$ low to write end	30	40	50	ns	min
TEH2WH	CS2 high to write end	30	40	50	ns	min
TWLQZ (7)	Write low to high Z	15	20	25	ns	max
TWLWH	Write pulse width	25	30	35	ns	min
TWHAX	Address hold to end of write	5	5	5	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (7)	Write high to low Z	3	3	3	ns	min

Notes : 7. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. All parameters tested only.
All parameters are screened during full speed functional test.
For subgroups 7 and 8 (functional test).
Tested at 1 MHz with VIL = 0V and VIH = 3V.
HM 65779 is verified with differents patterns unit for basic function, latch-up, maximum rating, data-retention.

WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 9)



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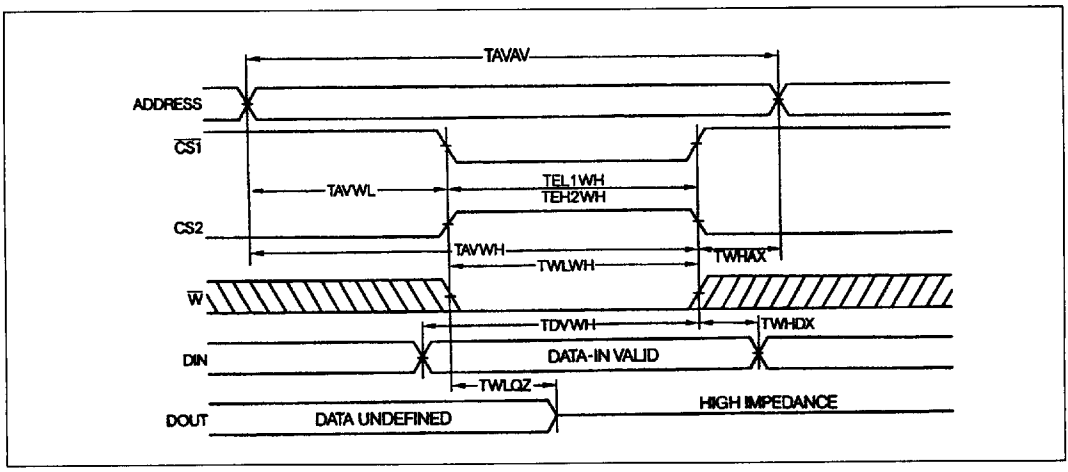
WRITE CYCLE 2 $\overline{CS1}$ CONTROLLED (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data-out will be high impedance if $\overline{OE}$ = VIH

READ CYCLE :

SYMBOL	PARAMETER (8)	65779 K	65779 M	65779 N	UNIT	VALUE
TAVAV	Read cycle time	35	45	55	ns	min
TAVQV	Address access time	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	35	45	55	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	ns	min
TEH2QX	CS2 high to low Z	5	5	5	ns	min
TEH1QZ (10)	$\overline{CS1}$ high to high Z	20	25	25	ns	max
TEL2QZ (10)	CS2 high to high Z	20	25	25	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	ns	min
TEH1ICCL	$\overline{CS1}$ high to power down	20	25	25	ns	max
TGLQV	Output enable access time	20	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	20	25	30	ns	max

Note : 10. TEHQZ and TWLQZ are specified with C1 = 5 pF. Transition is measured ± 500 mV from steady state voltage.

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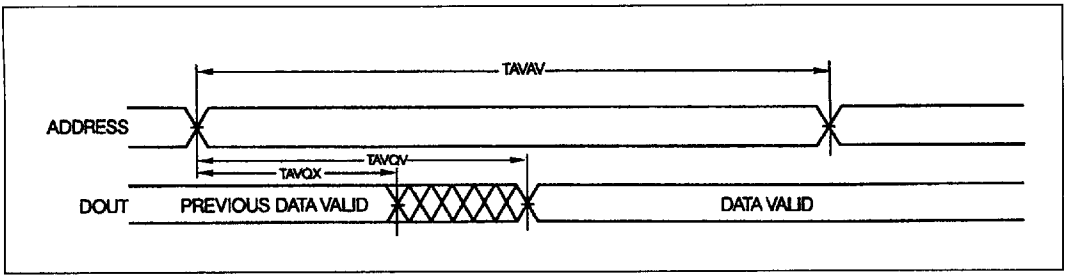
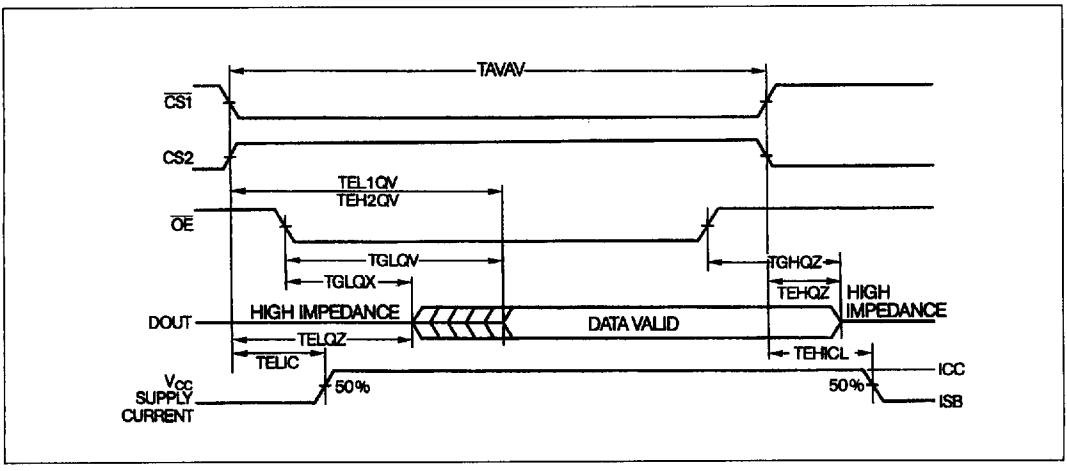
READ CYCLE nb 1 (notes 11,12)

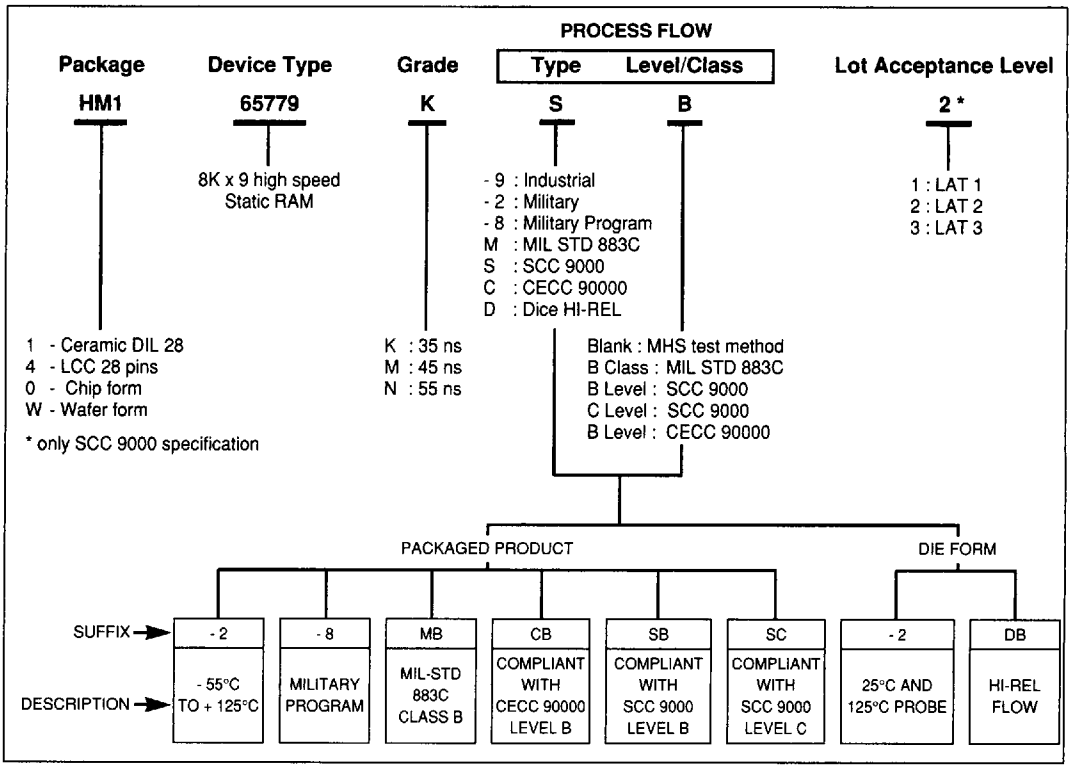


READ CYCLE nb 2 (notes 11, 13)

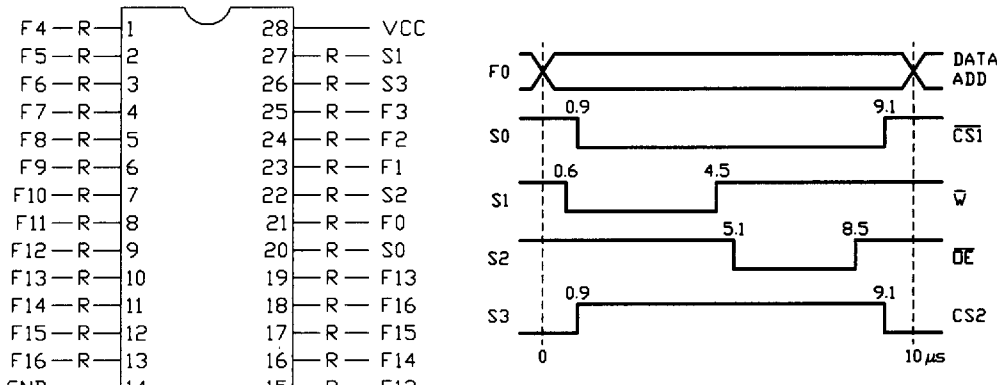


Notes : 11. $\overline{W}$ is high for read cycle.
12. Device is continuously selected, $\overline{CS1}/\overline{OE}$, = VIL, CS2 = VIH.
13. Address valid prior to or coincident with $\overline{CS}$ transitive low.

ORDERING INFORMATION



BURN IN SCHEMATICS

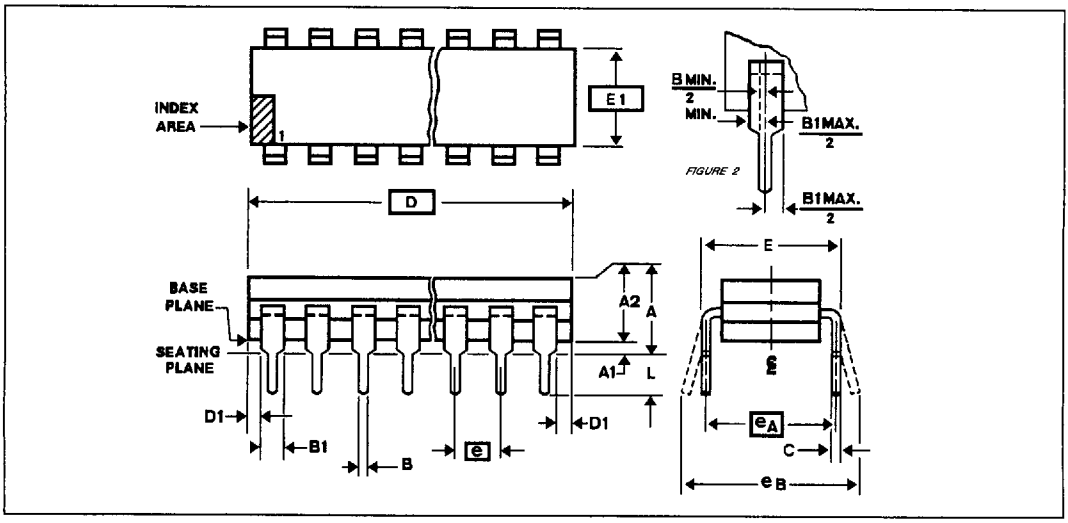


VCC = +5 V (– 0, + 0.5)
R = 1KΩ per pin

F0 = 50 KHz ± 20 %
Fn = 1/2 Fn-1

S0 to S3 : programmable signals for write / read cycles

PACKAGE OUTLINES



28 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	—	0.38	2.92	0.36	1.14	0.20	36.58	0.13	7.62	6.10	2.54	7.62	—	3.05
	MAX	5.84	—	4.95	0.58	1.78	0.38	37.50	—	8.25	7.87	BSC	BSC	11.43	5.08
INCHES	MIN	—	.015	.115	.014	.045	.008	1.440	.005	.300	.240	.100	.300	—	.125
	MAX	.230	—	.195	.023	.070	.015	1.476	—	.325	.310	BSC	BSC	.450	.200

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