CD54HC4538/3A
CD54HCT4538/3A

Switching Speed (Limits with black dots (•) are tested 100%.)
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{cc} V	25°C				−55°C to +125°C				UNITS
			HC		HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay A, $\overline{B}$ to Q	t_{PLH}	2	—	250	—	—	—	375	—	—	
		4.5	—	50•	—	55•	—	75•	—	83•	
		6	—	43	—	—	—	64	—	—	
A, $\overline{B}$ to $\overline{Q}$	t_{PHL}	2	—	250	—	—	—	375	—	—	
		4.5	—	50•	—	55•	—	75•	—	83•	
		6	—	43	—	—	—	64	—	—	
$\overline{R}$ to Q		2	—	250	—	—	—	375	—	—	ns
		4.5	—	50•	—	40•	—	75•	—	60•	
		6	—	43	—	—	—	64	—	—	
$\overline{R}$ to $\overline{Q}$	t_{PLH}	2	—	250	—	—	—	375	—	—	
		4.5	—	50•	—	50•	—	75•	—	75•	
		6	—	43	—	—	—	64	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Output Pulse Width R_x = 10 Ω, C_x = 0.1 μF	τ	3	0.64	0.78	—	—	0.605	0.819	—	—	ms
		5	0.63•	0.77•	0.63•	0.77•	0.595•	0.805•	0.595•	0.805•	
Output Pulse Width Match, Same Pkg.			Type ± 1%								
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{cc} (6V)	OPEN	GROUND	V_{cc} (6V)
CD54HC/HCT4538	1,2,6,7,9, 10,14,15	3-5,8,11-13	16	1,2,6,7,9, 10,14,15	8	3-5,11-13,16

Dynamic	OPEN	GROUND	1/2 V_{cc} (3V)	V_{cc} (6V)	OSCILLATOR	
					50 kHz	25 kHz
CD54HC/HCT4538	—	1,4,8,12,15	6,7,9,10	2,14,16	5,11	3,13

NOTE: Each pin except V_{cc} and Gnd will have a resistor of 2k-47k ohms.

BCD-to-7-Segment Latch/Decoder/Driver for LCDs

CD54HC4543/3A
CD54HCT4543/3A

The RCA CD54HC4543 and CD54HCT4543 high-speed silicon-gate devices are BCD-to-7-segment latch/decoder/drivers designed primarily for directly driving liquid-crystal displays. They have an active-high disable input (LD), an active-high blanking input (BI) and a phase input (PH) to which a square wave is applied for liquid-crystal applications. This square wave is also applied to the backplane of the liquid-crystal display.

These devices can also be used, in conjunction with current amplifying devices, for driving LEDs, incandescent, fluorescent, and gas-discharge displays. For these applications, the phase input provides a means for obtaining active-high or active-low segment outputs.

CD54HC4543/3A
CD54HCT4543/3A

FUNCTIONAL DIAGRAM

Package Specifications
See Section 11, Fig. 11
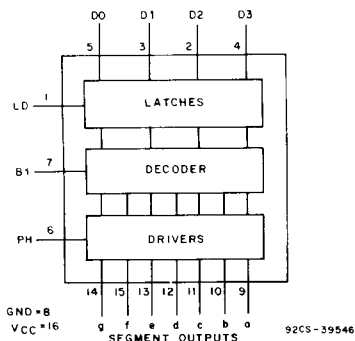
HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
D0, D1, D2	1
D3, BI	0.5
PH	1.25
LD	1.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

Static Electrical Characteristics (Limits with black dots (•) are tested 100%

		TEST CONDITIONS		
		\multicolumn{4}{c}{HC/HCT}	\multicolumn{2}{c}{V_{IN}}	\multicolumn{2}{c}{LIMITS}	
						HC	HCT			
CHARACTERISTICS		V_{DD}	V_O	I_O	V_{CC} or GND	V_{IL} or V_{IH}	V_{IL} or V_{IH}	MIN.	MAX.	UNITS
Quiescent	25°C	6	—	—	6, 0	—	—	—	8•	
Device Current	−55°C	6	—	—	6, 0	—	—	—	160•	μA
I_{CC}	+125°C									

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

Switching Speed (Limits with black dots (•) are tested 100%.)
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{CC} V	\multicolumn{8}{c}{LIMITS}	UNITS
			\multicolumn{4}{c}{25°C}	\multicolumn{4}{c}{−55°C to +125°C}	
			\multicolumn{2}{c}{HC}	\multicolumn{2}{c}{HCT}	\multicolumn{2}{c}{54HC}	\multicolumn{2}{c}{54HCT}	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay		2	—	340	—	—	—	510	—	—	
D_n to Output		4.5	—	68•	—	80•	—	102•	—	120•	
		6	—	58	—	—	—	87	—	—	
LD to Output		2	—	370	—	—	—	555	—	—	
		4.5	—	74•	—	77•	—	111•	—	116•	
	t_{PLH}	6	—	63	—	—	—	94	—	—	
BI to Output	t_{PHL}	2	—	265	—	—	—	400	—	—	ns
		4.5	—	53•	—	66•	—	80•	—	99•	
		6	—	45	—	—	—	68	—	—	
PH to Output		2	—	200	—	—	—	300	—	—	
		4.5	—	40	—	66	—	60	—	99	
		6	—	34	—	—	—	51	—	—	
Transition Time	t_{TLH}	2	—	250	—	—	—	375	—	—	
	t_{THL}	4.5	—	50	—	50	—	75	—	75	
		6	—	43	—	—	—	64	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

CD54HC4543/3A
CD54HCT4543/3A

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT4543	9-15	1-8	16	9-15	8	1-7,16
Dynamic					OSCILLATOR	
	OPEN	GROUND	1/2 V_{CC} (3V)	V_{CC} (6V)	50 kHz	25 kHz
CD54HC/HCT4543	—	6-8	9-15	1,4,16	2,3,5	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54HC7038/3A
CD54HCT7038/3A

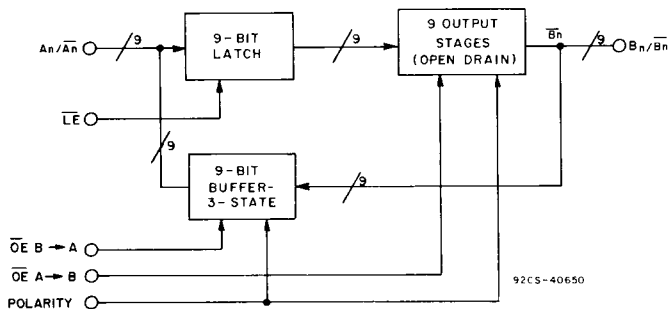# 9-Bit Bus Transceiver With Latch

The RCA CD54HC7038 and the CD54HCT7038 are high-speed CMOS 9-bit bidirectional transceivers with input data latch and data polarity selection capability. These data-bus interface products are intended for two-way asynchronous communications between data buses. The 48-mA output sink current meets the drive requirements for the SCSI/Q-02, multibus, and VME bus specifications. The HC/HCT7038 devices feature the low power consumption of standard CMOS circuits and the speed and drive capabilities of LSTTL and TTL circuits.

The CD54HC7038 and CD54HCT7038 allow transmission and internal latch storage of 9 bits of positive or negative logic data from the "A" bus to the "B" bus. A low level on the Latch Enable input ($\overline{LE}$) stores "A" bus data in a 9-bit latch. When $\overline{LE}$ is a high level, the latch is transparent and

data flows from "A" to "B". The "B" bus output data drivers are open-drain N-MOS transistors that allow the "B" bus high logic state level to be set by the B bus termination network which may be the SCSI/Q-02 (220/330 ohm) or multibus/VME (dual 330/470 ohm) terminations. B-bus data may be transferred to the A-bus via appropriate $\overline{OE}$ control levels.

Data polarity may be reversed in either direction.

For the HC types, A-bus ports and control are compatible with CMOS logic levels. For the HCT types, the A-bus ports and control are compatible with CMOS or TTL logic levels. For both types, the B-bus ports are compatible with only TTL levels; the TTL high-logic-level must be set by the external bus termination network.

FUNCTIONAL DIAGRAM

Package Specifications
See Section 11, Fig. 15