UMC

UM6264D Series

PRELIMINARY

8K X 8 CMOS SRAM

Features

- Single +5V power supply
- Access times: 55/70 ns (max.)
- Current:
  - Low power version: Operating: 70mA (max.)
    Standby: 100 μA (max.)
  - Very low power version: Operating: 70mA (max.)
    Standby: 25 μA (max.)
- Directly TTL compatible: All inputs and outputs
- Full static operation, no clock or refreshing required
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2V (min.)
- Available in 28-pin DIP, SKINNY DIP, SOP or TSOP packages

General Description

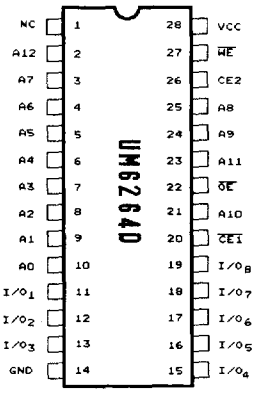
The UM6264D is a low operating current 65,536-bit static random access memory organized as 8,192 words by 8 bits and operates on a single 5V power supply. It is built using UMC's high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip enable inputs are provided for power down and device enable, and an output enable input is included for easy interface.

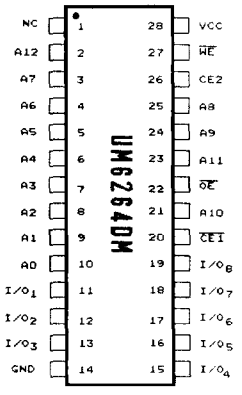
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configurations

■ DIP

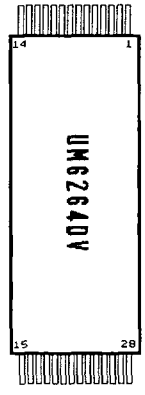


■ SOP

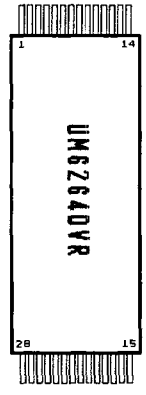


■ TSOP

(forward type)

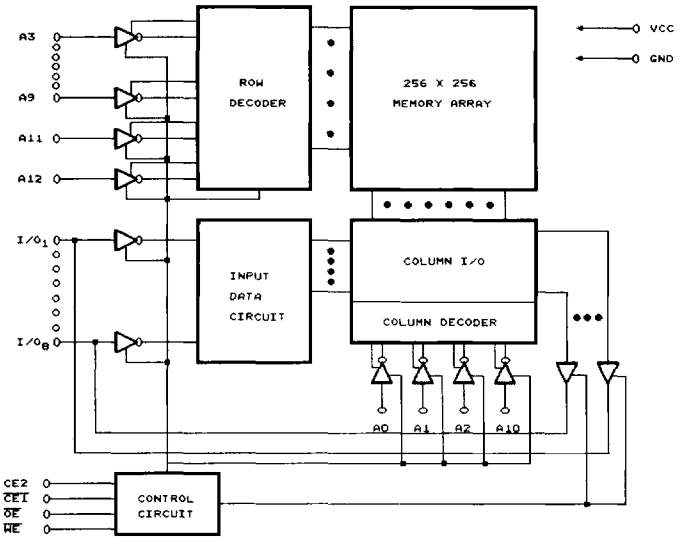


(reverse type)



Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Pin Name	$\overline{OE}$	A11	A9	A8	CE2	$\overline{WE}$	VCC	NC	A12	A7	A6	A5	A4	A3
Pin No.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Pin Name	A2	A1	A0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A10

Block Diagram



Pin Descriptions — DIP/SOP

Pin No.	Symbol	Description
1	NC	No Connection
2-10, 21, 23-25	A0 - A12	Address Input
27	$\overline{WE}$	Write Enable
22	$\overline{OE}$	Output Enable
20	$\overline{CE1}$	Chip Enable
26	CE2	Chip Enable
11-13, 15-19	I/O1 - I/O8	Data Input/Output
28	VCC	Power Supply
14	GND	Ground

Pin Description — TSOP

Pin No.	Symbol	Description
1	$\overline{OE}$	Output Enable
2-4, 9-17, 28	A0 - A12	Address Input
5	CE2	Chip Enable
6	$\overline{WE}$	Write Enable
8	NC	No Connection
18-20, 22-26	I/O1 - I/O8	Data Input/Output
27	$\overline{CE1}$	Chip Enable
7	VCC	Power Supply
21	GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	0	+0.8	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +7.0V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Temperature Under Bias, Tbias . . . . . -10°C to +85°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260 °C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM6264D-55L/70L		UM6264D-55LL/70LL		Unit	Conditions
		Min.	Max.	Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	–	1	–	1	μA	V_{IN} = GND to VCC
$\|I_{LO}\|$	Output Leakage Current	–	1	–	1	μA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $I_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	–	15	–	15	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA

DC Electrical Characteristics (continued)

Symbol	Parameter	UM6264D-55L/70L		UM6264D-55LL/70LL		Unit	Conditions
		Min.	Max.	Min.	Max.		
I_{CC1}	Dynamic Operating Current	–	70	–	70	mA	Min. Cycle, Duty = 100% $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA
I_{CC2}		–	15	–	15	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IH} = VCC, V_{IL} = 0V, f = 1 MHz, $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	–	3	–	2	mA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}
I_{SB1}		–	100	–	25	μA	$\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≥ VCC - 0.2V V_{IN} ≥ 0V
I_{SB2}		–	100	–	25	μA	CE2 ≤ 0.2V V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	–	0.4	–	0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4	–	2.4	–	V	I_{OH} = -1.0 mA

Truth Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disable	L	H	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X: H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, VCC = 5V ± 10%)

Symbol	Parameter		UM6264D-55L/55LL		UM6264D-70L/70LL		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{RC}	Read Cycle Time		55	–	70	–	ns
t_{AA}	Address Access Time		–	55	–	70	ns
t_{ACE1}	Chip Enable Access Time	$\overline{CE1}$	–	55	–	70	ns
t_{ACE2}		CE2	–	55	–	70	ns
t_{OE}	Output Enable to Output Valid		–	30	–	35	ns
t_{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE1}$	10	–	10	–	ns
t_{CLZ2}		CE2	10	–	10	–	ns
t_{OLZ}	Output Enable to Output in Low Z		5	–	5	–	ns
t_{CHZ1}	Chip Disable to Output in High Z	$\overline{CE1}$	0	20	0	25	ns
t_{CHZ2}		CE2	0	20	0	25	ns
t_{OHZ}	Output Disable to Output in High Z		0	20	0	25	ns
t_{OH}	Output Hold from Address Change		5	–	5	–	ns

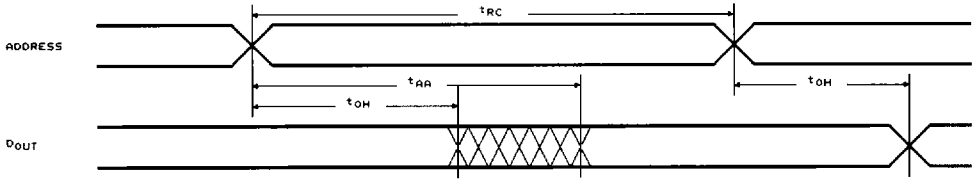
AC Characteristics (continued)

Symbol	Parameter	UM6264D-55L/55LL		UM6264D-70L/70LL		Unit
		Min.	Max.	Min.	Max.	
Write Cycle						
t_{WC}	Write Cycle Time	55	–	70	–	ns
t_{CW}	Chip Enable to End of Write	50	–	60	–	ns
t_{AS}	Address Setup Time	0	–	0	–	ns
t_{AW}	Address Valid to End of Write	50	–	60	–	ns
t_{WP}	Write Pulse Width	40	–	50	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z	0	25	0	20	ns
t_{DW}	Data to Write Time Overlap	25	–	30	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	ns
t_{OW}	Output Active from End of Write	0	–	5	–	ns

Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

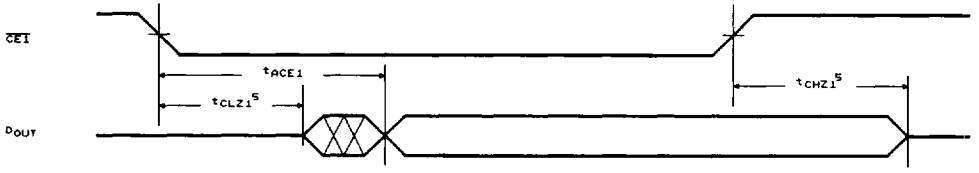
Timing Waveforms

Read Cycle 1 (1, 2, 4)



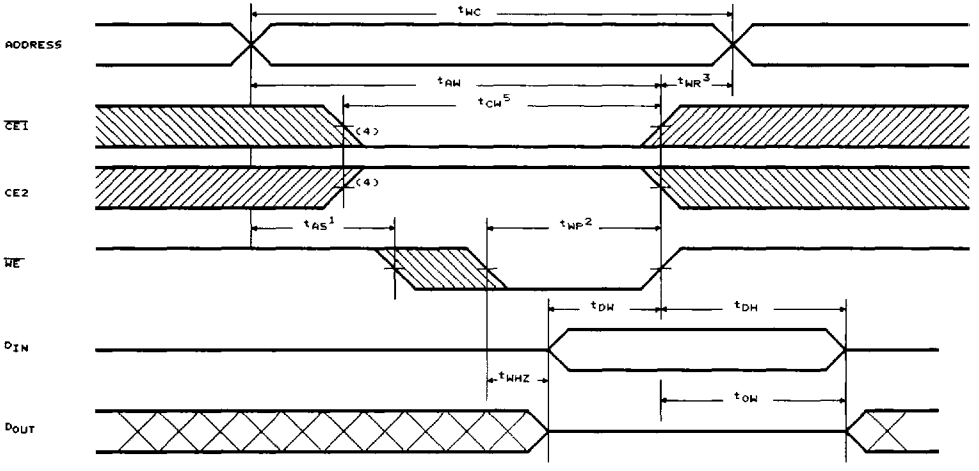
Timing Waveforms (continued)

Read Cycle 2 (1, 3, 4, 6)



Read Cycle 3 (1, 4, 7, 8)

Read Cycle 4 (1)



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled, $\overline{CE1}$ = V_{IL} and CE2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2

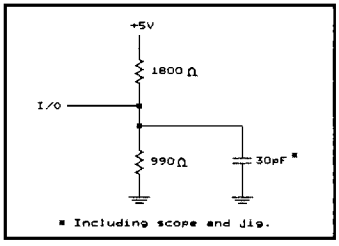


Figure 1. Output Load

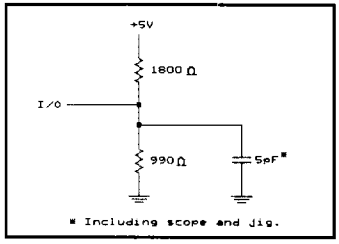


Figure 2. Output Load for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{WHZ}, and t_{OW}

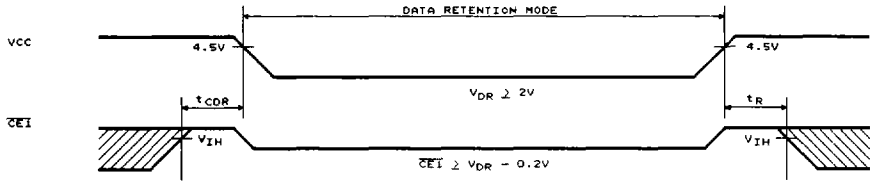
Data Retention Characteristics (TA = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention		2.0	5.5	V	$\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≥ VCC - 0.2V or CE2 ≤ 0.2V
V_{DR2}			2.0	5.5	V	CE2 ≤ 0.2V
I_{CCDR1}	Data Retention Current	L-Version	–	50*	µA	VCC = 3.0V, $\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≥ VCC - 0.2V, V_{IN} ≥ 0V
		LL-Version	–	10**		
I_{CCDR2}		L-Version	–	50*	µA	VCC = 3.0V, CE2 ≤ 0.2V V_{IN} ≥ 0V
		LL-Version	–	10**		
t_{CDR}	Chip Disable to Data Retention Time		0	–	ns	See Retention Waveform
t_R	Operation Recovery Time		5	–	ms	

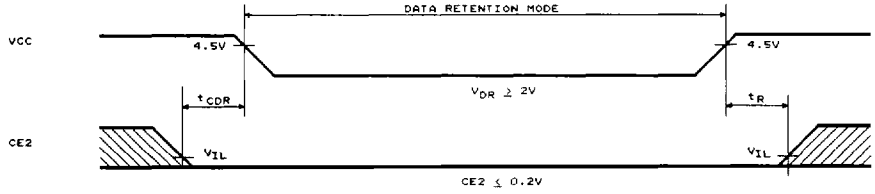
** UM6264D-55LL/70LL I_{CCDR}: Max. 3 µA at T_A = 0°C to +40°C

* UM6264D-55L/70L I_{CCDR}: Max. 20 µA at T_A = 0°C to +40°C

Low VCC Data Retention Waveform ($\overline{CE1}$ Controller)

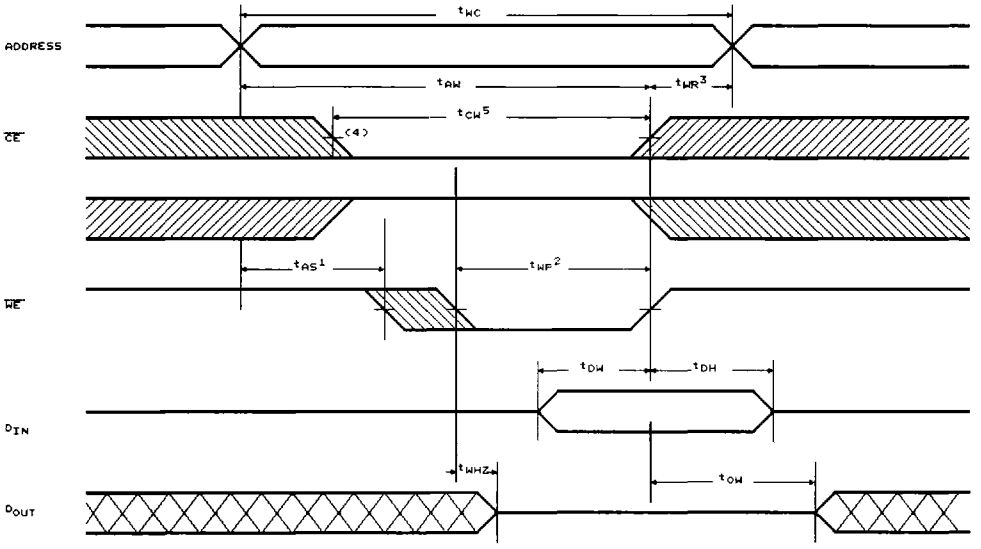


Low VCC Data Retention Waveform (CE2 Controller)



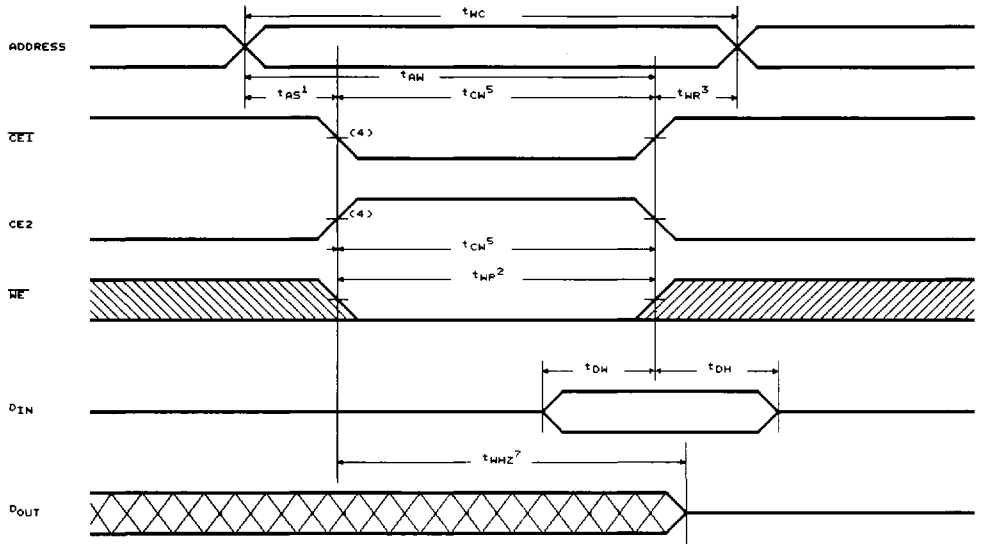
Timing Waveforms (continued)

Read Cycle 1 [6]
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2 [6]
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE1}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ level is high or low.
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (μA)	Package
UM6264D-55L	55	70	100	28L DIP
UM6264D-55LL		70	25	28L DIP
UM6264DM-55L		70	100	28L SOP
UM6264DM-55LL		70	25	28L SOP
UM6264DK-55L		70	100	28L SKINNY
UM6264DK-55LL		70	25	28L SKINNY
UM6264DV-55L		70	100	28L TSOP
UM6264DV-55LL		70	25	28L TSOP
UM6264DVR-55L		70	100	28L TSOP
UM6264DVR-55LL		70	25	28L TSOP
UM6264D-70L	70	70	100	28L DIP
UM6264D-70LL		70	25	28L DIP
UM6264DM-70L		70	100	28L SOP
UM6264DM-70LL		70	25	28L SOP
UM6264DK-70L		70	100	28L SKINNY
UM6264DK-70LL		70	25	28L SKINNY
UM6264DV-70L		70	100	28L TSOP
UM6264DV-70LL		70	25	28L TSOP
UM6264DVR-70L		70	100	28L TSOP
UM6264DVR-70LL		70	25	28L TSOP