ADVANCE INFORMATION

Based on Evaluation of Limited Number of Devices
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MAXIM

Ultra High-Precision CMOS Op Amps

General Description

The MAX425/MAX426 precision CMOS amplifiers provide input offset and noise specifications superior to chopper-stabilized amplifiers while using no external capacitors. Two independent error-correction schemes operate on-chip: A unique input switching design reduces input offset voltage (V_{OS}) to 0.5µV, while offsets inside the amplifier are removed with digital correction to reduce common-mode errors and minimize clock ripple. The MAX425 is unity-gain stable with a 350kHz gain-bandwidth product. The MAX426 has a 15MHz gain-bandwidth product, and is stable for closed-loop gains of 30dB (30V/V) or greater.

The error-correction design of the MAX425/MAX426 is completely different from chopper-stabilized amplifiers. Ultra-low V_{OS} is achieved with negligible clock noise, fast overload recovery, improved high-frequency performance, and reduced 1/f noise. 1Hz bandwidth noise is typically $100nV_{p-p}$. The amplifiers are ideal for precision measurement applications where large, accurate gains and low noise are required. The MAX426 is also ideal when wide bandwidth is required.

Signal input and power-supply connections conform to the standard op amp pin configuration. Both devices operate from ±2.5V to ±7.5V or from single supplies ranging from +5V to +15V. They are offered in 8-pin DIP and 16-pin wide SO packages.

Applications

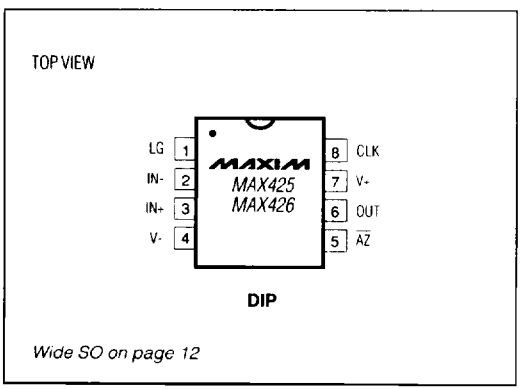
Low-Noise DC Amplifier

Weigh Scales

Thermocouple Amplifiers

Strain-Gauge Vibration Analysis

Pin Configurations



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Features

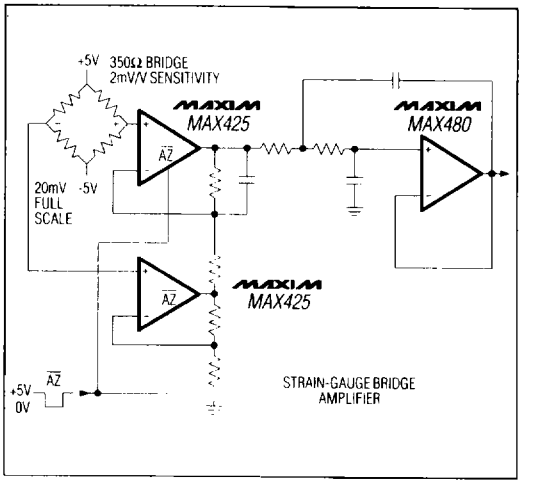
- **250nV$_{p-p}$ Noise (0.1Hz to 10Hz BW)**
- **0.5µV Typ V_{OS}**
- **0.01µV/°C Typ Offset Drift**
- **No External Components**
- **Controllable Auto-Zero**
- **190dB Open-Loop Gain**
- **15MHz Gain Bandwidth (MAX426)**
- **Unity-Gain Stable (MAX425)**
- **Rail-to-Rail Output Swing**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX425C/D	0°C to +70°C	Dice*
MAX425EPA	-40°C to +85°C	8 Plastic DIP
MAX425EWE	-40°C to +85°C	16 Wide SO
MAX425MJA	-55°C to +125°C	8 CERDIP
MAX426C/D	0°C to +70°C	Dice*
MAX426EPA	-40°C to +85°C	8 Plastic DIP
MAX426EWE	-40°C to +85°C	16 Wide SO
MAX426MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Typical Operating Circuit



Ultra High-Precision CMOS Op Amps

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) ..... +18V
Input Voltage Range ..... (V+ +0.3) to (V- -0.3) V
Duration of Output Short Circuit ..... Indefinite
Current into Any Pin (except pins 2 and 3) 50mA
Current into Pins 2 and 3 ..... 10mA
Continuous Total Power Dissipation (any package) ... 300mW

Operating Temperature Ranges:
MAX42 _ EPA/EWE ..... -40°C to +85°C
MAX42 _ MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec.) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V; T_A = T_{MIN} to T_{MAX}; LG = 0V; Auto-Zero activated after power-up, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 1, 2)	V_{OS}	T_A = +25°C	After auto-zero, CLK off		0.5	5	µV
			Before auto-zero, CLK off		50	500	
Offset Tempco (Note 3)	$\Delta V_{OS}/\Delta T$	After auto-zero, CLK off			0.005	0.05	µV/°C
		No auto-zero, CLK on			0.01	0.05	
Offset Tempco	$\Delta V_{OS}/\Delta T$	Auto-zero off, CLK off			0.5	10	µV/°C
Input Bias Current CLK Off (Note 4)	I_B	At IN+ and IN-, CLK off	T_A = +25°C		0.2	10	pA
			T_A = +85°C		5	100	
			T_A = +125°C		0.15	5	nA
Input Bias Current (Charge Injection) CLK On (Note 4)	I_B	At IN+ and IN-, CLK on	Internal CLK		120	200	pA
			External CLK		0.4		pA/Hz
Large Signal Gain	A_{VOL}	R_L = 10kΩ		140	190		dB
Output Voltage Swing		R_L = 2kΩ		±3.5	±4.4		V
		R_L = 10kΩ		±4.7	±4.9		
Common-Mode Voltage Range	CMVR	V+ = +5V	V- = -5V	+3/-4			V
			V- = 0V		+3/+1		
Common-Mode Rejection Ratio (Note 1)	CMRR	CMVR = -4V to +3V	With auto-zero at CMV	120	150		dB
			Internal CLK, auto-zero off		130		
			Auto-zero off, CLK off	70	85		
Power-Supply Rejection Ratio (Note 1)	PSRR	V_{SUP} = ±4.5V to ±5.5V	Auto-zero at both limits	120	150		dB
			Auto-zero off, CLK off	80	95		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +5V, V- = -5V; T_A = T_{MIN} to T_{MAX}; LG = 0V; Auto-Zero activated after power-up, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Noise Voltage	e_N	T_A = +25°C, R_S = 100Ω, Internal CLK	In 0.1Hz to 1Hz BW		0.1		μV_{p-p}
			In 0.1Hz to 10Hz BW		0.25		
		T_A = +25°C; R_S = 100Ω; CLK off	In 0.1Hz to 10Hz BW		1.5		μV_{p-p}
			In 1kHz to 100kHz BW, Figure 10		2.5		μV_{RMS}
Gain-Bandwidth Product	GBWP	T_A = +25°C	MAX425	0.25	0.35		MHz
			MAX426	8	15		
Slew Rate	SR	T_A = +25°C	MAX425	0.25	0.4		V/µs
			MAX426	8	12		
Operating Supply Range				4.75		15.75	V
Supply Current	I_{SUP}	No load after auto-zero			1.2	1.4	mA
Short-Circuit Current	I_{SC}	T_A = +25°C, V_{OUT} = 0V		5	9	15	mA
Switching-Clock Frequency	f_C	T_A = +25°C; CLK pin open		200	300	450	Hz
CLK Input Current	I_{CLK}	External clock operation	V_{CLK} = V+		6	20	µA
			V_{CLK} = 0V		-35	-100	
$\overline{AZ}$ Input Logic Levels		LG = 0V, High level		2			V
		LG = 0V, Low level				0.8	
$\overline{AZ}$ Input Current					0.1	10	µA
LG Input Current					5	20	µA
$\overline{AZ}$ Input Pulse Width				10			µs
$\overline{AZ}$ Input Transition Time						0.25	µs
Auto-Zero Duration		MAX425			125	200	ms
		MAX426			31	50	

Note 1: V_{OS}, CMRR, and PSRR errors are all corrected during auto-zero operation.

Note 2: With CLK on and following an auto-zero cycle, the input offset voltage consists of a square wave with a typical amplitude of 1µV_{p-p}.

Note 3: Specification is guaranteed by design and correlates with internal amplifier parameters. Thermocouple effects inherent in high-speed automatic test systems prevent measurement of these levels in a production environment.

Note 4: Input bias current is largely a leakage term and doubles every 8°C. Total input current also includes charge injection when internal CLK is operating, or if CLK is driven from an external source. See Input Bias Current with CLK on (Charge Injection) specification.

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Pin Description

8-PIN DIP	16-PIN SO	NAME	FUNCTION
1	1	LG	Auto-Zero Logic Ground - usually 0V.
-	2, 3, 6, 7, 11, 14 15	N.C	No Connect
2	4	IN-	Inverting Op Amp Input
3	5	IN+	Noninverting Op Amp Input
4	8	V-	Negative Power Supply
-	9	AZ STAT	Auto-Zero Status Output open-drain p-channel FET. Pulled to V+ during auto-zero cycle FET on resistance is typically 500Ω
5	10	$\overline{AZ}$	Auto-Zero Control Input: Pulse low to start auto-zero cycle. Connect to V+ to turn off Connect with LG to 0V to activate auto-zero cycles at 1 minute intervals.
6	12	OUT	Amplifier Signal Output
7	13	V+	Positive Power Supply
8	16	CLK	Clock Input. Leave open for 300Hz switching clock, connect to V+ to disable, or drive from clock source. With CLK pin open, CLK signal is 128 times faster than the input switch frequency.

Detailed Description

Auto-Correction Circuitry

The MAX425/MAX426 unique precision amplifier design employs two independent error-correction schemes A switching input amplifier eliminates V_{OS} and minimizes 1/f noise, and digital auto-zeroing corrects all internal amplifier stage offsets to remove common-mode errors and clock ripple. Figure 1 shows a block diagram of the basic architecture. The amplifier can be set to use both, one, or none of these correction techniques. Table 1 outlines the op amp's characteristics with various auto-correction combinations.

"Switching" Op Amp

A 300Hz internal switching clock switches the inputs. Internal errors that vary slowly compared to 300Hz, such as thermal drift, input offset, low-frequency noise, power-supply sensitivities, and common-mode errors, are all dramatically reduced. Since low-frequency noise looks

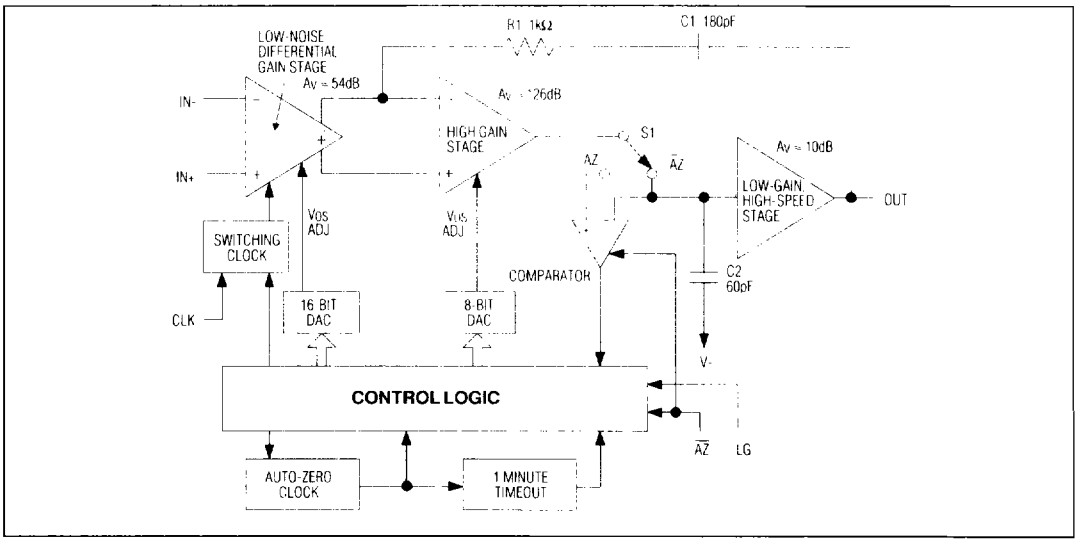

Figure 1. Block Diagram of MAX425 Op Amp

like a slowly varying offset signal, 1/f noise (about 300nV/√Hz at 1Hz before switching) is removed the same way as offset. The main noise contribution is from wideband noise at the input switching frequency, which is demodulated and appears as low-frequency noise at the output. In this case, the noise density at 300Hz is typically 17nV/√Hz. Wideband noise (1kHz to 100kHz) is typically 2.5μVRMS. This corresponds to a noise voltage density of 8nV/√Hz.

In a switching amplifier, the inputs and outputs of the differential input stage are periodically swapped. Figure 2 shows this type of amplifier configured with a closed-loop gain of 100. The example assumes a 1mV offset (mismatch) between P1 and P2. Figure 2A's circuit generates an output signal of 100(VIN - 1mV), or 100VIN - 100mV. When the inputs and outputs of P1 and P2 are interchanged, the output signal becomes 100VIN + 100mV. Note: The offset error, but not the input signal, has changed polarity. Therefore, by switching back and forth with a 50% duty cycle, the output averages to 100VIN while the offset error averages to zero. The output then consists of the desired signal with a small superimposed square wave whose amplitude is the internal offset voltage. The square-wave amplitude is negligibly small because digital auto-zeroing reduces the internal offset to less than 1μV.

Digital Auto-Zero

In addition to switched inputs, the MAX425/MAX426 also employ digital auto-zeroing circuitry. In conventional auto-zero schemes, capacitors store offset correction signals, but require frequent updating because leakage currents soon drain this information from the capacitors. The MAX425/MAX426 eliminate this problem by storing the corrections digitally. A 16-bit DAC, with 0.1μV resolution, supplies the actual error-correction voltage that cancels the amplifier's internal first-stage offset voltage. An 8-bit DAC performs a similar task in the second amplifier stage.

An auto-zero cycle can be initiated manually or at approximately 1 minute intervals by an internal clock. An auto-zero cycle lasts approximately 125ms for the MAX425 and 31ms for the MAX426. During this time, the $\overline{AZ}$ input is ignored, and the amplifier output remains fixed near the output level it had just prior to auto-zero. The amplifier returns to normal operation when the cycle ends.

Digital correction reduces the need for auto-zeroing. Hours can pass between auto-zero cycles without loss of DC accuracy. The only detrimental effect is slight changes in clock ripple as internal (but not input) offsets drift without correction. VOS is still kept within specified limits by the input switching circuitry. In practice, the amplifier is typically auto-zeroed during other system calibration routines while the signal path is inactive.

Table 1. Auto-Correction Characteristics

$\overline{AZ}$	CLK	Correction Mode	Characteristics
⌐_⌐	OPEN	Input Switching On, Manual Auto-Zero	VOS = 0.5μV typ. Inputs switch at 300Hz or at external clock rate. One auto-zero cycle follows $\overline{AZ}$ going low. Auto-zero disables amplifier for 125ms (31ms - MAX426). Clock ripple drops to 1μVp-p after auto-zero. Frequent auto-zero NOT required for 1μV VOS.
0V	OPEN	Input Switching On, Internal Auto-Zero	VOS = 0.5μV typ. Inputs switch at 300Hz or at external clock rate. Auto-zero cycles occur at approximately 1 minute intervals. Auto-zero disables amplifier for 125ms (31ms - MAX426).
⌐_⌐	V+	Input Switching Off, Manual Auto-Zero	VOS = 0.5μV typ. Input switching disabled. No clock ripple (clock off) VOS nulled after auto-zero cycle. Auto-zero disables amplifier for 125ms (31ms - MAX426). Required auto-zero rate depends on thermal environment.
V+	V+	Input Switching Off, Auto-Zero Off	VOS < 500μV max, 50μV typ. Auto-zero disabled Input switching disabled. No clock ripple (clock off). Lowest input bias current (0.2pA typ. at +25°C.) Works as an uncorrected CMOS op amp.

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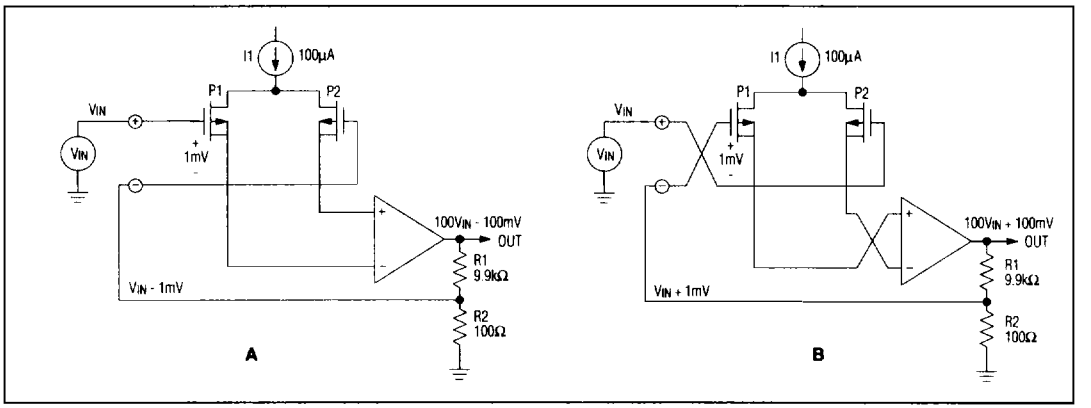

Figure 2. Switching-Amplifier Operation. In Figure A, offset voltage appears as -100mV at the output of the amplifier; in Figure B, it is +100mV. If the duty cycle of each state is 50%, the offset voltage at the output averages zero.

Only the internal DAC resolution and the inherent amplifier noise limit the repeatability of the digital auto-zero circuitry. Consequently, successive auto-zero cycles are repeatable to within 0.1µVRMS.

Overload Recovery

Since digital offset nulling also allows corrections to be stored digitally and not on capacitors, the MAX425/MAX426 recover almost immediately from an overload condition. The MAX425/MAX426 typically recover from overload in less than 10µs, compared to tens of milliseconds for most chopper-stabilized amplifiers. Figure 3 plots the overload recovery characteristic of the MAX426.

Auto-Zero Control Inputs

$\overline{AZ}$ controls auto-zero calibration. With LG at 0V, $\overline{AZ}$ can be driven with TTL or CMOS levels as long as V+ and V- are not exceeded. With ±5V operation, LG connects to supply ground and the op amp zeros when $\overline{AZ}$ is pulled within 0.8V of LG (Figure 4) for at least 10µs. The auto-zero cycle begins within 2µs and lasts about 125ms for the MAX425, 31ms for the MAX426. For single-supply operation, LG can be tied to V-. Again, when $\overline{AZ}$ is pulled to within 0.8V of LG, the amplifier zeros.

If $\overline{AZ}$ is tied low along with LG, an auto-zero cycle is internally triggered approximately once per minute. The input switching clock controls this interval, so CLK must not be disabled if auto-zero cycles are to be internally triggered. When an external clock source is used at the CLK input, the relation between this rate and the time between auto-zero cycles is: t_{AZ} (sec.) = 16,384/f_{CLK}. Although the time between cycles depends on CLK, the auto-zero cycle itself is timed by a separate

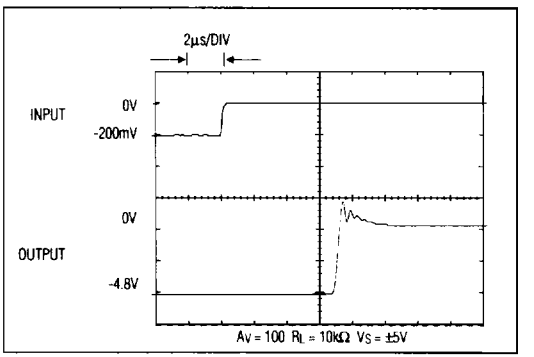

Figure 3. MAX426 Overload Recovery Time

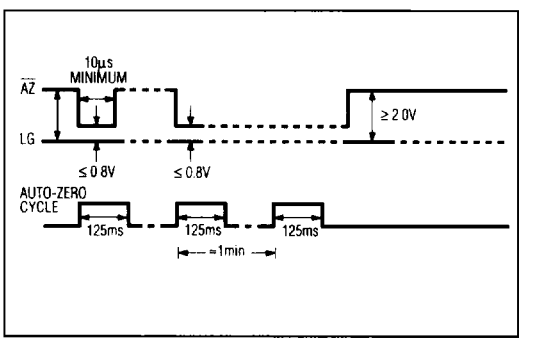

Figure 4. Auto-Zero Calibration Cycle Initiation – MAX425 cycle duration is 125ms and MAX426 is 31ms.

internal oscillator, independent from CLK, that runs only during auto-zero calibration.

During auto-zero, the amplifier's noninverting input remains connected to the input signal while the inverting input is internally shorted to the noninverting input. The output stage is held within 0.2V of its previous level. Since the amplifier is zeroed with both signal inputs shorted together at IN+, common-mode offset error is zeroed during calibration. Similarly, DC power-supply rejection error is auto-zeroed.

The auto-zero status function (AZ STAT) is available on pin 9 of the 16-pin small outline (SO) packages only. AZ STAT connects to the drain of a p-channel FET that is pulled to V+ while the device executes an auto-zero command. The typical FET on resistance is about 500Ω. By attaching a 47kΩ pull-down resistor from this pin to the system logic ground, the operator can monitor the device auto-zero cycle.

Amplifier Output

The MAX425/MAX426 feature 190dB of open-loop gain. Consequently, the amplifier's closed-loop DC gain error is negligible in even the most precise high-gain applications.

Outputs can swing from V+ to V- under lightly loaded conditions. Output impedance is typically 300Ω. Because the MAX425/MAX426 operate typically at 12mW, the chip temperature rises only 1°C to 2°C above ambient temperature. Such low self-heating minimizes thermocouple errors. Although optimized for 10kΩ loads, the MAX425/MAX426 drive a 2kΩ load to within a volt of each supply. However, such low-impedance loads are not recommended for precision applications, because changes in power dissipation within the op amp cause thermal gradients that limit performance. The current-limited output can withstand short circuits to either power supply or ground indefinitely.

Power Supply and Input Range

The MAX425/MAX426 are specified with a 10V (or ±5V) power supply, but will also operate with supplies ranging from 5V (±2.5V) to 15V (±7.5V). When operating with a 15V power supply, the amplifier's common-mode input voltage ranges from V- to V+ -2V. (Best common-mode and power-supply rejection are achieved with V_{IN} between V+ -2.5V and V- +1V.) A single 5V supply reduces the input common-mode voltage range to between 1V and 3V. As with most precision analog components, each supply should be bypassed at the amplifier with a 0.1µF ceramic capacitor.

The MAX425/MAX426 require 30ms on power-up to allow calibration circuits to initialize. However, the amplifier does NOT automatically auto-zero on power-up. The MAX425/MAX426 require a minimum supply of 4.5V to ensure the digital calibration circuit functions properly. The supply current is about 2.5mA until the first auto-zero cycle is initiated. Following the initial auto-zero cycle, the supply current typically drops to 1.2mA.

Input Bias Current

Two independent components comprise the input bias current: junction leakage current and charge injection current. The junction leakage current comes from the input protection diodes and the FET switches. The input protection diodes are very compact to minimize leakage currents. Thus, while still maintaining overvoltage protection, the leakage current is approximately 0.03pA at +25°C. Since package and printed circuit board leakage can add to this significantly, pay special attention to layout for accurate measurements.

The leakage current approximately doubles for every 8°C rise in temperature. This results in an input bias current of about 150pA at +125°C and 1.2nA at +150°C. This current tends to track in both input leads. For example, the offset current at +150°C is typically 20pA.

The second component of input bias current is charge injection current. This comes from the switching-clock circuitry. The bias current from charge injection is directly proportional to the clock frequency and varies with supply voltage. With ±5V supplies and a nominal 300Hz switching frequency, the charge injection current is about 120pA. This current flows into the IN+ terminal and out of the IN- terminal. At other clock frequencies, calculate the charge injection current by multiplying the switching-clock frequency by 0.4pA/Hz. If the switching clock is disabled, there is no charge injection input bias current. Charge injection current changes very little with temperature.

Below +125°C, charge injection current is the major component of the total input bias current. Above +125°C, the junction leakage current dominates the total input bias current.

In order to cancel the bias current-induced input offset voltage, circuit designers often add extra resistors to match the equivalent resistance at each of the amplifier input terminals. This technique reduces the apparent input offset voltage of most op amps because the bias current usually matches in magnitude and direction between the two input terminals. Thus, assuming matched input bias currents, any voltage at the op amp input due to bias current appears as a common mode, not a differential input voltage.

Bias current cancellation resistors should NOT be used when the MAX425/MAX426 are operated with the switching clock. In this case, the charge injection component dominates the input bias current. The charge injection current flows in opposite directions in the

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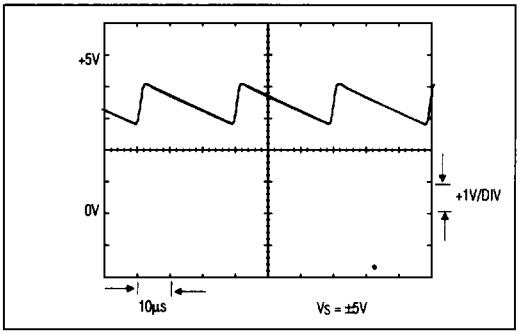

Figure 5. Typical Waveform at CLK Pin

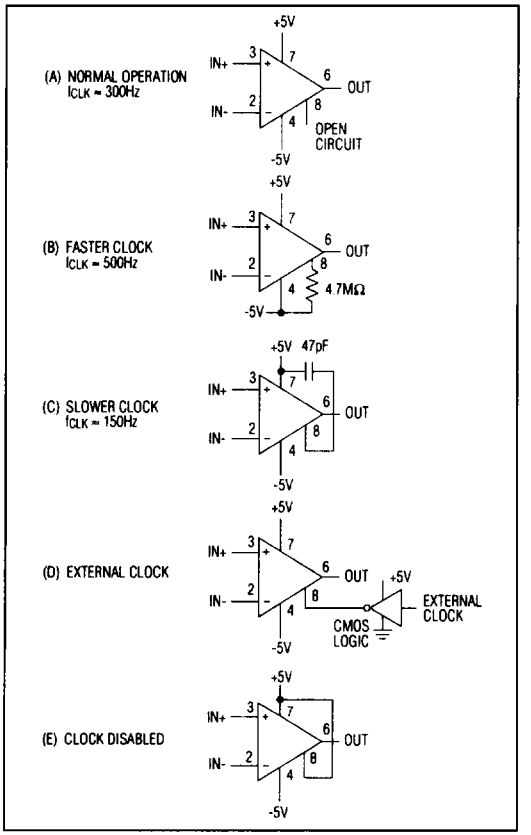

Figure 6. The oscillator frequency for the switching amplifier can be altered as shown in drawings (A) through (E).

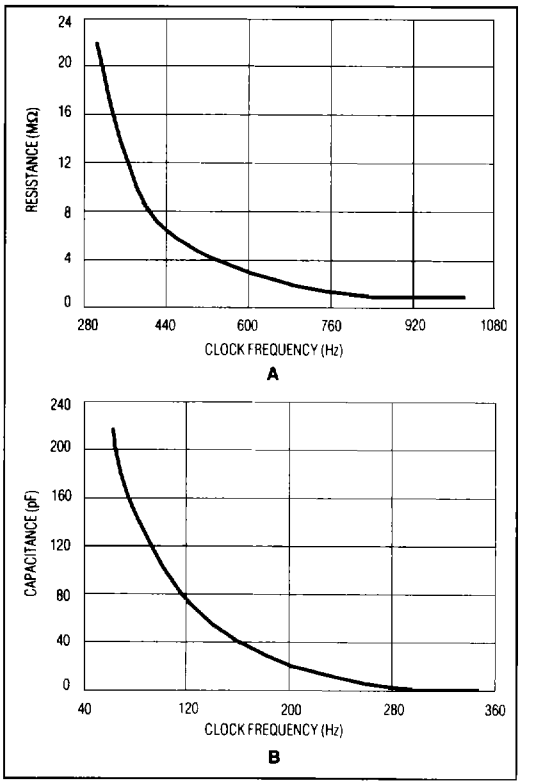

Figure 7. A: Clock Frequency vs. Resistance (Resistor to V-) B: Clock Frequency vs. Capacitance (Capacitor to V+)

MAX425/MAX426 input terminals. Thus, instead of cancelling offsets due to bias current flowing through resistors, the error signals add together and actually increase the apparent offset voltage.

In high-temperature applications (above +125°C) where the clock isn't used, the junction leakage current component dominates the input bias current. The junction leakage current flows into both amplifier inputs. When operating under these conditions, the circuit designer should match the resistance paths in both input leads to take advantage of the excellent matching of leakage currents. The input offset current of the MAX425/MAX426 is typically less than 2nA at +200°C.

Internal/External Clock

The MAX425/MAX426 internal switching clock free runs at about 38kHz with no external components connected to CLK and is internally divided by 128. A 300Hz input

switching frequency results. CLK connects directly to an internal 20pF timing capacitor where the signal oscillates between V+ -1V and V+ -2V. Figure 5 plots a typical waveform at CLK. The clock frequency can be adjusted or driven as shown in Figure 6.

To slow the internal clock, add a capacitor between CLK and V+. To increase clock rate, connect a resistor from CLK to V-. The frequency should not be increased by more than a factor of 3 using this technique. The oscillator can also be shut down by driving CLK to within 0.1V of V+ or below V+ -3.0V. Figure 6 shows all of the clock operating modes. Figure 7A shows the typical variation of the internal clock frequency vs. resistance between CLK and V-. Figure 7B shows the typical variation of the internal clock frequency vs. capacitance between CLK and V+.

When driving CLK from an external source, the input signal should swing within 0.1V of V+ and at least 3V below V+. Standard CMOS logic families do this reliably. These levels will override the internal oscillator AND the internal divider, so the external clock rate and the input switching frequency will be the same. When directly driving CLK, only a 50% duty-cycle square wave can be used for optimum offset correction. (The internal divider is disabled and cannot "square up" the waveform.) If necessary, a flip-flop or divider should be connected between the clock source and the CLK input to ensure a precise 50% duty-cycle.

Applications Information

Noise

The MAX425/MAX426 are the first offset-corrected op amps designed primarily for low-noise performance. Clock feedthrough, ripple, low frequency (1/f), and wideband noise are three to five times lower than present chopper-stabilized amplifiers. Figure 8A shows noise in a 10Hz bandwidth below 250nV$_{p-p}$. Figure 8B shows noise in 1Hz bandwidth. Low noise is especially important where high-resolution measurements are made since such noise limits resolution and requires excess filtering. In Figures 9A and 9B, 10Hz and 1Hz noise are shown with the CLK disabled. This noise is greater than that shown in Figure 8 because the switching clock no longer removes the amplifier's 1/f noise. Figure 10 shows the wideband noise (1kHz to 100kHz) of a MAX426.

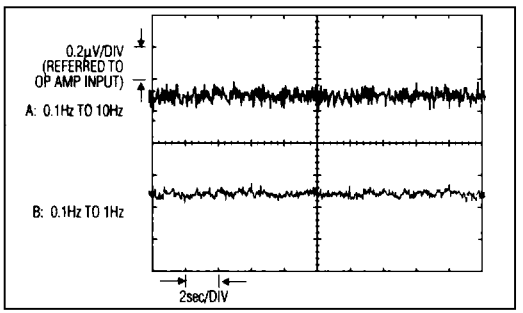

Figure 8. MAX425/MAX426 Noise in 10Hz and 1Hz Bandwidths (Switching Clock On)

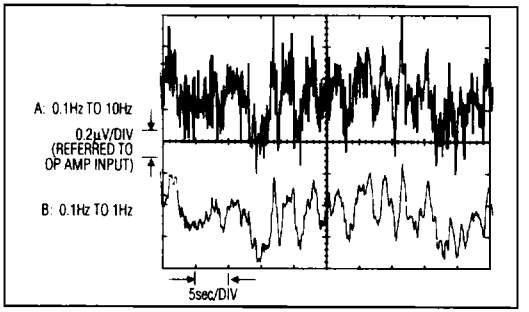

Figure 9. MAX425/MAX426 Noise in 10Hz and 1Hz Bandwidths (Switching Clock Off)

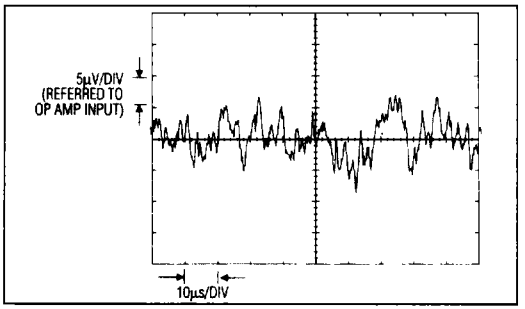

Figure 10. MAX425/MAX426 Wideband Noise (1kHz to 100kHz) (Swithching Clock Off)

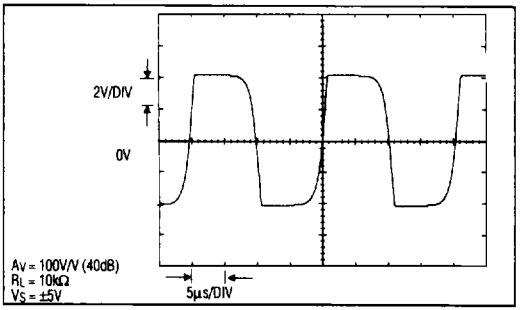

Figure 11. MAX426 Large Signal Response (Response to 80mV$_{p-p}$, 50kHz Square-Wave Input)

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Switching-Clock Frequency

The clock-induced input bias current of the amplifier (due to the switching action) varies directly with the CLK frequency. This current is about 120pA with a 300Hz switching clock and increases at a rate of about 0.4pA/Hz. In applications where input bias current specification is critical (such as low-level current to voltage converters), operate with a low clock frequency or disable the clock. The input bias current with the clock disabled is typically 0.2pA at +25°C. Even without the clock, the MAX425/MAX426 input offset voltage and noise specifications exceed those of most CMOS op amps.

High-Frequency Applications – MAX426

With a midband voltage noise density of $8nV/\sqrt{Hz}$, the wideband MAX426 has the same broadband noise as a 3.9kΩ resistor. This, along with its 15MHz gain bandwidth, makes it a logical choice for high-precision, high-speed applications. Symmetric output drive capability also allows the MAX426 to perform out to its gain-bandwidth limit. The MAX426 is designed to be stable with a closed-loop gain of 30V/V (30dB) or greater. Figure 11 shows a MAX426 operating at a closed-loop gain of 100V/V (40dB). The input signal is an $80mV_{p-p}$ square wave at 50kHz. Note the high degree of symmetry at the amplifier output.

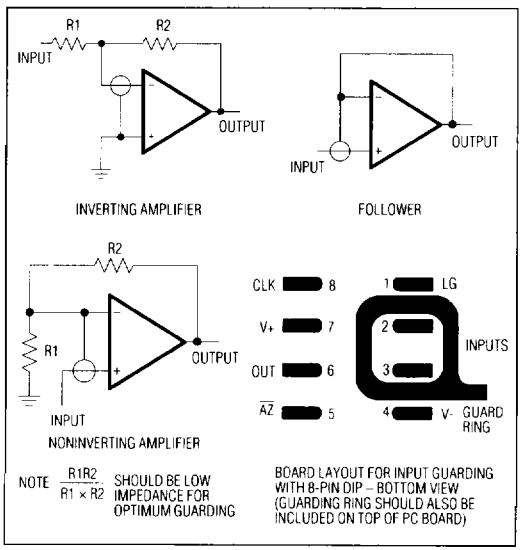

Figure 12. Input-Guard Connections

Working with Low-Level Signals

To take full advantage of the MAX425/MAX426 drift and offset capabilities when amplifying low-level signals, the circuit must be laid-out carefully. Unfortunately, in many low-level circuits, a schematic alone does not provide all the necessary information for a successful design. External characteristics that can degrade "ideal" performance include thermoelectric effects, noise pickup, board leakage, and improper grounding.

Thermoelectric potentials are created when wires/circuit board traces made from dissimilar metals are subjected to temperature gradients. The same principle works with thermocouples. When it occurs in the input of precision circuitry, the resulting voltage (often many microvolts) adds to temperature drift and offset errors. The most effective way to minimize this is to match the dissimilar metals or junctions in the circuit, remove the temperature gradient, or both.

Noise pick-up is best eliminated by minimizing the physical size of the input portions of the circuit. The summing input node (IN-) on high-gain stages is critical. Components connected to this point should have the shortest lead length on the amplifier side, and board traces should be as short as possible. If input lines must be long, use shielded wire.

Board leakage can degrade amplifier performance in high-gain stages that employ large resistances. Even low gain may be susceptible if signal source impedance is very high. In such applications, a guard ring (Figure 12) provides a low impedance point for external leakage currents to flow. Guard both sides of the board. The guard potential should be close to that of the inputs. Also remove flux and other residue from handling. Surface coating may be desirable for harsh environments, but take extreme care to ensure that contaminants are not trapped beneath the coating.

Single-point grounds are mandatory for low-level, high-gain circuits. The key is to ensure ground current from amplifier outputs do not generate ground differentials, which are seen by input stages in a way that makes them indistinguishable from real input signals.

High-Temperature Operation

Although the MAX425/MAX426 are not tested at temperatures above +125°C, input-switching and auto-zero functions will operate to about +150°C. At temperatures beyond +150°C, the internal clock will no longer function properly, and the amplifier cannot be auto-zeroed. But it still maintains operation as an unswitched, nonauto-zeroed CMOS op amp. At +200°C, input bias current is typically 50nA, and offset drift is about 0.5µV/°C. Plastic packaged parts should not be operated at ambient temperatures above +150°C.

Integrating Analog-to-Digital Converters

Because of their design flexibility, the MAX425/MAX426 can be used in many applications. For example, as the front-end integrator of a dual slope ADC, digital auto-zeroing nulls the offset of the amplifier as it discharges the integration capacitor. The switching clock may or may not be used during signal integration. The clock substantially reduces 1/f noise. Without the clock, input current (devoid of any switching spikes) is typically less than 1pA, which is orders of magnitude below the input bias current of bipolar amplifiers. During reference integration, the switching clock is held off to keep the output free of clock glitches. MAX425/MAX426 accuracy and noise performance allow a 20-bit dual slope ADC to be realized.

Weigh Scale

In the weigh-scale circuit of Figure 13, two amplifiers (A1 and A2) with appropriate gain resistors (R1 through R4), amplify the differential 20mV full-scale signal of the strain-gauge bridge by a factor of 300. This signal is then filtered and buffered by A3. The filter's approximate 3Hz bandwidth limits output noise to around 12μVRMS (40nVRMS referred to the input), which gives a signal-to-noise ratio of 114dB. Scale measurement to within a few parts per million is possible.

The two amplifiers A1 and A2 are auto-zeroed simultaneously. This only needs to be done occasionally (several minutes or more) because the effects of internal drift appear only as a small 300Hz ripple signal with an average value of zero. This ripple is removed by the 3Hz filter. Amplifiers A1 and A2 switching clocks free run to minimize 1/f noise. A3 1/f noise is not significant because of A3's low gain. Figure 13 assumes the strain gauge is loaded with a tare weight, so the output signal is always positive. Consequently, A3's output is always positive, so A1, A2, and A3 may all be powered from a single 10V supply. R7 and C4 keep the voltage across C3 to a minimum without affecting the performance of the filter. For optimal performance, guard traces on the top and bottom of the printed circuit board should surround both the sensitive nodes where R5, R6 and C2 connect and the IN+ node of the amplifier.

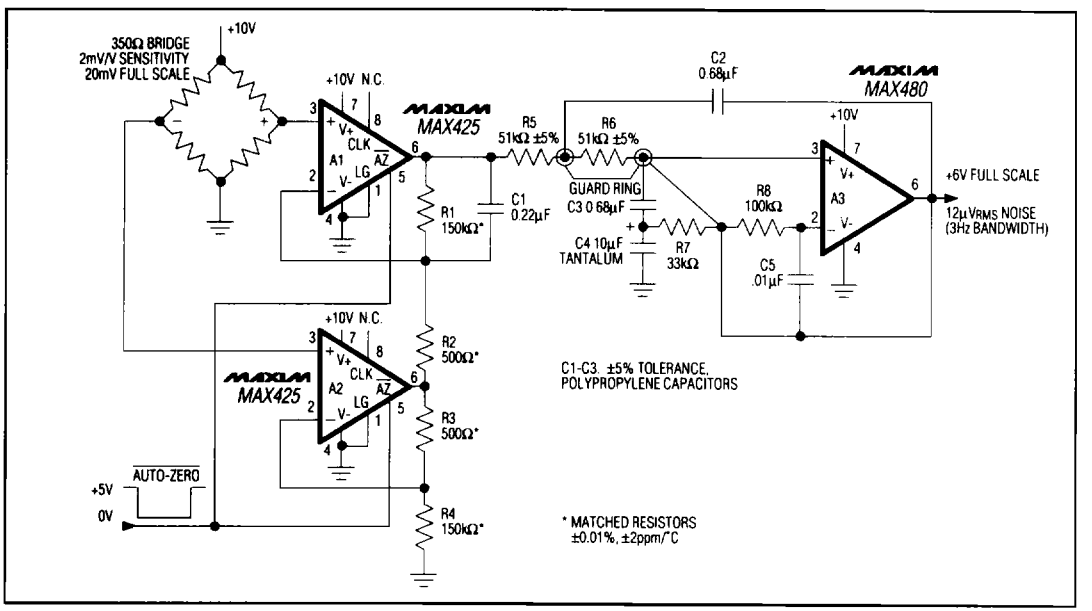

Figure 13. Weigh-Scale Circuit

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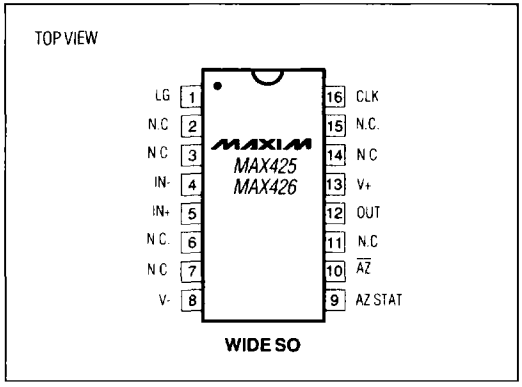
Pin configurations (continued)



Chip Topography