

SDLS028

**SN5403, SN54LS03, SN54S03,  
SN7403, SN74LS03, SN74S03**

**QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

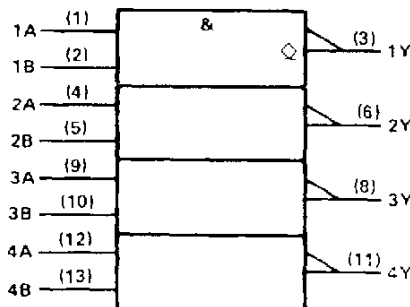
These devices contain four independent 2-input-NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher  $V_{OH}$  levels.

The SN5403, SN54LS03 and SN54S03 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7403, SN74LS03 and SN74S03 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE (each gate)**

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

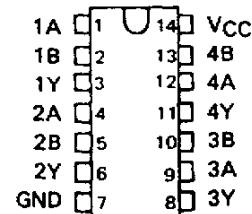
**logic symbol †**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

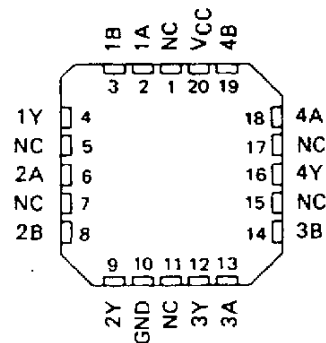
SN5403 . . . J OR W PACKAGE  
SN54LS03, SN54S03 . . . J OR W PACKAGE  
SN7403 . . . N PACKAGE  
SN74LS03, SN74S03 . . . D OR N PACKAGE

(TOP VIEW)



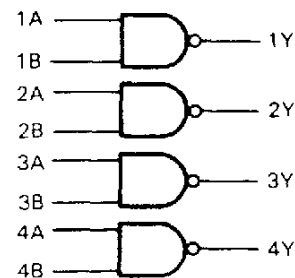
SN54LS03, SN54S03 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

**logic diagram (positive logic)**



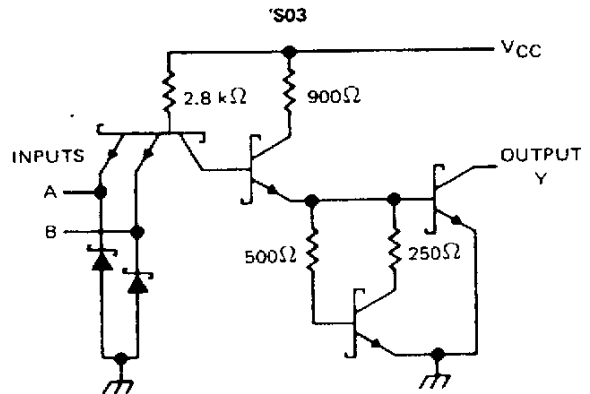
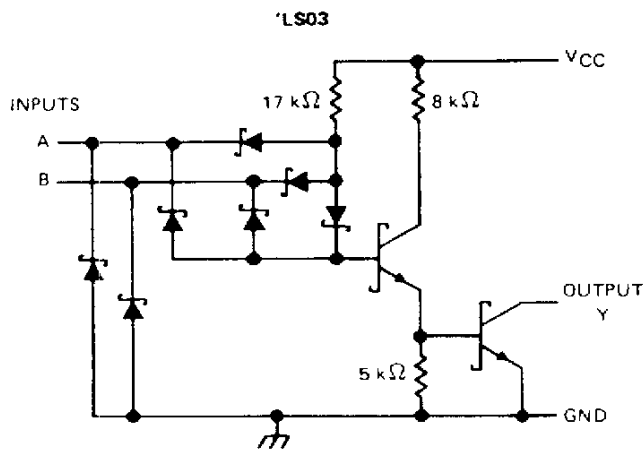
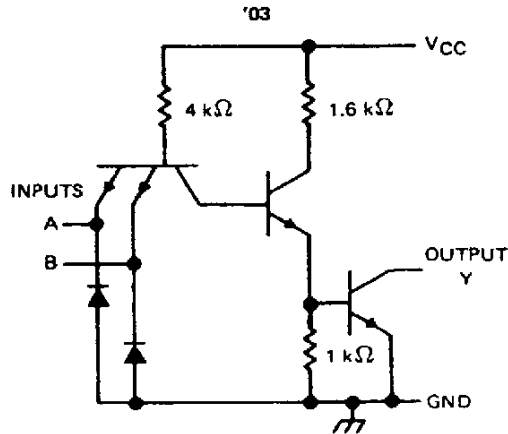
$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

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**SN5403, SN54LS03, SN54S03,  
SN7403, SN74LS03, SN74S03**  
**QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

schematics (each gate)



Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage: '03, 'S03 .....	5.5 V
'LS03 .....	7 V
Off-state output voltage .....	7 V
Operating free-air temperature range: SN54' .....	-55°C to 125°C
SN74' .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## SN5403, SN7403

### QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

#### recommended operating conditions

	SN5403			SN7403			UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX			
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
$V_{IH}$ High-level input voltage	2			2			V		
$V_{IL}$ Low-level input voltage	0.8			0.8			V		
$V_{OH}$ High-level output voltage	5.5			5.5			V		
$I_{OL}$ Low-level output current	16			16			mA		
$T_A$ Operating free-air temperature	- 55			125			0	70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN5403			SN7403			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
$I_{OH}$	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$						0.25	mA
	$V_{CC} = \text{MIN}, V_{IL} = 0.7 \text{ V}, V_{OH} = 5.5 \text{ V}$			0.25				
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{CCH}$	$V_{CC} = \text{MAX}, V_I = 0$		4	8		4	8	mA
$I_{CCL}$	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		12	22		12	22	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

#### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Y	$R_L = 4 \text{ k}\Omega,$	$C_L = 15 \text{ pF}$		35	45	ns
$t_{PHL}$			$R_L = 400 \Omega,$	$C_L = 15 \text{ pF}$		8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

# SN54LS03, SN74LS03 QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

## recommended operating conditions

	SN54LS03			SN74LS03			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.7			0.8	V
V <sub>OH</sub> High-level output voltage			5.5			5.5	V
I <sub>OL</sub> Low-level output current			4			8	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS03		SN74LS03		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		-1.5	V	
I <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>OH</sub> = 5.5 V			0.1		0.1	mA	
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4	V
	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA					0.35	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1		0.1	mA	
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20		20	μA	
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4		-0.4	mA	
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0		0.8	1.6		0.8	1.6	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		17	32	ns
t <sub>PHL</sub>					15	28	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## SN54S03, SN74S03 QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

### recommended operating conditions

	SN54S03			SN74S03			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$V_{OH}$ High-level output voltage			5.5			5.5	V
$I_{OL}$ Low-level output current			20			20	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54S03			SN74S03			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
$I_{OH}$	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$						0.25	mA
	$V_{CC} = \text{MIN}, V_{IL} = 0.7 \text{ V}, V_{OH} = 5.5 \text{ V}$			0.25				
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	μA
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{CCH}$	$V_{CC} = \text{MAX}, V_I = 0$		6	13.2		6	13.2	mA
$I_{CCL}$	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		20	36		20	36	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$	2	5	7.5	ns
$t_{PHL}$				2	4.5	7	ns
$t_{PLH}$			$R_L = 280 \Omega, C_L = 50 \text{ pF}$	7.5			ns
$t_{PHL}$				7			ns

NOTE 2. Load circuits and voltage waveforms are shown in Section 1.

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### SN74LS03, Quad 2-input positive-NAND gates with open collector outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS03	SN74LS03
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		- /8
No. of Gates	4	4
Static Current		3
tpd max (ns)		32

#### FEATURES

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- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

#### DESCRIPTION

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These devices contain four independent 2-input-NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher  $V_{OH}$  levels.

The SN5403, SN54LS03 and SN54S03 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7403, SN74LS03 and SN74S03 are characterized for operation from 0°C to 70°C.

#### TECHNICAL DOCUMENTS

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#### DATASHEET

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Full datasheet in Acrobat PDF: [sn74ls03.pdf](#) (123 KB) (Updated: 03/01/1988)

#### APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Designing with the SN54/74LS123 \(Rev. A\)](#) (SDLA006A - Updated: 03/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)

**RELATED DOCUMENTS**

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- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

**PRICING/AVAILABILITY/PKG**

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY   SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS03D	ACTIVE	<a href="#">SOP (D)</a>   14	0 TO 70	<a href="#">View Contents</a>	1KU   0.28	50	<a href="#">N/A*</a>	> 10k   07 Oct	4 WKS			
								> 10k   14 Oct				
								> 10k   21 Oct				
SN74LS03DR	ACTIVE	<a href="#">SOP (D)</a>   14	0 TO 70	<a href="#">View Contents</a>	1KU   0.31	2500	<a href="#">N/A*</a>	490   25 Sep	4 WKS			
								> 10k   04 Oct				
								> 10k   11 Oct				
								> 10k   18 Oct				
SN74LS03N	ACTIVE	<a href="#">PDIP (N)</a>   14	0 TO 70	<a href="#">View Contents</a>	1KU   0.28	25	1000	10k   24 Sep	4 WKS	<a href="#">Avnet</a>   AMERICA	> 1k	<b>BUY NOW</b>
								3859   26 Sep		<a href="#">DigiKey</a>   AMERICA	317	<b>BUY NOW</b>
								100   03 Oct				
								> 10k   04 Oct				
								> 10k   09 Oct				
SN74LS03N3	OBSOLETE	<a href="#">PDIP (N)</a>   14	0 TO 70	<a href="#">View Contents</a>	1KU		<a href="#">N/A*</a>		Not Available			
SN74LS03NSR	ACTIVE	<a href="#">SOP (NS)</a>   14		<a href="#">View Contents</a>	1KU   0.28	2000	<a href="#">N/A*</a>	> 10k   04 Oct	4 WKS			
								> 10k   11 Oct				



								> 10k   18 Oct			
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Table Data Updated on: 9/26/2002