Programmable Timing Control Hub™ for P4™ processor

Recommended Application:

CK410M Compliant Main Clock

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 8 - 0.7V current-mode differential SRC pairs
- 1 - 0.7V current-mode differential CPU_ITP/SRC selectable pair
- 4 - PCI (33MHz)
- 1 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 1 - REF, 14.318MHz
- 1 - 0.7V current-mode differential LCD/SRC selectable pair

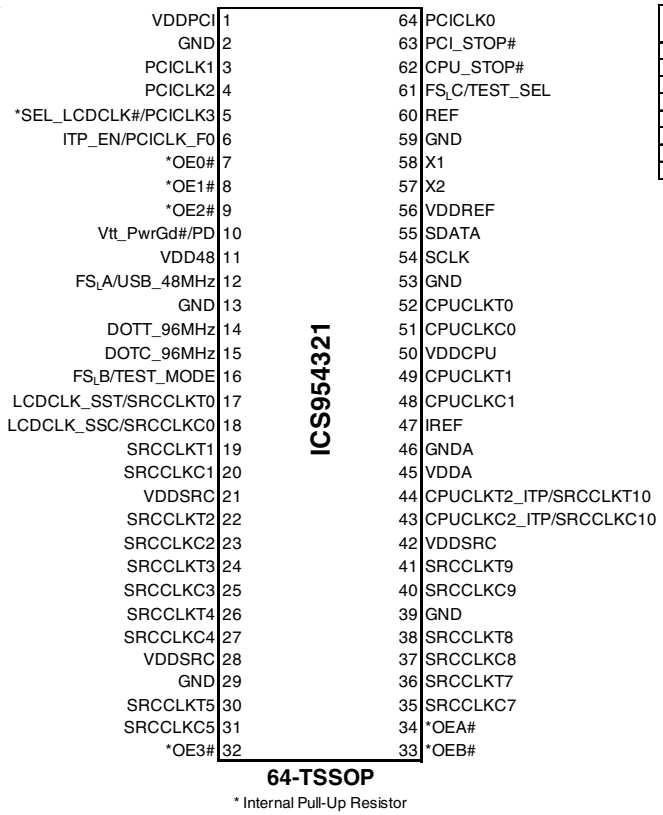
Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 300ppm frequency accuracy on CPU, and SRC clocks
- +/- 100ppm frequency accuracy on USB clocks

Features/Benefits:

- Supports tight ppm accuracy clocks for SRC
- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, SRC pair in PD for power management.
- OE# pins to support SRC power management.

Pin Configuration



64-TSSOP

* Internal Pull-Up Resistor

Functionality Table

FSLC B6b2	FSLB B6b1	FSLA B6b0	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz	Spread %
0	0	0	266.66	100.00	33.33	14.318	48.00	96.00	0.5% Down
0	0	1	133.33	100.00	33.33	14.318	48.00	96.00	0.5% Down
0	1	0	200.00	100.00	33.33	14.318	48.00	96.00	0.5% Down
0	1	1	166.66	100.00	33.33	14.318	48.00	96.00	0.5% Down
1	0	0	333.33	100.00	33.33	14.318	48.00	96.00	0.5% Down
1	0	1	100.00	100.00	33.33	14.318	48.00	96.00	0.5% Down
1	1	0	400.00	100.00	33.33	14.318	48.00	96.00	0.5% Down
1	1	1	200.00	100.00	33.33	14.318	48.00	96.00	0.5% Down

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
2	GND	PWR	Ground pin.
3	PCICLK1	OUT	PCI clock output.
4	PCICLK2	OUT	PCI clock output.
5	*SEL_LCDCLK#/PCICLK3	I/O	Latched input select for LCD_ss/ SRCCLK output frequency: 0 = LCD, 1 = SRCCLK/ 3.3V free-running PCI clock output.
6	ITP_EN/PCICLK_F0	I/O	Free running PCI clock not affected by PCI_STOP#. ITP_EN: latched input to select pin functionality 1 = CPU_ITP pair 0 = SRC pair
7	*OE0#	IN	Active low input for enabling DIF pair 0. 1 = tri-state outputs, 0 = enable outputs
8	*OE1#	IN	Active low input for enabling DIF pair 1. 1 = tri-state outputs, 0 = enable outputs
9	*OE2#	IN	Active low input for enabling DIF pair 2. 1 = tri-state outputs, 0 = enable outputs
10	Vtt_PwrGd#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
11	VDD48	PWR	Power pin for the 48MHz output.3.3V
12	FSLA/USB_48MHz	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V.
13	GND	PWR	Ground pin.
14	DOTT_96MHz	OUT	True clock of differential pair for 96.00MHz DOT clock.
15	DOTC_96MHz	OUT	Complement clock of differential pair for 96.00MHz DOT clock.
16	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
17	LCDCLK_SST/SRCCLKT0	OUT	True clock of LCDCLK_SS output / True clock of SRCCLK differential pair. Selected by SEL_LCDCLK#
18	LCDCLK_SSC/SRCCLKC0	OUT	Complementary clock of LCDCLK_SS output / Complementary clock of SRCCLK differential pair. Selected by SEL_LCDCLK#
19	SRCCLKT1	OUT	True clock of differential SRC clock pair.
20	SRCCLKC1	OUT	Complement clock of differential push-pull SRC clock pair.
21	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
22	SRCCLKT2	OUT	True clock of differential SRC clock pair.
23	SRCCLKC2	OUT	Complement clock of differential SRC clock pair.
24	SRCCLKT3	OUT	True clock of differential SRC clock pair.
25	SRCCLKC3	OUT	Complement clock of differential SRC clock pair.
26	SRCCLKT4	OUT	True clock of differential SRC clock pair.
27	SRCCLKC4	OUT	Complement clock of differential SRC clock pair.
28	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
29	GND	PWR	Ground pin.
30	SRCCLKT5	OUT	True clock of differential SRC clock pair.
31	SRCCLKC5	OUT	Complement clock of differential SRC clock pair.
32	*OE3#	IN	Active low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs

Note: Pins 5, 7, 8, 9, 32, 33, and 34 have internal pull-up resistors

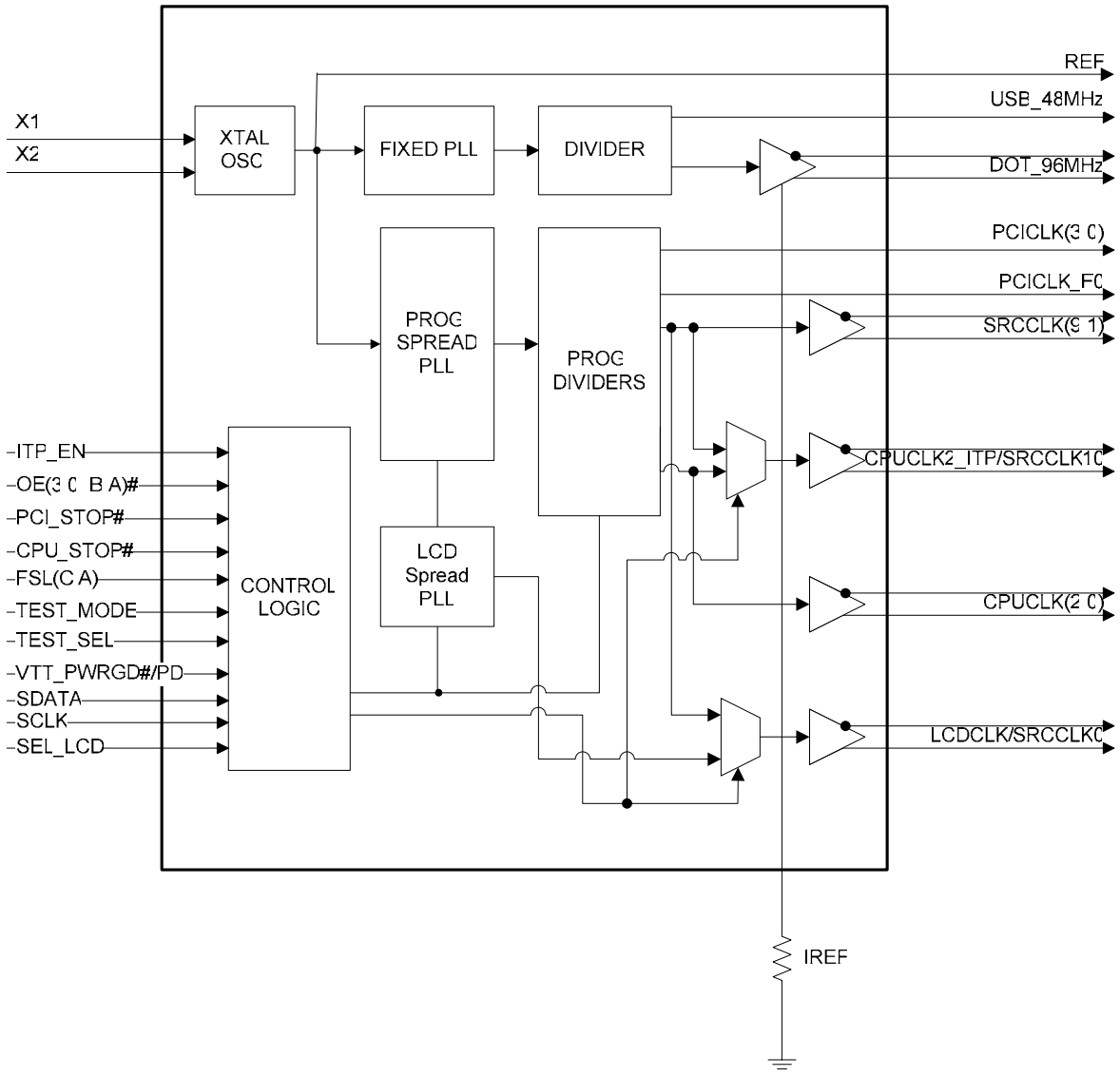
Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
33	*OEB#	IN	Active low input for enabling outputs. 1 = tri-state outputs, 0 = enable outputs
34	*OEA#	IN	Active low input for enabling outputs. 1 = tri-state outputs, 0 = enable outputs
35	SRCCLKC7	OUT	Complement clock of differential SRC clock pair.
36	SRCCLKT7	OUT	True clock of differential SRC clock pair.
37	SRCCLKC8	OUT	Complement clock of differential SRC clock pair.
38	SRCCLKT8	OUT	True clock of differential SRC clock pair.
39	GND	PWR	Ground pin.
40	SRCCLKC9	OUT	True clock of differential push-pull SRC clock pair.
41	SRCCLKT9	OUT	True clock of differential SRC clock pair.
42	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
43	CPUCLKC2_ITP/SRCCLKC10	OUT	Complementary clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
44	CPUCLKT2_ITP/SRCCLKT10	OUT	True clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
45	VDDA	PWR	3.3V power for the PLL core.
46	GNDA	PWR	Ground pin for the PLL core.
47	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
48	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
49	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
50	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
51	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
52	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
53	GND	PWR	Ground pin.
54	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
55	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
56	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
57	X2	OUT	Crystal output, Nominally 14.318MHz
58	X1	IN	Crystal input, Nominally 14.318MHz.
59	GND	PWR	Ground pin.
60	REF	OUT	14.318 MHz reference clock.
61	FSLC/TEST_SEL	IN	3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values. TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table
62	CPU_STOP#	IN	Stops all CPUCLK, except those set to be free running clocks
63	PCI_STOP#	IN	Stops all PCICLKs at logic 0 level, when low. Free running PCICLKs are not effected by this input.
64	PCICLK0	OUT	PCI clock output.

General Description

ICS954321 follows the Intel CK410M-compliant clock specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS954321** is driven with a 14.318MHz crystal.

Block Diagram



General I²C serial interface information for the ICS954321

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
○		
○		○
○		○
		○
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
	X Byte	Beginning Byte N	
ACK			
		○	
○		○	
○		○	
○			
		Byte N + X - 1	
N	Not acknowledge		
P	stoP bit		

Table2: LCDCLK Spread and Frequency Selection Table

Byte 6b7	Byte 6b6	Byte 6b5	Byte 6b4	Byte 6b3	Pin 17/18	Spread
					MHz	%
0	0	0	0	0	96.00	0.8 Down
0	0	0	0	1	96.00	1 Down
0	0	0	1	0	96.00	1.25 Down
0	0	0	1	1	96.00	1.5 Down
0	0	1	0	0	96.00	1.75 Down
0	0	1	0	1	96.00	2 Down
0	0	1	1	0	96.00	2.5 Down
0	0	1	1	1	96.00	3 Down
0	1	0	0	0	96.00	+/-0.3 Center
0	1	0	0	1	96.00	+/-0.4 Center
0	1	0	1	0	96.00	+/-0.5 Center
0	1	0	1	1	96.00	+/-0.6 Center
0	1	1	0	0	96.00	+/-0.8 Center
0	1	1	0	1	96.00	+/-1.0 Center
0	1	1	1	0	96.00	+/-1.25 Center
0	1	1	1	1	96.00	+/-1.5 Center
1	0	0	0	0	100.00	0.8 Down
1	0	0	0	1	100.00	1 Down
1	0	0	1	0	100.00	1.25 Down
1	0	0	1	1	100.00	1.5 Down
1	0	1	0	0	100.00	1.75 Down
1	0	1	0	1	100.00	2 Down
1	0	1	1	0	100.00	2.5 Down
1	0	1	1	1	100.00	3 Down
1	1	0	0	0	100.00	+/-0.3 Center
1	1	0	0	1	100.00	+/-0.4 Center
1	1	0	1	0	100.00	+/-0.5 Center
1	1	0	1	1	100.00	+/-0.6 Center
1	1	1	0	0	100.00	+/-0.8 Center
1	1	1	0	1	100.00	+/-1.0 Center
1	1	1	1	0	100.00	+/-1.25 Center
1	1	1	1	1	100.00	+/-1.5 Center

SMBus Table: Output Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	44, 43	CPUCLK2_ITP/SRCCLK10 Enable	Output Enable	RW	Disable	Enable	1
Bit 6	36, 35	SRCCLK7 Enable	Output Enable	RW	Disable	Enable	1
Bit 5	31, 30	SRCCLK5 Enable	Output Enable	RW	Disable	Enable	1
Bit 4	27, 26	SRCCLK4 Enable	Output Enable	RW	Disable	Enable	1
Bit 3	25, 24	SRCCLK3 Enable	Output Enable	RW	Disable	Enable	1
Bit 2	23, 22	SRCCLK2 Enable	Output Enable	RW	Disable	Enable	1
Bit 1	20, 19	SRCCLK1 Enable	Output Enable	RW	Disable	Enable	1
Bit 0	18, 17	LCDCLK/SRCCLK0 Enable	Output Enable	RW	Disable	Enable	1

SMBus Table: Spread and Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Test Clock Mode Entry	Test Mode	RW	Disable	Enable	0
Bit 6	15, 14	DOT_96MHz Enable	Output Enable	RW	Disable	Enable	1
Bit 5	12	USB_48MHz Enable	Output Enable	RW	Disable	Enable	1
Bit 4	60	REFOUT Enable	Output Enable	RW	Disable	Enable	1
Bit 3	-	LCDCLK Spectrum Mode	Spread Control	RW	OFF	ON	1
Bit 2	49, 48	CPUCLK1	Output Enable	RW	Disable	Enable	1
Bit 1	52, 51	CPUCLK0	Output Enable	RW	Disable	Enable	1
Bit 0	-	Spread Spectrum Mode	Spread Control for PLL1	RW	OFF	ON	0

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	5	PCICLK3	Output Enable	RW	Disable	Enable	1
Bit 6	4	PCICLK2	Output Enable	RW	Disable	Enable	1
Bit 5	3	PCICLK1	Output Enable	RW	Disable	Enable	1
Bit 4	64	PCICLK0	Output Enable	RW	Disable	Enable	1
Bit 3	-	Test Mode Selection	Test Mode Selection	RW	Hi-Z	REF/N	0
Bit 2	-	PCI_STOP	Stop all PCI clocks	RW	Enable	Disable	1
Bit 1	6	PCI_F0 Enable	Output Enable	RW	Disable	Enable	1
Bit 0	-	Reserved					1

SMBus Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved					-
Bit 6	41, 40	SRCCLK9 Enable	Output Enable	RW	Disable	Enable	1
Bit 5	38, 37	SRCCLK8 Enable	Output Enable	RW	Disable	Enable	1
Bit 4	-	Reserved					-
Bit 3	-	Reserved					-
Bit 2	-	Reserved					-
Bit 1	-	Reserved					-
Bit 0	-	Reserved					-

SMBus Table:Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved					1
Bit 6	-	96MHz	Driven in PD	RW	Driven	Hi-Z	1
Bit 5	-	REFOUT STRENGTH	Strength Programming	RW	1X	2X	1
Bit 4	-	Reserved					1
Bit 3	-	PCI_F0	Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in SMBus register to stop PCICLK_F output.	RW	Free Running	Stoppable	1
Bit 2	-	CPUCLK2_ITP	Allow assertion of CPU_STOP# to stop CPUCLK outputs	RW	Free Running	Stoppable	1
Bit 1	-	CPUCLK1		RW	Free Running	Stoppable	1
Bit 0	-	CPUCLK0		RW	Free Running	Stoppable	1

SMBus Table:Output Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved					-
Bit 6	-	CPUCLK2_ITP_STOP Drive Mode	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 5	-	CPUCLK1_STOP Drive Mode		RW	Driven	Hi-Z	0
Bit 4	-	CPUCLK0_STOP Drive Mode		RW	Driven	Hi-Z	0
Bit 3	-	SRCCLK (10:7, 5:0), LCD PD Drive Mode	Driven in Powerdown (PD)	RW	Driven	Hi-Z	0
Bit 2	-	CPUCLK2_ITP PD Drive Mode		RW	Driven	Hi-Z	0
Bit 1	-	CPUCLK[1:0] PD Drive Mode		RW	Driven	Hi-Z	0
Bit 0	-	ITP_EN	SRCCLK/CPU_ITP select	R	SRCCLK6	CPU_ITP	latch

SMBus Table: Output Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SS4	LCDCLK Spread Prog Bit 4	RW	96Mhz	100Mhz	0
Bit 6	-	SS3	LCDCLK Spread Prog Bit 3	RW	See Table 2: LCDCLK Freq Sel		1
Bit 5	-	SS2	LCDCLK Spread Prog Bit 2	RW			0
Bit 4	-	SS1	LCDCLK Spread Prog Bit 1	RW			0
Bit 3	-	SS0	LCDCLK Spread Prog Bit 0	RW			0
Bit 2	-	FSLC	Freq Select Bit 2	R	See Table 1: PLL1 Frequency Selection Table		Latched
Bit 1	-	FSLB	Freq Select Bit 1	R			Latched
Bit 0	-	FSLA	Freq Select Bit 0	R			Latched

SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	x
Bit 6	-	RID2		R	-	-	x
Bit 5	-	RID1		R	-	-	x
Bit 4	-	RID0		R	-	-	x
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 17 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			1
Bit 3	-	BC3		RW			0
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			1

SMBus Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDH_EN	Watchdog Hard Alarm Enable	RW	Disable	Enable	0
Bit 6	-	WDS_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Bit 5	-	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	-	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	X
Bit 3	-	WDTCtrl	Watch Dog Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	-	WD2	WD Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

SMBus Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLLM/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	LCDCLK/SRCCLK0 SEL	SELSRC/LCDCLK#	R	LCDCLK	SRCCLK0	latch
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved					-
Bit 3	-	WD Safe Freq Source	WD Safe Freq Source	RW	Latch	B10b(2:0)	0
Bit 2	-	WD SFC	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte6 bit (2:0).		0
Bit 1	-	WD SFB		RW			0
Bit 0	-	WD SFA		RW			0

SMBus Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div 9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(8:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	SRCCLK Div3	SRCCLK Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-	SRCCLK Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-	SRCCLK Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-	SRCCLK Div0		RW	0011:/15	0111:/30	1011:/60	1111:/120	X
Bit 3	-	CPU Div3	CPUDivider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-	CPU Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-	CPU Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-	CPU Div0		RW	0011:/15	0111:/30	1011:/60	1111:/120	X

SMBus Table: CLKREQ# Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	OEB# controls selected outputs. Outputs controlled by this pin will be Hi-Z when OEB# is high.	SRCCLK4 is controlled	RW	Not Controlled	Controlled	1
Bit 5	-		SRCCLK8 is controlled	RW	Not Controlled	Controlled	0
Bit 4	-		SRCCLK10 is controlled	RW	Not Controlled	Controlled	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	OEA# controls selected outputs. Outputs controlled by this pin will be Hi-Z when OEA# is high.	SRCCLK5 is controlled	RW	Not Controlled	Controlled	1
Bit 1	-		SRCCLK7 is controlled	RW	Not Controlled	Controlled	0
Bit 0	-		SRCCLK9 is controlled	RW	Not Controlled	Controlled	0

SMBus Table: PLL 2 VCO Frequency Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: PLL 2 VCO Frequency Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(8:0)	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: PLL 2 Spread Spectrum Control Register

Byte 19		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-		SSP6		RW			X
Bit 5	-		SSP5		RW			X
Bit 4	-		SSP4		RW			X
Bit 3	-		SSP3		RW			X
Bit 2	-		SSP2		RW			X
Bit 1	-		SSP1		RW			X
Bit 0	-		SSP0		RW			X

SMBus Table: PLL2 Spread Spectrum Control Register

Byte 20		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved	Reserved	R	-	-	0
Bit 6	-		SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-		SSP13		RW			X
Bit 4	-		SSP12		RW			X
Bit 3	-		SSP11		RW			X
Bit 2	-		SSP10		RW			X
Bit 1	-		SSP9		RW			X
Bit 0	-		SSP8		RW			X

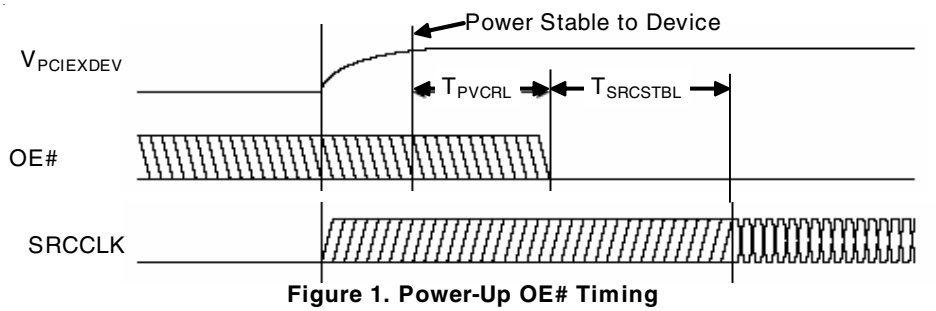


Figure 1. Power-Up OE# Timing

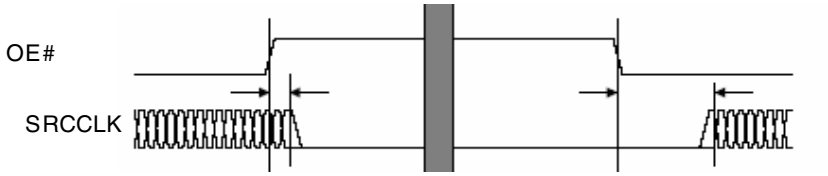


Figure 2. OE# Control Timing

Table 1. Power-Up OE# Timing1

Symbol	Parameter	Min	Max	Units
T_{PVCRL}	Power Valid to OE# Output Active (Fig. 1)		100	µs
$T_{SRCSTBL}$	SRC Clock Stablilzation Time from assertion of OE# (Fig. 1)		800	µs

[1]This timing is valid only after system clocks are stable.

Table 2. OE# Control Timing

Symbol	Parameter	Min	Max	Units
T_{CRHoff}	OE# De-asserted High to SRCCLK Parked (Fig. 2)	0		µs
T_{CRHon}	OE# Asserted LOW to SRCCLK Active (Fig. 2)		0.4	µs

OE# - Assertion (transition from logic "1" to logic "0")
The impact of asserting the OE# pin is that the SRCCLK output will become active per the timing found in the OE# Control Timing Table. The clock will become active in a glitch free manner, providing a full cycle at the time it becomes active.

OE# - De-Assertion (transition from logic "0" to logic "1")
The impact of asserting the OE# pin is that the SRCCLK output will become inactive setliing in the Tristate condition per the timing found the OE# Control Timing Table. The clock will become inactive in a glitch free manner.

Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			V_{DD} + 0.5V	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			350	mA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	CPU(1:0), V_T = 50%			100	ps	1
Skew	t_{sk4}	CPU(1:0) to CPU2_ITP, V_T = 50%			150	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom (CPU2_ITP)			125	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom, (CPU(1:0))			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - SRC and LCD 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabsmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	V_T = 50%			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			125	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}$*(0.5)	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-33			mA	1
		V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	30			mA	1
		V_{OL} = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[3] Spread Spectrum is off

Electrical Characteristics - USB48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8313		20.8354	ns	2
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V			-29	mA	1
		V_{OH} = 3.135 V	-23			mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	29			mA	1
		V_{OL} = 0.4 V			27	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Edge Rate	t_{slewr/f_USB}	USB48 Rising/Falling edge rate	1		2	V/ns	1
Rise Time	t_{r_USB}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f_USB}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - DOT_96MHz 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Average period	Tperiod	96.00MHz nominal	10.4135		10.4198	ns	2
Absolute min period	Tabsmin	96.00MHz nominal	10.1635			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			250	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

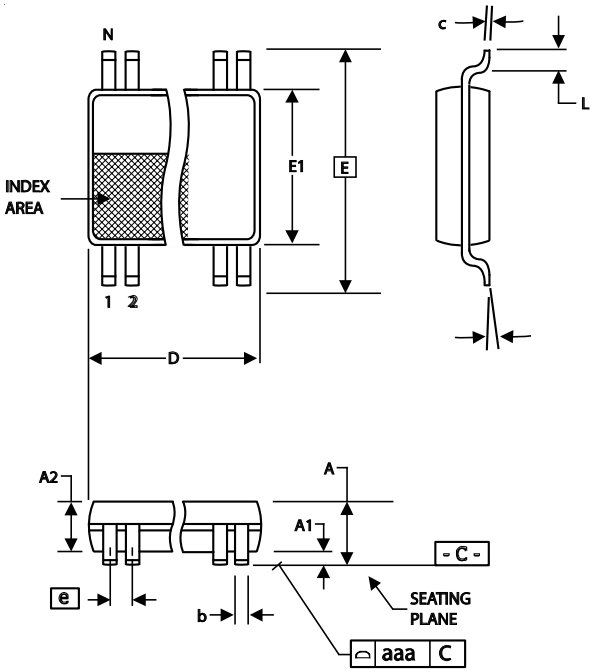
Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} = 1.0 V	-33			mA	1
		V_{OH} = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} = 1.95 V	30			mA	1
		V_{OL} = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Skew	t_{sk1}	V_T = 1.5 V			500	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz



6.10 mm. Body, 0.50 mm. Pitch TSSOP (240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS954321yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

1078B—09/20/05

Revision History

Rev.	Issue Date	Description	Page #
A	8/2/2005	Final Release	-
B	9/20/2005	1. Added LCDCLK Frequency Table. 2. Updated SMBus B0b7 from R to RW.	6, 7