Signetics

54LS109
Flip-Flop

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop

Product Specification

Military Logic Products

DESCRIPTION

The 54LS109 is a dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active Low inputs and operate independently of the Clock input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table.

The J and $\overline{K}$ inputs must be stable just one set-up time prior to the Low-to-High transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.7V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

ORDERING INFORMATION

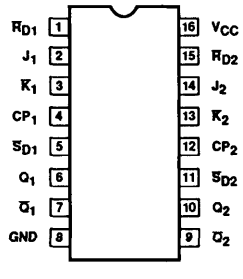
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS109/BEA
16-Pin Ceramic FlatPack	54LS109/BFA
16-Pin Ceramic LLCC	54LS109/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
CP	Clock input	1LSUL
$\overline{R}_D$	Reset input	2LSUL
$\overline{S}_D$	Set input	2LSUL
J, $\overline{K}$	Data inputs	1LSUL
Q, $\overline{Q}$	Outputs	10LSUL

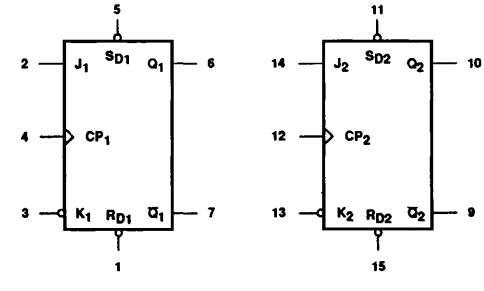
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



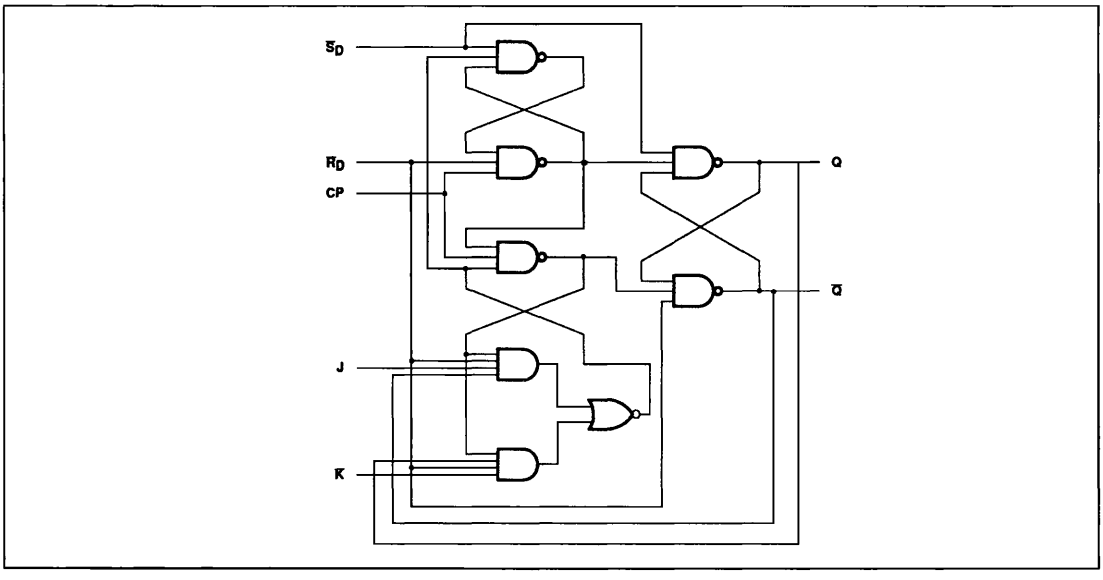
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = High voltage level steady state.
L = Low voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High Clock transition.
l = Low voltage one setup time prior to the Low-to-High Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High Clock transition.
↑ = Low-to-High Clock transition.

NOTE: Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	μA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V	J, $\overline{K}$ inputs			0.1	mA
			$\overline{R}_D$, $\overline{S}_D$ inputs			0.2	mA
			CP inputs			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	J, $\overline{K}$ inputs			20	μA
			$\overline{R}_D$, $\overline{S}_D$ inputs			40	μA
			CP inputs			20	μA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	J, $\overline{K}$ inputs			-0.4	mA
			$\overline{R}_D$, inputs			-0.8	mA
			$\overline{S}_D$ inputs			-0.8	mA
			CP inputs			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			4	8	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		25 40	ns ns
t_{PLH} t_{PHL}	Propagation delay Reset to output	Waveform 2		25 40	ns ns
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 2		25 40	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMIT		UNIT
			Min	Max	
$t_w(H)$	Clock pulse width (High)	Waveform 1	25		ns
$t_w(L)$	Clock pulse width (Low)	Waveform 1	15		ns
$t_w(L)$	Set or reset pulse width (Low)	Waveform 2	25		ns
t_s	Set-up time J or $\overline{K}$ to clock	Waveform 1	20		ns
t_h	Hold time J or $\overline{K}$ to clock	Waveform 1	5.0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		30 45	ns ns
t_{PLH} t_{PHL}	Propagation delay Reset to output	Waveform 2		30 45	ns ns
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 2		30 45	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[5]

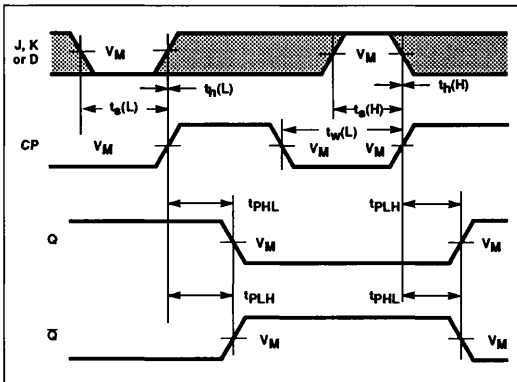
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		39 59	ns ns
t_{PLH} t_{PHL}	Propagation delay Reset to output	Waveform 2		39 59	ns ns
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 2		39 59	ns ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

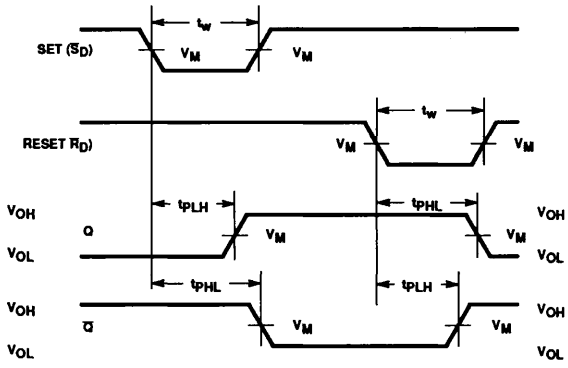
SYMBOL	PARAMETER	TEST CONDITIONS	LIMIT		UNIT
			Min	Max	
$t_w(H)$	Clock pulse width (High)	Waveform 1	25		ns
$t_w(L)$	Clock pulse width (Low)	Waveform 1	25		ns
$t_w(L)$	Set or reset pulse width (Low)	Waveform 2	25		ns
t_s	Set-up time J or $\overline{K}$ to clock	Waveform 1	25		ns
t_h	Hold time J or $\overline{K}$ to clock	Waveform 1	5.0		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



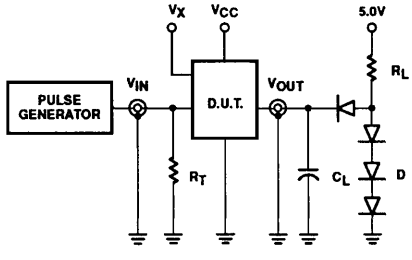
Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



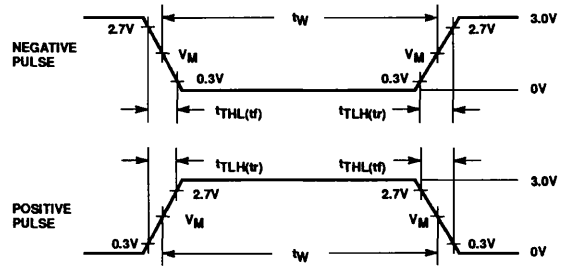
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths

NOTE: V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.