EDI 8417C
35/45/55
Monolithic

16Kx4 SRAM
CMOS, High Speed
Monolithic

The EDI8417C is a 65,536-Bit high speed CMOS Static RAM organized as 16Kx4.

The EDI8417C features fully static operation, requiring no external clocks or timing strobes, and equal access and cycle times.

The EDI8417C provides a chip enable function ($\overline{E}$) that can be used to place the device into a low power standby mode as well as an output enable function ($\overline{G}$) to eliminate bus contention. All inputs and outputs are TTL compatible and operate from a single 5V supply.

All EDI Military Components are compliant to MIL-STD-883C.

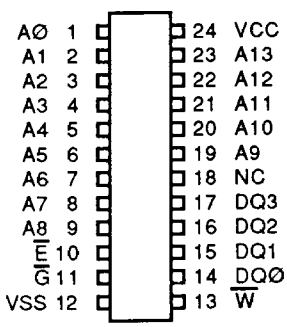
Features

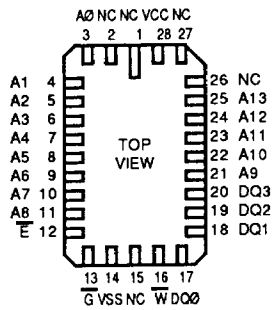
64K bit CMOS Static Random Access Memory
- Access Times of 35, 45, 55
- Fully Static, No Clocks
- Common Data Inputs and Outputs

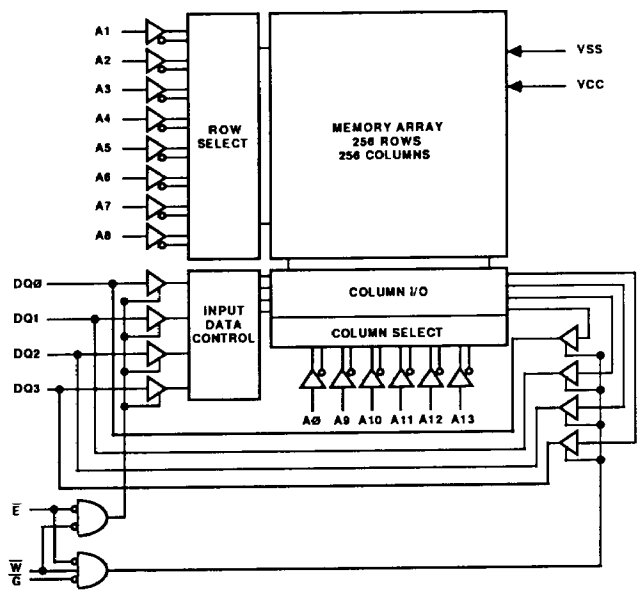
24 Pin DIP or 28 Pin LCC
- JEDEC Approved Pinout
- Output Enable to Control Bus Contention

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram







Pin Names

AØ-A13	Addres Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ3	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.3V to 7.0V
Operating Temperature TA (Ambient)	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature (Ambient/Ceramic)	-65°C to +150°C
Power Dissipation	1 Watts
Output Current	25mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	Ø	Ø	Ø	V
Input High Voltage	VIH	2.0	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

DC Electrical Characteristics

(TA = -55°C to +125°; VCC = 5.0V ± 10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{E}$ = VIL, II/O = ØmA Min Cycle	--	70	95	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$≥ VIH VIN ≤ VIL or VIN ≥ VIH	--	--	30	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC-O.2V VIN ≥VCC-0.2V or VIN≤0.2V	--	--	20	mA
Input Leakage Current	IIL	VIN = ØV to VCC	--	--	±5	µA
Output Leakage Current	IOL	V I/O = ØV to VCC $\overline{E}$ = VIH	--	--	±10	µA
Output High Voltage	VOH	IOH= -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL= 8.0mA	--	--	0.4	V

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	STANDBY	HIGH Z	ICC2, ICC3
H	L	H	READ	DOUT	ICC1
L	L	H	WRITE	HIGH Z	ICC1
X	L	L	OUTPUT DESELECT	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN = VCC or VSS)

Parameter		Sym	Max		Unit
			LCC	DIP	
Input Capacitance (Except D/Q Pins)		CI	6	10	pF
Capacitance Control (D/Q Pins)		CD/Q	8	12	pF

Note: These parameters are sampled, not 100% tested.

A.C. Test Conditions

Input Pulse Levels.....	VSS to 3.0V
Input Rise and Fall Times.....	5ns
Input and Output Timing Levels....	1.5V
Output Load.....	1 TTL, CL = 30pF (Note: For TEHQZ and TWLQZ, CL = 5pF)

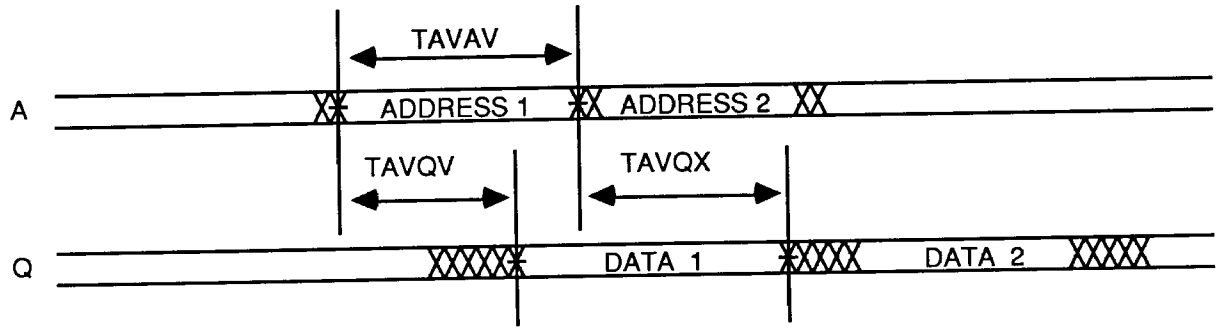
AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

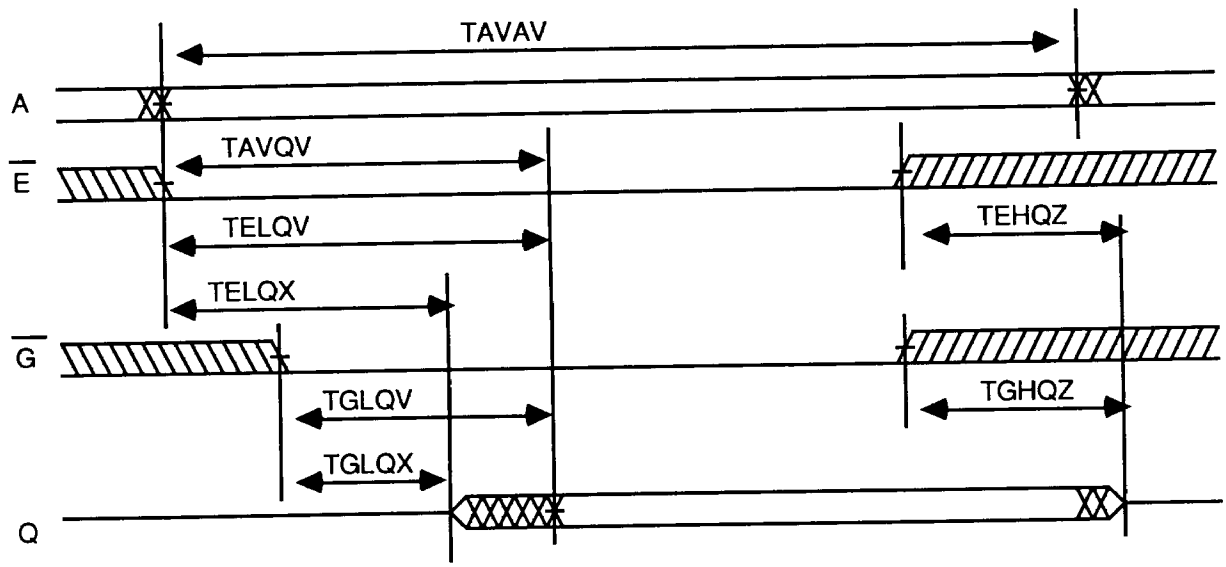
Parameter	Sym	35ns		45ns		55ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip Enable Access Time	TELQV		35		45		55	ns
Output Enable to Data Valid	TGLQV		20		20		25	ns
Output Hold from Address Change	TAVQX	3		3		3		ns
Output Enable to Output Active (1)	TGLQX	Ø		Ø		Ø		ns
Chip Enable to Output Low Z (1)	TELQX	3		3		3		ns
Chip Enable to Output in High Z (1)	TEHQZ		15		20		25	ns
Output Disable to Output Active (1)	TGHQZ		15		20		25	ns
Read Command Set-up Time	TWHEL	Ø		Ø		Ø		ns
Read Command Hold Time	TEHWL	Ø		Ø		Ø		ns
Chip Enable to Power Up (1)	TPU	Ø		Ø		Ø		ns
Chip Disable to Power Down (1)	TPD		35		45		55	ns

Note 1: Parameter guaranteed but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



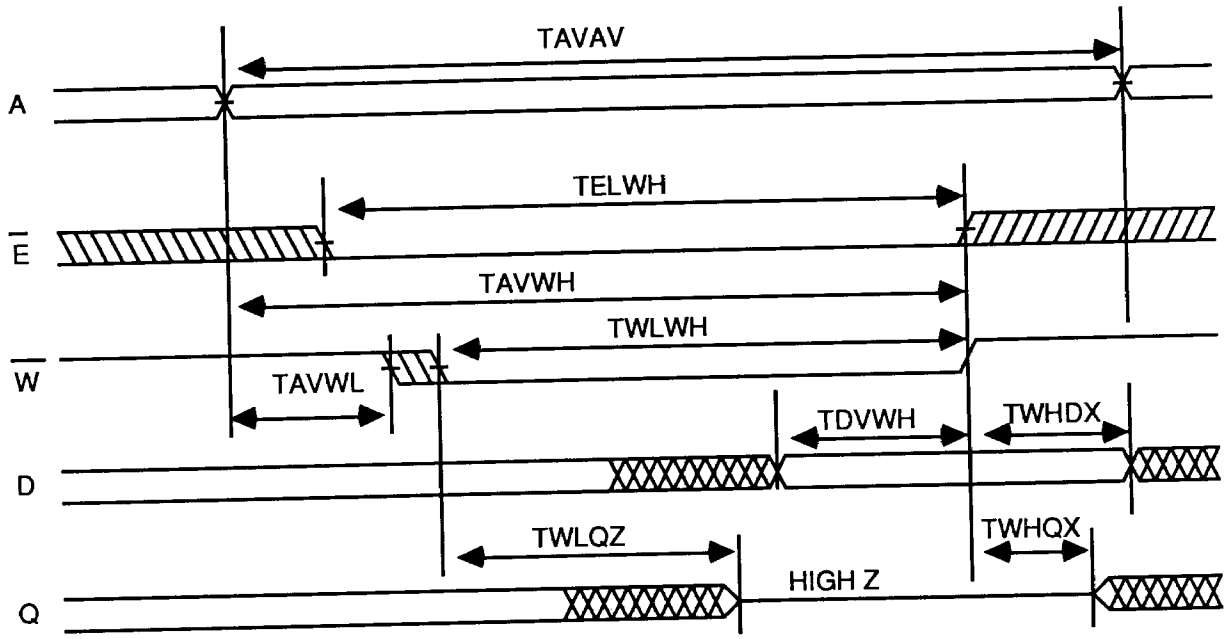
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

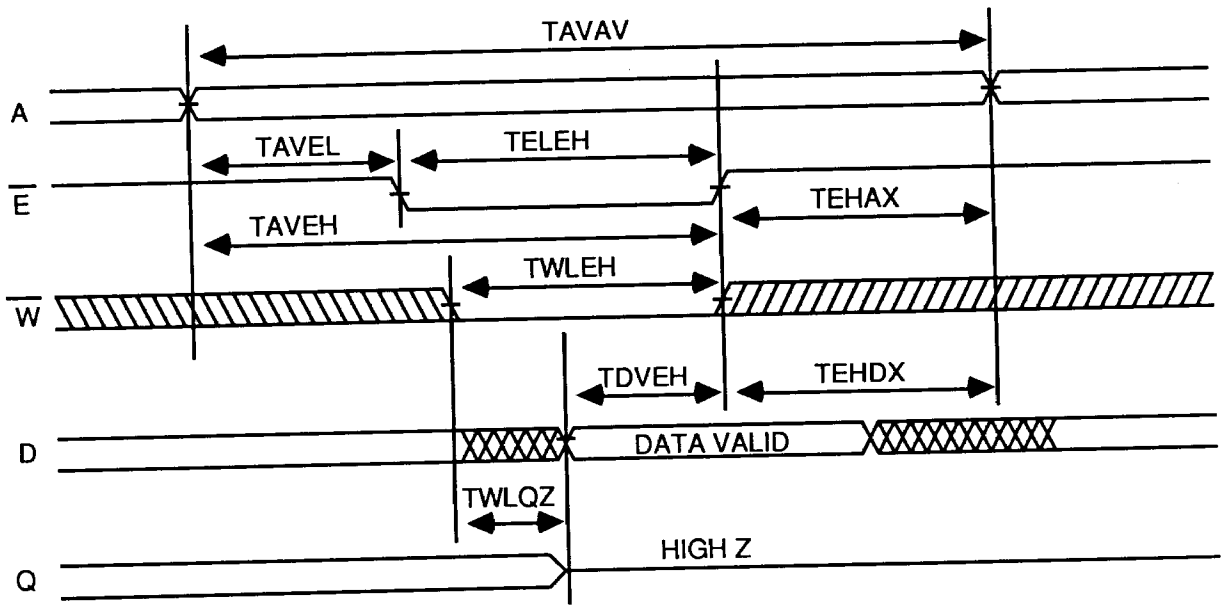
Parameter	Sym		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		ns
Chip Enable to End of Write	TELWH	$\overline{W}$	30		40		50		ns
	TWLEH	$\overline{E}$	30		40		50		ns
Address Setup Time	TAVWL	$\overline{W}$	Ø		Ø		Ø		ns
	TAVEL	$\overline{E}$	Ø		Ø		Ø		ns
Address Valid to End of Write	TAVWH	$\overline{W}$	30		40		50		ns
	TAVEH	$\overline{E}$	30		40		50		ns
Write Pulse Width	TWLWH	$\overline{W}$	30		40		50		ns
	TELEH	$\overline{E}$	30		40		50		ns
Write Recovery Time	TWHAX	$\overline{W}$	Ø		Ø		Ø		ns
	TEHAX	$\overline{E}$	Ø		Ø		Ø		ns
Data Hold Time	TWHDX	$\overline{W}$	Ø		Ø		Ø		ns
	TEHDX	$\overline{E}$	Ø		Ø		Ø		ns
Write to Output in High Z (1)	TWLQZ			15		20		25	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		25		ns
	TDVEH	$\overline{E}$	15		20		25		ns
Output Active from End of Write (1)	TWHQX		5		5		5		ns

Note 1: Parameter guaranteed but not tested.

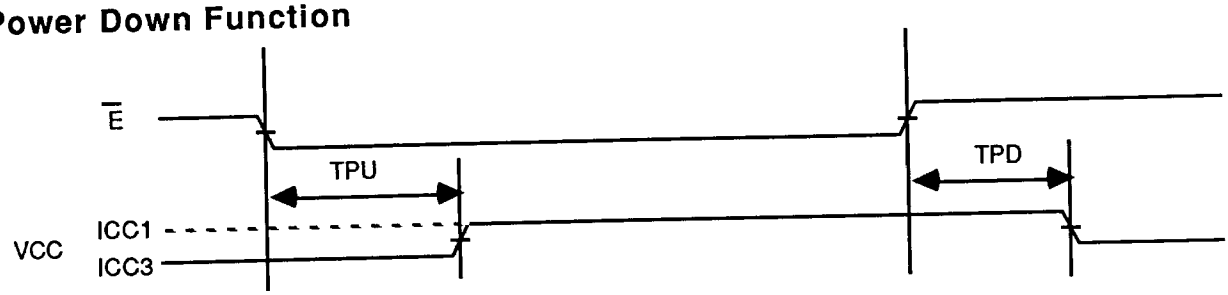
Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled

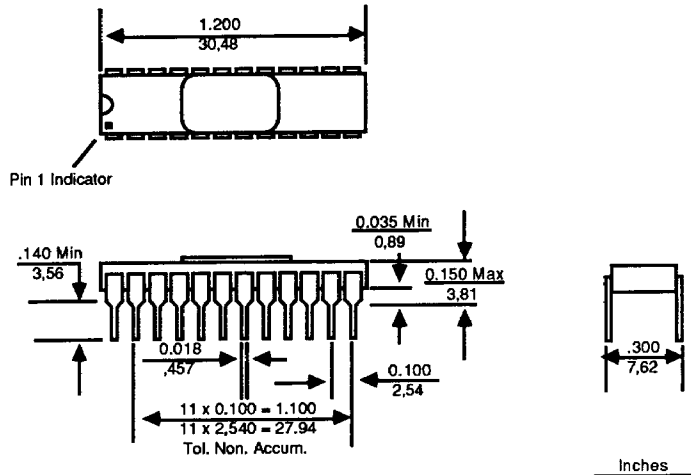


$\overline{E}$ Power Down Function

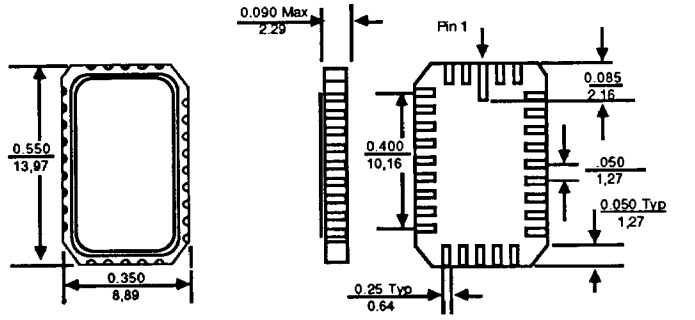


Package Description

24 Pin Dual-in-line Ceramic Package 300 Mils Wide



28 Pin Ceramic Leadless Chip Carrier



Ordering Information

Part No.	Speed (ns)	Package	Temp. Range
EDI8417C35QB	35	DIP	Military
EDI8417C45QB	45	DIP	Military
EDI8417C55QB	55	DIP	Military
EDI8417C35LB	35	LCC	Military
EDI8417C45LB	45	LCC	Military
EDI8417C55LB	55	LCC	Military
EDI8417C35QI	35	DIP	Industrial
EDI8417C45QI	45	DIP	Industrial
EDI8417C55QI	55	DIP	Industrial

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