FEATURES

- 4-bit synchronous counters
- Synchronously programmable
- Internal look-ahead counting
- Carry output for n-bit cascading
- Synchronous or asynchronous clear
- Advanced low-power Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883

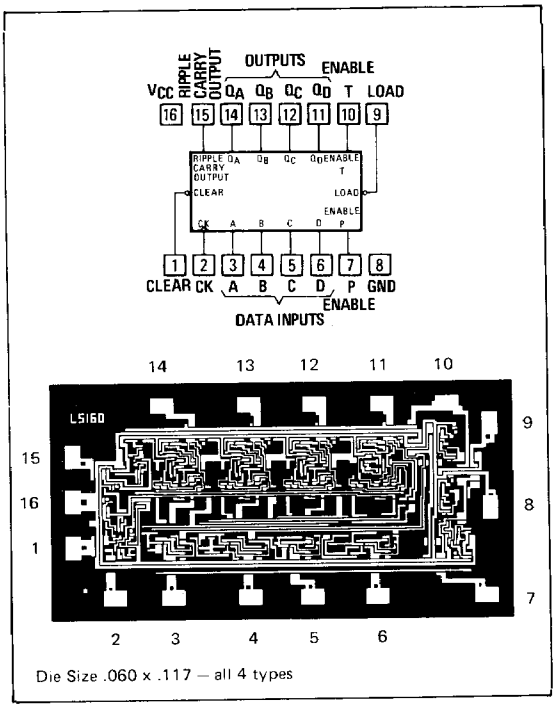
DESCRIPTION

The LS160, LS161, LS162 and LS163 synchronous, presettable counts have internal look-ahead carry and ripple carry output for high-speed counting applications. The LS160 and LS162 are decade counters and the LS161 and LS163 are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition.

The LS160 and LS161 feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The LS162 and LS163 have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection.

PIN-OUT DIAGRAM



Die Size .060 x .117 — all 4 types

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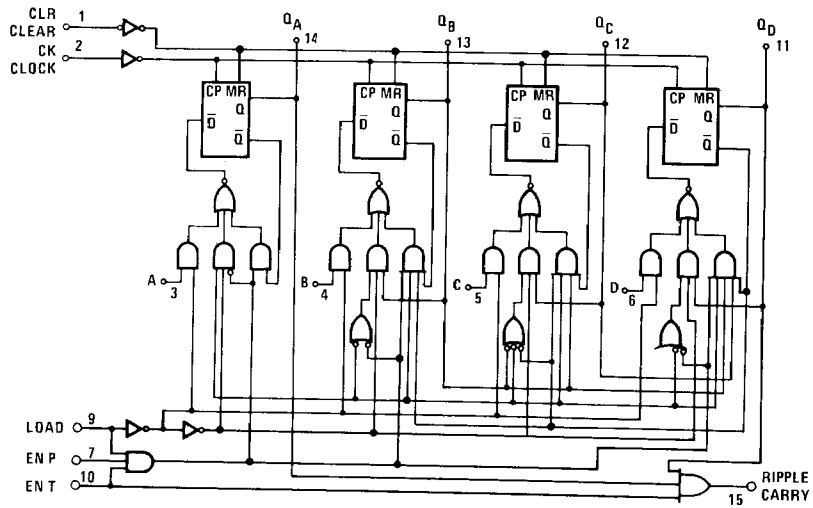
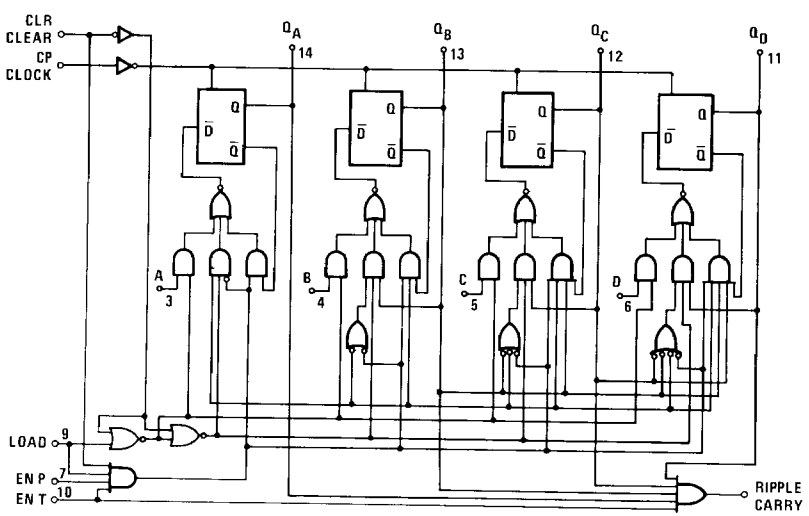
LOGIC DIAGRAMS

LS160 Synchronous Decade Counter



LS162 synchronous decade counters are similar; however, the clear is synchronous as shown for the LS163 binary counters.

LS163 SYNCHRONOUS BINARY COUNTER



LS161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the LS160 decade counters.

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5.0	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figures 3 and 4)	Data inputs A, B, C, D	0			0			ns
	Enable P or T	20			20			
	Load	20			20			
	Clear◊	20			20			
Hold time, t_{hold}	Data inputs A, B, C, D	25¶			25			ns
	Other inputs	10¶			10			
Operating free-air temperature, T_A		-55		125	0		70	°C

◊ This applies only for LS162 and LS163, which have synchronous clear inputs.

¶ The minimum hold time is as specified or as long as the clock input takes to rise from 0.8 V to 2 V, whichever is longer.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max,	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	Data or enable P	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	Load, clock, or enable T					0.2			0.2	
	Clear (LS160,161)					0.1			0.1	
	Clear (LS162,163)					0.2			0.2	
I_{IH}	Data or enable P	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Load, clock, or enable T					40			40	
	Clear (LS160,161)					20			20	
	Clear (LS162,163)					40			40	
I_{IL}	Data or enable P	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
	Load, clock, or enable T					-0.8			-0.8	
	Clear(LS160,161)					-0.4			-0.4	
	Clear(LS162,163)					-0.8			-0.8	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CCH}		V_{CC}=MAX, See Note 1			18	31		18	31	mA
I_{CCL}		V_{CC}=MAX, See Note 2			19	32		19	32	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

NOTES:

1. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
2. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1 and 2 and Notes 3 and 4 and Fig. A, page 2-174)												
f_{max}						30	40					MHz
t_{PLH}	Clock	Ripple carry		28	39		25	35		28	39	ns
t_{PHL}				23	39		20	35		23	39	
t_{PLH}	Clock (load input high)	Any Q		13	22		10	18		13	22	ns
t_{PHL}				18	24		15	20		18	24	
t_{PLH}	Clock (load input low)	Any Q		13	22		10	18		13	22	ns
t_{PHL}				18	24		14	20		18	24	
t_{PLH}	Enable T	Ripple carry		18	25		15	20		18	25	ns
t_{PHL}				13	18		9	14		13	18	
t_{PHL}	Clear	Any Q		17	32		14	28		17	32	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1 and 2 and Notes 3 and 4 and Fig. A, page 2-174)												
t_{PLH}	Clock	Ripple carry		31	44		28	39		31	44	ns
t_{PHL}				26	44		23	39		26	44	
t_{PLH}	Clock (load input high)	Any Q		16	27		13	22		16	27	ns
t_{PHL}				21	29		18	24		21	29	
t_{PLH}	Clock (load input low)	Any Q		16	27		13	22		16	27	ns
t_{PHL}				21	29		17	24		21	29	
t_{PLH}	Enable T	Ripple carry		21	30		18	24		21	30	ns
t_{PHL}				16	23		12	18		16	23	
t_{PHL}	Clear	Any Q		20	37		17	32		20	37	ns

NOTES:

3. Propagation delay for clearing is measured from the clear input for the LS160 and LS161 or from the clock input transition for the LS162 and LS163.
4. AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

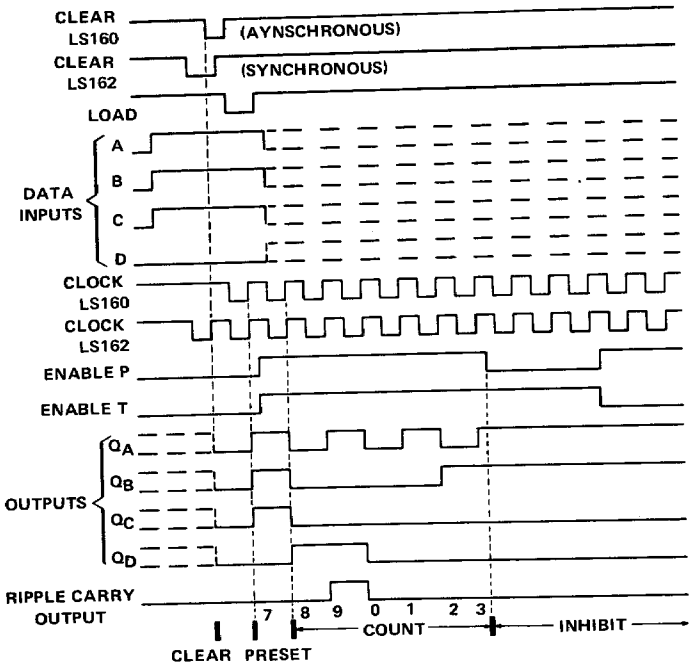


FIGURE 1

LS160, LS162

Illustrated below is the following sequence:
1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

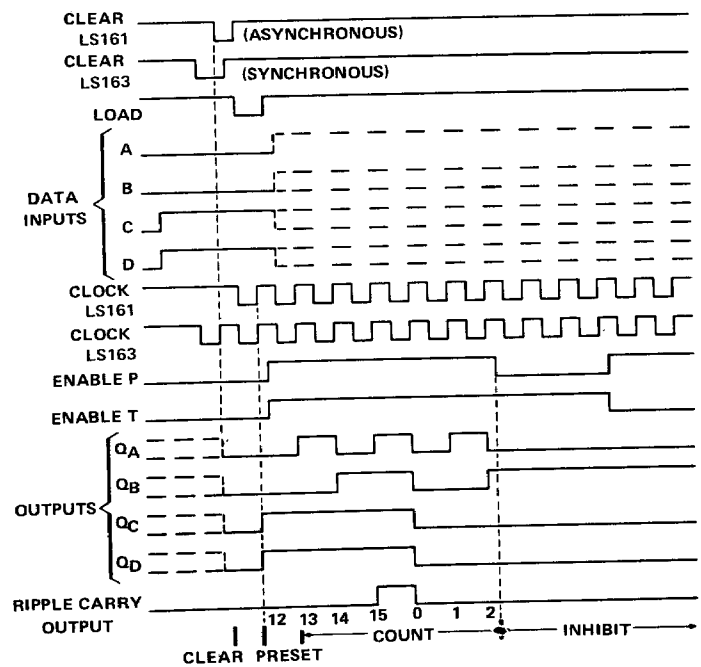


FIGURE 2

LS161, LS163

Illustrated below is the following sequence:
1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen; fourteen fifteen, zero, one, and two
4. Inhibit

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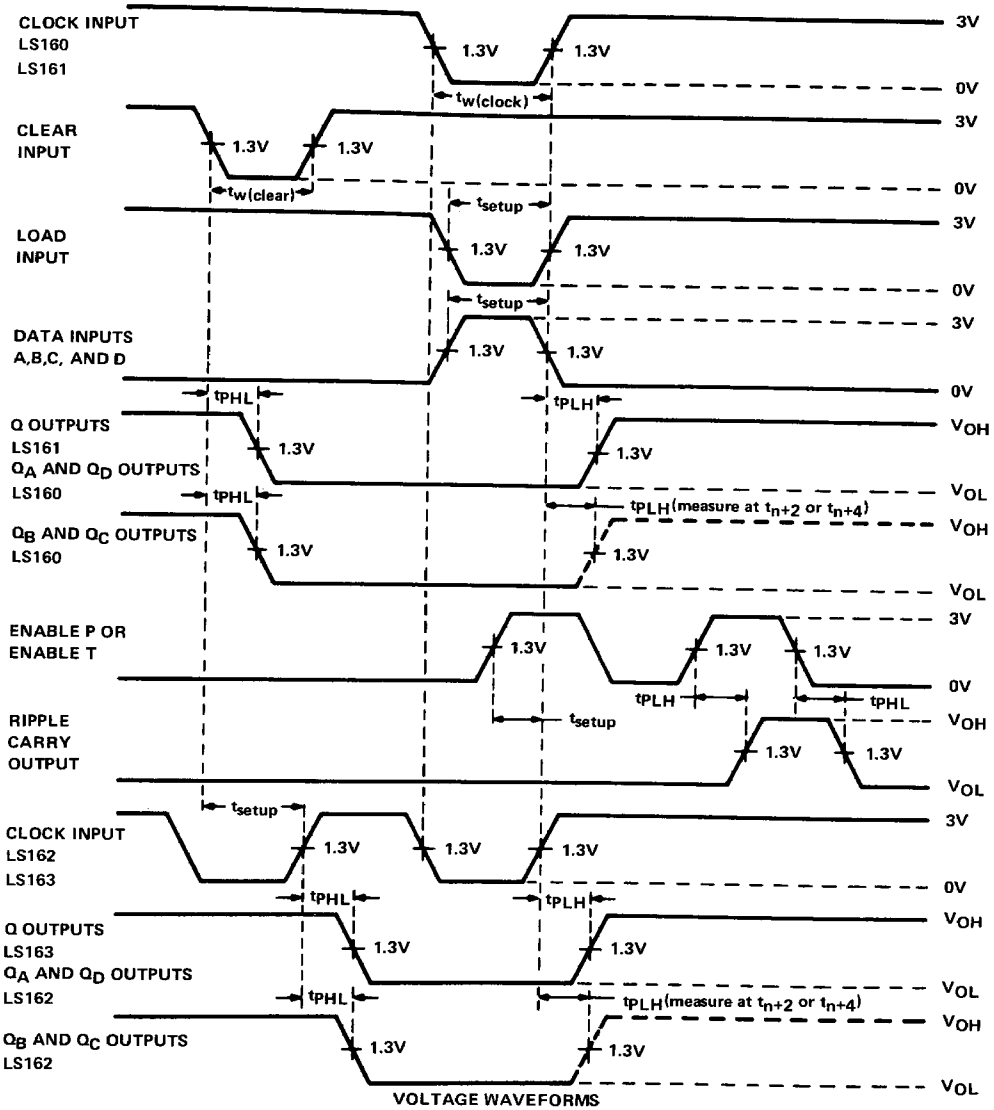
FIGURE 1

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

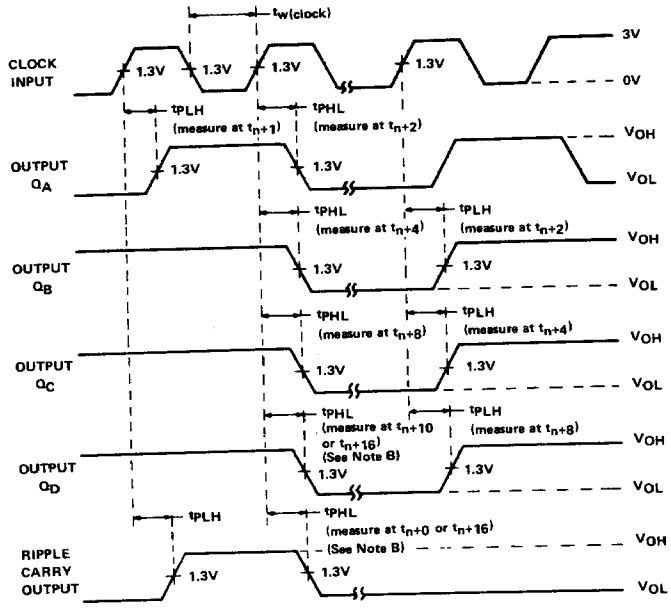
NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\,\Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at $t_n = 0$.

FIGURE 4

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

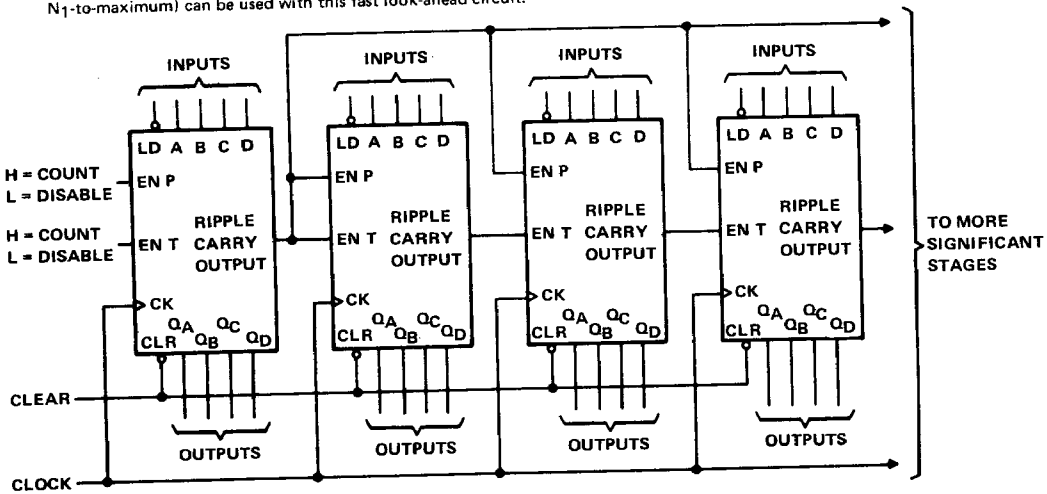
A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$: $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_d and carry are tested at t_{n+10} LS160, LS162, and at t_{n+16} for LS161, LS163 where t_n is the bit time when all outputs are low.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The LS160 or LS162 will count in BCD and the LS163 will count in binary. Virtually any count mode (modulo-N, N_1-to N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



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