SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SDLS068A – DECEMBER 1972 – REVISED OCTOBER 2001

'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

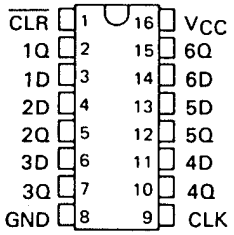
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

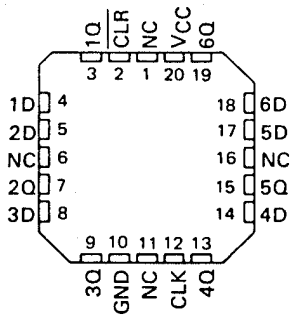
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

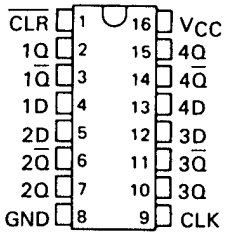
SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE
SN74174 . . . N PACKAGE
SN74LS174, SN74S174 . . . D OR N PACKAGE
(TOP VIEW)



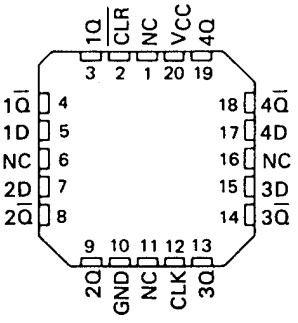
SN54LS174, SN54S174 . . . FK PACKAGE
(TOP VIEW)



SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175 . . . N PACKAGE
SN74LS175, SN74S175 . . . D OR N PACKAGE
(TOP VIEW)



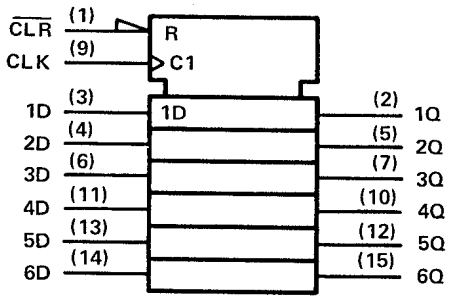
SN54LS175, SN54S175 . . . FK PACKAGE
(TOP VIEW)



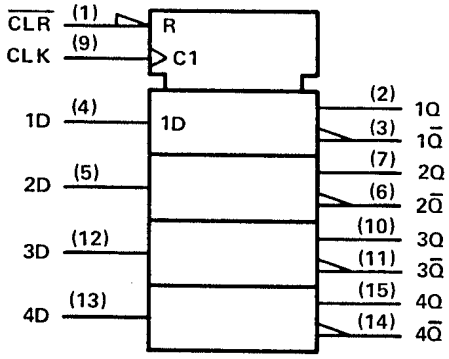
NC – No internal connection

logic symbols†

'174



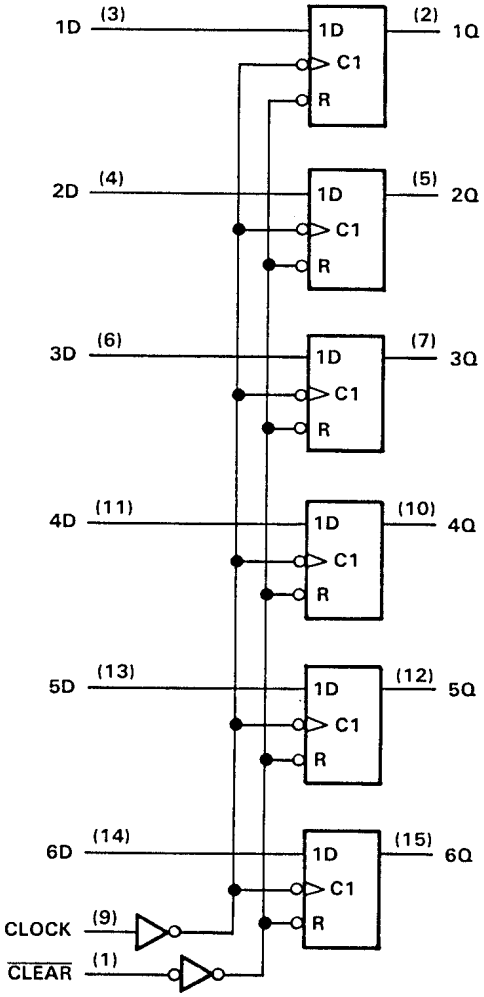
'175



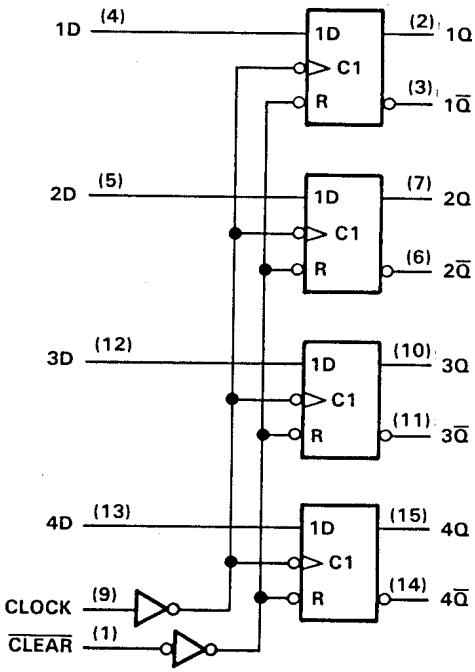
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagrams (positive logic)

'174, 'LS174, 'S174



'175, 'LS175, 'S175

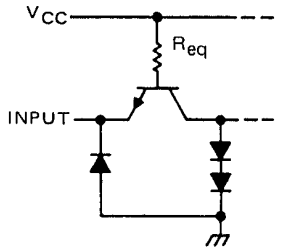


Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

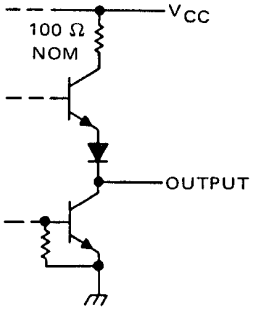
SN54174, SN54175, SN74174, SN74175

EQUIVALENT OF ALL INPUTS



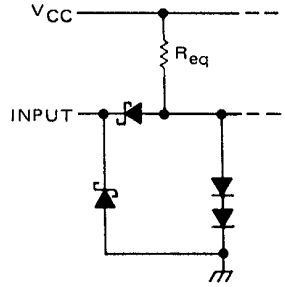
Clock, D: R_{eq} = 8 kΩ NOM
$\overline{\text{Clear}}$: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



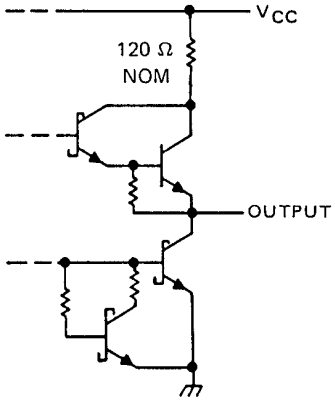
SN54LS174, SN54LS175, SN74LS174, SN74LS175

EQUIVALENT OF ALL INPUTS



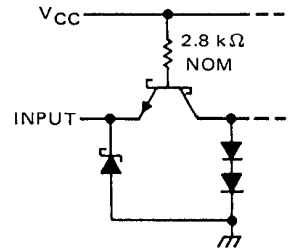
Clock: R_{eq} = 23 kΩ NOM
$\overline{\text{Clear}}$, D: R_{eq} = 28 kΩ NOM

TYPICAL OF ALL OUTPUTS

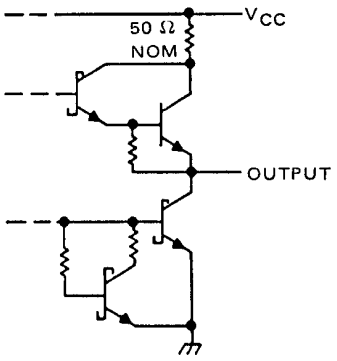


SN54S174, SN54S175, SN74S174, SN74S175

EQUIVALENT OF ALL INPUTS



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54174, SN54175 Circuits . . . . . −55°C to 125°C
SN74174, SN74175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54174, SN54175			SN74174, SN74175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54′	−20		−57	mA
			SN74′	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	′174		45	65	mA
			′175		30	45	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 3	25	35		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear (SN54175, SN74175 only)			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			24	35	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS174, SN54LS175 Circuits . . . . . −55°C to 125°C
SN74LS174, SN74LS175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'LS174		16	26		16	26	mA
			'LS175		11	18		11	18	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	'LS174			'LS175			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{max} Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Note 3	30	40		30	40		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clear						20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear			23	35		20	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			20	30		13	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			21	30		16	25	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S174, SN54S175 Circuits . . . . . −55°C to 125°C
SN74S174, SN74S175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S174, SN54S175			SN74S174, SN74S175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		75	0		75	MHz
Pulse width, t_w	Clock	7			7			ns
	Clear	10			10			
Setup time, t_{su}	Data input	5			5			ns
	Clear inactive-state	5			5			
Data hold time, t_h		3			3			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'174		90	144	mA
			'175		60	96	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω, See Note 3	75	110		MHz
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output from clear (SN54S175, SN74S175 only)			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			13	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL}	Propagation time, high-to-low-level output from clock			11.5	17	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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Post Office Box 655303
Dallas, Texas 75265

SN74LS174, Hex D-Type Flip-Flops With Clear

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS174	SN74LS174
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-0.4/8
Output	2S	2S
No. of Bits	6	6
Static Current		26
th (ns)		5
tpd max (ns)		30
tsu (ns)		20

FEATURES

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- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

DESCRIPTION

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These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74ls174.pdf (318 KB,Rev.A) (Updated: 10/12/2001)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Designing with the SN54/74LS123 (Rev. A) (SDLA006A - Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74LS174D	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.34	40	560	>10k | 19 Sep	4 WKS	Avnet | AMERICA	>1k	BUY NOW
								1114 | 03 Oct				
								>10k | 10 Oct				
								>10k | 17 Oct				
SN74LS174DR	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.36	2500	7500	3614 | 03 Oct	4 WKS	Avnet | AMERICA	>1k	BUY NOW
								>10k | 10 Oct				
								>10k | 17 Oct				
SN74LS174J	OBSOLETE	CDIP (J) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available			
SN74LS174N	ACTIVE	PDIP (N) | 16	0 TO 70	View Contents	1KU | 0.27	25	N/A*	350 | 23 Sep	4 WKS	Avnet | AMERICA	>1k	BUY NOW
								1800 | 24 Sep		DigiKey | AMERICA	789	BUY NOW
								2980 | 25 Sep				

								6935 | 02 Oct						
								>10k | 04 Oct						
SN74LS174N3	OBSOLETE	PDIP (N) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available				
SN74LS174NSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.27	2000	N/A*	>10k | 04 Oct	4 WKS					
								2302 | 11 Oct						
								>10k | 18 Oct						
								1500 | 19 Nov						
								500 | 21 Nov						

Table Data Updated on: 9/26/2002

SN74S174, Hex D-Type Flip-Flops With Clear

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54S174	SN74S174
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-1/20
Output	2S	2S
No. of Bits	6	6
Static Current		144
th (ns)		3
tpd max (ns)		17
tsu (ns)		5

FEATURES

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- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

DESCRIPTION

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These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74s174.pdf (318 KB,Rev.A) (Updated: 10/12/2001)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74S174J	OBSOLETE	CDIP (J) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available			
SN74S174N	ACTIVE	PDIP (N) | 16	0 TO 70	View Contents	1KU | 0.59	25	N/A*	7949 | 04 Oct	5 WKS	Avnet | AMERICA	>1k	BUY NOW
								>10k | 11 Oct				
SN74S174N3	OBSOLETE	PDIP (N) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available			
SN74S174NSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.59	2000	N/A*	7909 | 04 Oct	5 WKS			
								2302 | 11 Oct				
								>10k | 18 Oct				

Table Data Updated on: 9/26/2002

PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG | APPLICATION NOTES | RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

SN74S175, Quadruple D-Type Flip-Flops With Clear

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54S175	SN74S175
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-1/20
Output	2S	2S
No. of Bits	4	4
Static Current		96
th (ns)		3
tpd max (ns)		17
tsu (ns)		5

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- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

DESCRIPTION

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These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: sn74s175.pdf (318 KB,Rev.A) (Updated: 10/12/2001)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
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PRICING/AVAILABILITY/PKG

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SN74S175D	ACTIVE	SOP (D) | 16	0 TO 70	View Contents	1KU | 0.60	40	N/A*	1800 | 03 Oct	5 WKS			
								>10k | 10 Oct				
SN74S175DR	OBSOLETE	SOP (D) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available			
SN74S175N	ACTIVE	PDIP (N) | 16	0 TO 70	View Contents	1KU | 0.59	25	N/A*	>10k | 04 Oct	5 WKS	Avnet | AMERICA	249	BUY NOW
								>10k | 11 Oct				
SN74S175N3	OBSOLETE	PDIP (N) | 16	0 TO 70	View Contents	1KU |		N/A*		Not Available			
SN74S175NSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.59	2000	N/A*	>10k | 04 Oct	5 WKS			
								2302 | 11 Oct				
								>10k | 18 Oct				

Table Data Updated on: 9/26/2002