IS62LV2568L
IS62LV2568LL

256K x 8 LOW POWER and LOW Vcc CMOS STATIC RAM

ADVANCE INFORMATION
FEBRUARY 1999

FEATURES

- Access times of 70 ns, 85 ns, and 100 ns
- Low active power: 126 mW (max, L, LL)
- Low standby power: 36 µW (max, L) and 7.2 µW (max, LL) CMOS standby
- Low data retention voltage: 2V (min.)
- Available in Low Power (-L) and Ultra-Low Power (-LL)
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- TTL compatible inputs and outputs
- Single 2.7V to 3.6V power supply

DESCRIPTION

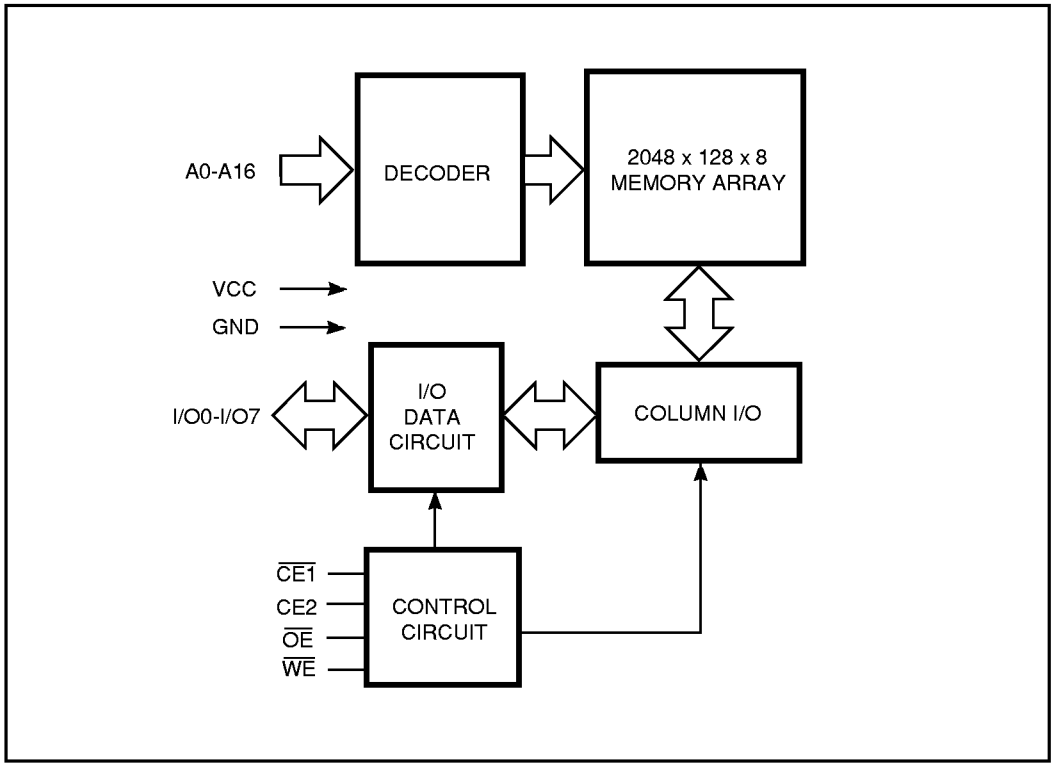
The *ISSI* IS62LV2568L and IS62LV2568LL are low power and low Vcc, 262,144-word by 8-bit CMOS static RAMs. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

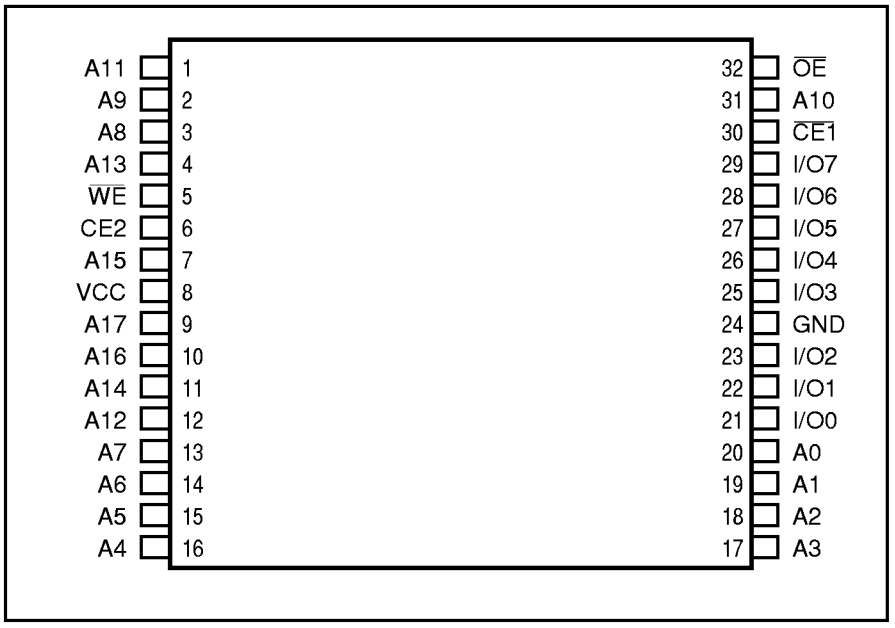
The IS62LV2568L and IS62LV2568LL are available in 32-pin TSOP (Type I) and STSOP (Type I).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

32-Pin TSOP (Type I), STSOP (Type I)



PIN DESCRIPTIONS

A0-A17	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
Vcc	Power
GND	Ground

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	–40°C to +85°C	2.7V to 3.6V

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
V_{CC}	Vcc related to GND	–0.3 to +4.6	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	0.7	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.2	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage(1)		–0.3	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	–1	1	µA

Note:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

IS62LV2568L POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-70 L ns Min.	-70 L ns Max.	-85 L ns Min.	-85 L ns Max.	-100 L ns Min.	-100 L ns Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., CE = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	55 —	— —	45 65	— —	35 55	mA
$I_{SB}1$	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, CE1 ≥ V_{IH} or CE2 ≤ V_{IL}, f = 0	Com. Ind.	— —	300 —	— —	300 500	— —	300 500	µA
$I_{SB}2$	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0 CE1 ≥ V_{CC} – 0.2V, CE2 ≤ 0.2V, or V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V	Com. Ind.	— —	10 —	— —	10 15	— —	10 15	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IS62LV2568LL POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-70 LL ns Min.	-70 LL ns Max.	-85 LL ns Min.	-85 LL ns Max.	-100 LL ns Min.	-100 LL ns Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., CE = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	55 —	— —	45 65	— —	35 55	mA
$I_{SB}1$	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, CE1 ≥ V_{IH} or CE2 ≤ V_{IL}, f = 0	Com. Ind.	— —	300 —	— —	300 500	— —	300 500	µA
$I_{SB}2$	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., f = 0 CE1 ≥ V_{CC} – 0.2V, CE2 ≤ 0.2V, or V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V	Com. Ind.	— —	2 —	— —	2 5	— —	2 5	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-70 Min.	-70 Max.	-85 Min.	-85 Max.	-100 Min.	-100 Max.	Unit
t_{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	ns
t_{OHA}	Output Hold Time	10	—	15	—	15	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	70	—	85	—	100	ns
t_{ACE2}	CE2 Access Time	—	70	—	85	—	100	ns
t_{DOE}	$\overline{OE}$ Access Time	—	35	—	45	—	50	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	25	0	25	0	30	ns
t_{LZCE1}[2]	$\overline{CE1}$ to Low-Z Output	10	—	10	—	10	—	ns
t_{LZCE2}[2]	CE2 to Low-Z Output	10	—	10	—	10	—	ns
t_{HZCE}[2]	$\overline{CE1}$ or CE2 to High-Z Output	0	25	0	25	0	30	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

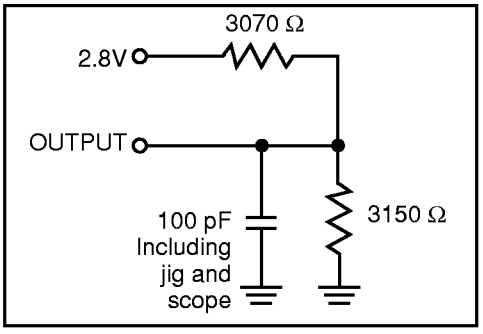


Figure 1

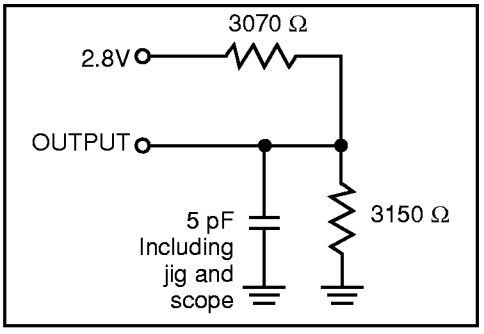
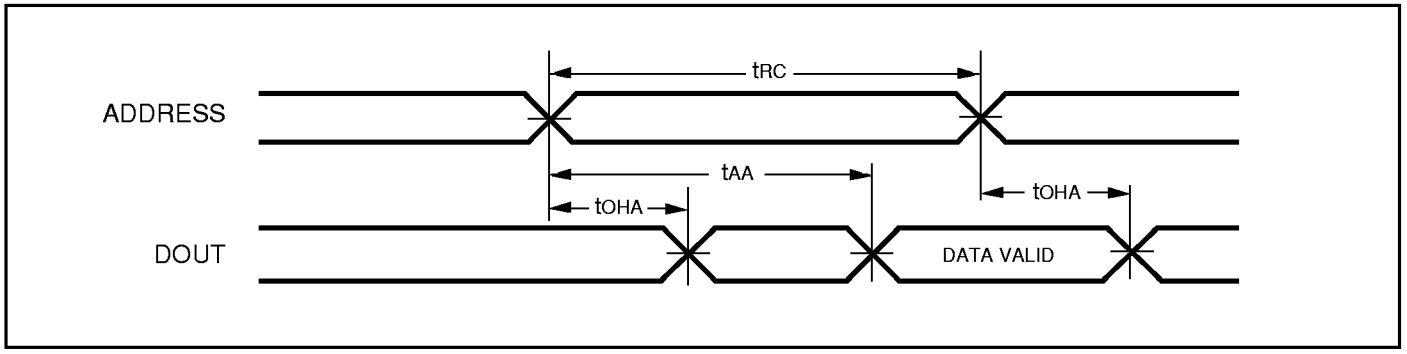


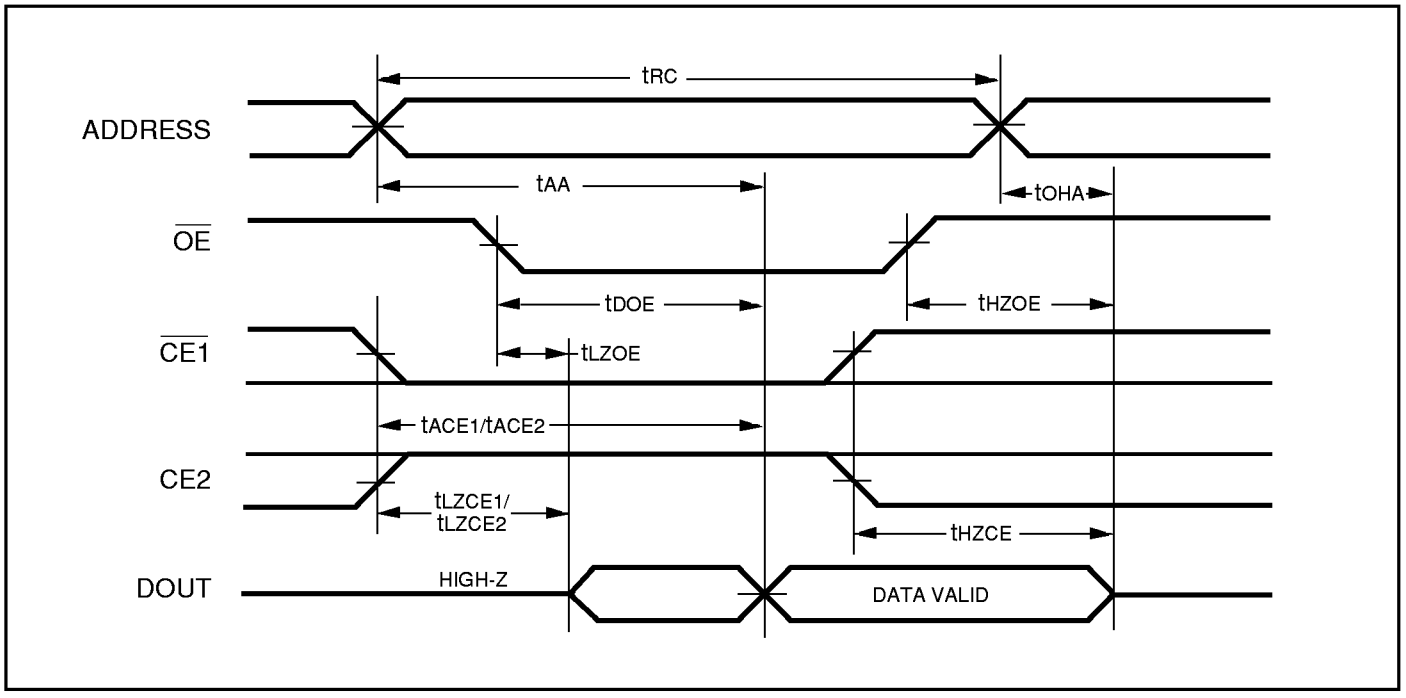
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

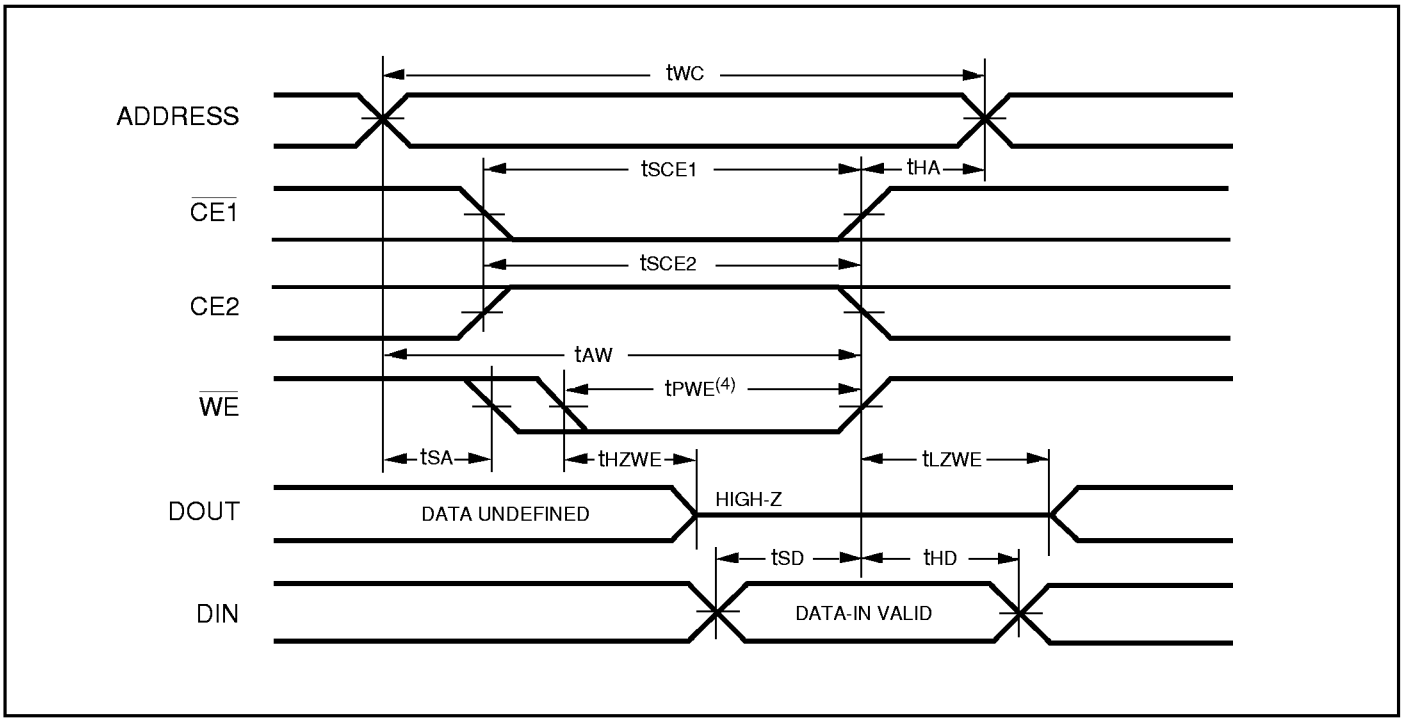
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range, Standard and Low Power)

Symbol	Parameter	-70 Min.	-70 Max.	-85 Min.	-85 Max.	-100 Min.	-100 Max.	Unit
t_{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t_{SCE1}	$\overline{CE1}$ to Write End	65	—	70	—	80	—	ns
t_{SCE2}	CE2 to Write End	65	—	70	—	80	—	ns
t_{AW}	Address Setup Time to Write End	65	—	70	—	80	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	55	—	60	—	70	—	ns
t_{SD}	Data Setup to Write End	30	—	35	—	40	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	0	25	0	25	0	30	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

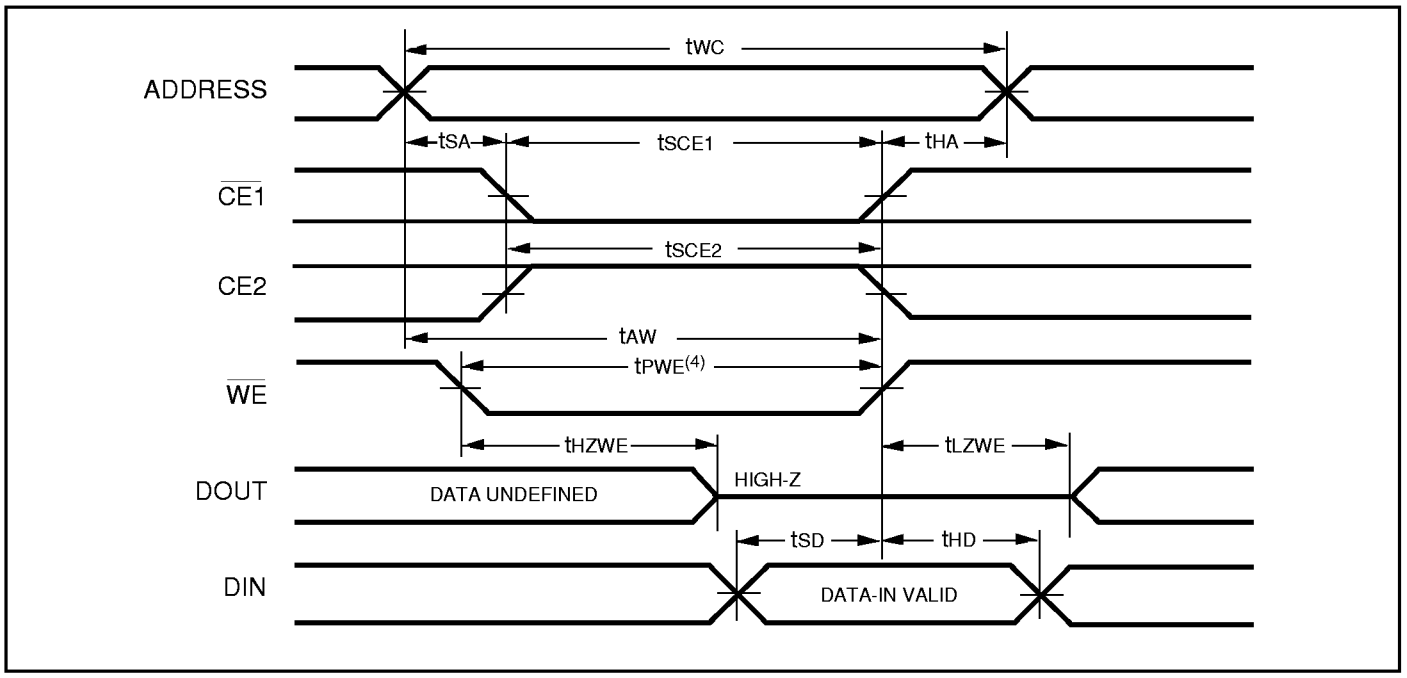
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 Controlled)[1,2]



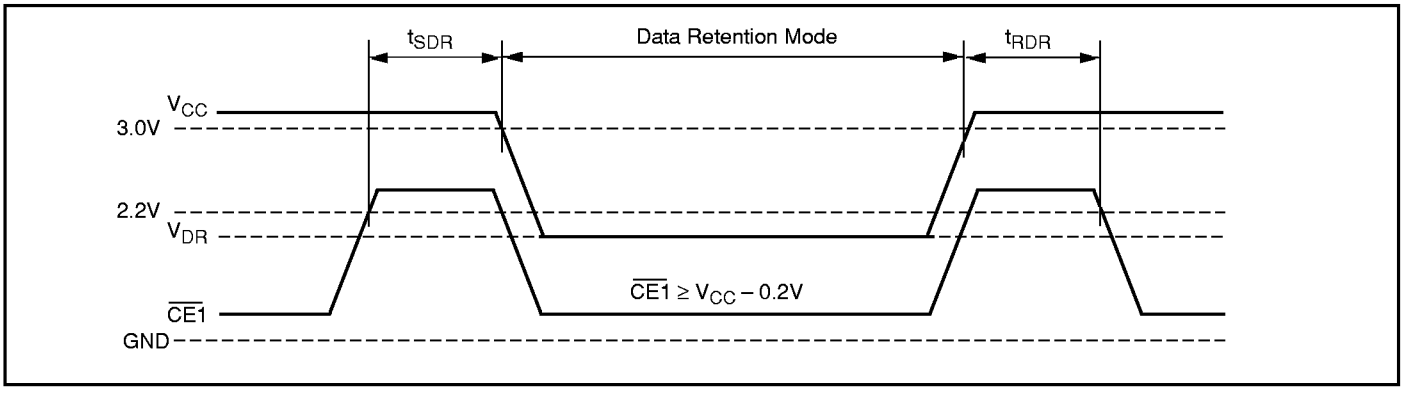
Notes:

1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

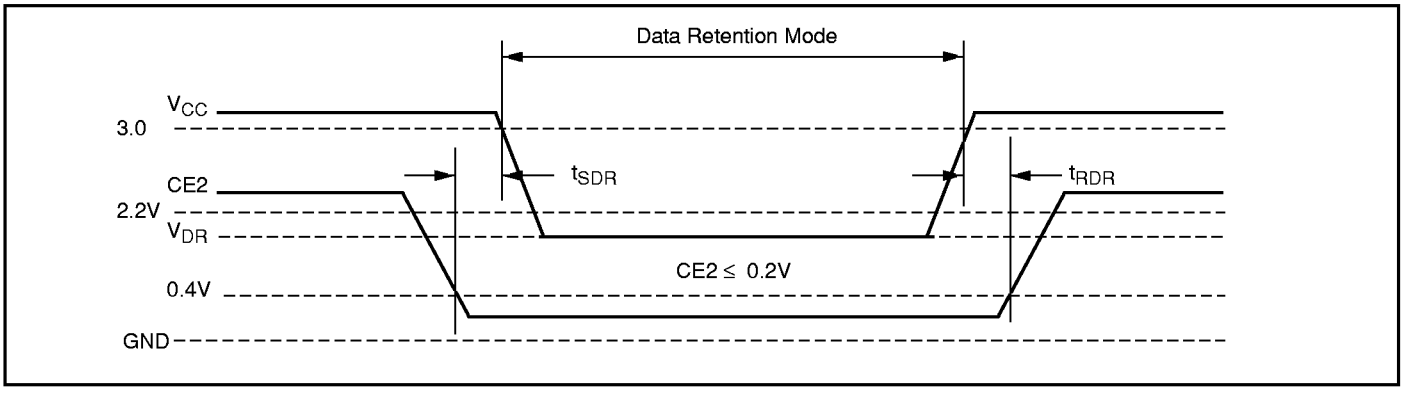
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform		2.0	3.6	V
I_{DR}	Data Retention Current	Vcc = 2.0V, $\overline{CE1} \geq$ Vcc – 0.2V	Com. (-L)	—	10	µA
			Com. (-LL)	—	2	µA
			Ind. (-L)	—	15	µA
			Ind. (-LL)	—	5	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



DATA RETENTION WAVEFORM (CE2 Controlled)



IS62LV2568L
ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS62LV2568L-70T	TSOP, Type I
70	IS62LV2568L-70H	STSOP, Type I
85	IS62LV2568L-85T	TSOP, Type I
85	IS62LV2568L-85H	STSOP, Type I
100	IS62LV2568L-100T	TSOP, Type I
100	IS62LV2568L-100H	STSOP, Type I

IS62LV2568L
ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS62LV2568L-70TI	TSOP, Type I
70	IS62LV2568L-70HI	STSOP, Type I
85	IS62LV2568L-85TI	TSOP, Type I
85	IS62LV2568L-85HI	STSOP, Type I
100	IS62LV2568L-100TI	TSOP, Type I
100	IS62LV2568L-100HI	STSOP, Type I

IS62LV2568LL
ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS62LV2568LL-70T	TSOP, Type I
70	IS62LV2568LL-70H	STSOP, Type I
85	IS62LV2568LL-85T	TSOP, Type I
85	IS62LV2568LL-85H	STSOP, Type I
100	IS62LV2568LL-100T	TSOP, Type I
100	IS62LV2568LL-100H	STSOP, Type I

IS62LV2568LL
ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS62LV2568LL-70TI	TSOP, Type I
70	IS62LV2568LL-70HI	STSOP, Type I
85	IS62LV2568LL-85TI	TSOP, Type I
85	IS62LV2568LL-85HI	STSOP, Type I
100	IS62LV2568LL-100TI	TSOP, Type I
100	IS62LV2568LL-100HI	STSOP, Type I

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