

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

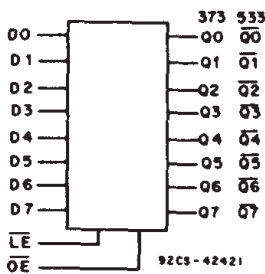
Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533



Data sheet acquired from Harris Semiconductor  
SCHS289



FUNCTIONAL DIAGRAM

## Octal Transparent Latch, 3-State

CD54/74AC/ACT373 - Non-Inverting  
CD54/74AC/ACT533 - Inverting

**Type Features:**

- Buffered inputs
- Typical propagation delay:  
4.3 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA-CD54/74AC373 and CD54/74AC533 and the CD54/74ACT373 and CD54/74ACT533 octal transparent 3-state latches use the RCA ADVANCED CMOS technology. The outputs are transparent to the inputs when the Latch Enable ( $\overline{LE}$ ) is HIGH. When the Latch Enable ( $\overline{LE}$ ) goes LOW, the data is latched. The Output Enable ( $\overline{OE}$ ) controls the 3-state outputs. When the Output Enable ( $\overline{OE}$ ) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD74AC/ACT373 and CD74AC/ACT533 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT373 and CD54AC/ACT533, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

**Family Features:**

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

Output Enable	Latch Enable	Data	AC/ACT373 Output	AC/ACT533 Output
L	H	H	H	L
L	H	L	L	H
L	L	I	L	H
L	L	h	H	L
H	X	X	Z	Z

Note:

- L = Low voltage level
- H = High voltage level
- I = Low voltage level one set-up time prior to the high to low latch enable transition
- h = High voltage level one set-up time prior to the high to low latch enable transition.
- X = Don't Care
- Z = High Impedance State

This data sheet is applicable to the CD54/74AC373, CD54/74ACT373, and CD54ACT533. The CD74AC533 and CD74ACT533 were not acquired from Harris Semiconductor.

# Technical Data

## CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	.....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	.....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	.....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	.....	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	.....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	.....	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	.....	$+300^\circ\text{C}$

\*For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.

### RECOMMENDED OPERATING CONDITIONS:

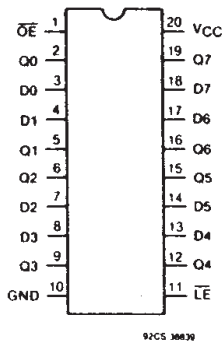
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V
DC Input or Output Voltage, $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

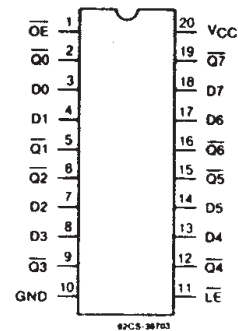
\*Unless otherwise specified, all voltages are referenced to ground.

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### TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC373, CD54/74ACT373



CD54/74AC533, CD54/74ACT533

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	ACT373	ACT533
OE	0.87	0.87
Dn	0.5	0.5
LE	0.8	0.8

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
LE Pulse Width	t <sub>w</sub>	1.5	44	—	50	—	ns
		3.3*	4.9	—	5.6	—	
		5†	3.5	—	4	—	
Setup Time Data to LE	t <sub>su</sub>	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Hold Time Data to LE	t <sub>h</sub>	1.5	33	—	38	—	ns
		3.3	3.7	—	4.2	—	
		5	2.6	—	3	—	

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn 373	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	96	—	106	ns
		3.3*	3.1	10.8	3	11.9	
		5†	2.2	7.7	2.1	8.5	
533	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	119	—	131	ns
		3.3	3.8	13.4	3.7	14.7	
		5	2.7	9.5	2.6	10.5	
LE on Qn 373	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	136	—	150	ns
		3.3	4.3	15.2	4.2	16.8	
		5	3.1	10.9	3	12	
533	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
Output Enable Times	t <sub>PZL</sub> t <sub>PZH</sub>	1.5	—	119	—	131	ns
		3.3	4.1	14.4	4	15.8	
		5	2.7	9.5	2.6	10.5	
Output Disable Times	t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5	—	131	—	144	ns
		3.3	3.7	13.1	3.6	14.4	
		5	3	10.5	2.9	11.5	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	63 Typ.		63 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per latch.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

**PREREQUISITE FOR SWITCHING: ACT Series**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
LE Pulse Width	t <sub>w</sub>	5†	3.6	—	4	—	ns
Setup Time Data to LE	t <sub>su</sub>	5	2	—	2	—	ns
Hold Time Data to LE	t <sub>h</sub>	5	2.7	—	3	—	ns

†5 V: min. is @ 4.5 V

**SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn 373	t <sub>PLH</sub>	5†	2.7	9.5	2.6	10.4	ns
	t <sub>PHL</sub>		3	10.4	2.9	11.4	
LE to Qn 373 533	t <sub>PLH</sub> t <sub>PHL</sub>	5	3.1	11.4	3	12.5	ns
Output Enable Times	t <sub>PZL</sub> t <sub>PZH</sub>	5	3.5	12.3	3.4	13.5	ns
Output Disable Times	t <sub>PLZ</sub> t <sub>PHZ</sub>	5	3.2	11.4	3.1	12.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	63 Typ.		63 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per latch.

$$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency}$$

$$C_L = \text{output load capacitance}$$

$$V_{CC} = \text{supply voltage.}$$

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD54AC373F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54AC373F3A	<a href="#">Samples</a>
CD54ACT373F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54ACT373F3A	<a href="#">Samples</a>
CD54ACT533F3A	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
CD74AC373E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC373E	<a href="#">Samples</a>
CD74AC373EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC373E	<a href="#">Samples</a>
CD74AC373M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC373M	<a href="#">Samples</a>
CD74AC373M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC373M	<a href="#">Samples</a>
CD74AC373M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC373M	<a href="#">Samples</a>
CD74AC373M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC373M	<a href="#">Samples</a>
CD74AC373ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC373M	<a href="#">Samples</a>
CD74AC373MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC373M	<a href="#">Samples</a>
CD74ACT373E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT373E	<a href="#">Samples</a>
CD74ACT373EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT373E	<a href="#">Samples</a>
CD74ACT373M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT373M	<a href="#">Samples</a>
CD74ACT373M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT373M	<a href="#">Samples</a>
CD74ACT373M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT373M	<a href="#">Samples</a>
CD74ACT373M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT373M	<a href="#">Samples</a>
CD74ACT373ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT373M	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74ACT373MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT373M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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#### OTHER QUALIFIED VERSIONS OF CD54AC373, CD54ACT373, CD74AC373, CD74ACT373 :

● Catalog: [CD74AC373](#), [CD74ACT373](#)

● Military: [CD54AC373](#), [CD54ACT373](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74ACT373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC373M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74ACT373M96	SOIC	DW	20	2000	367.0	367.0	45.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

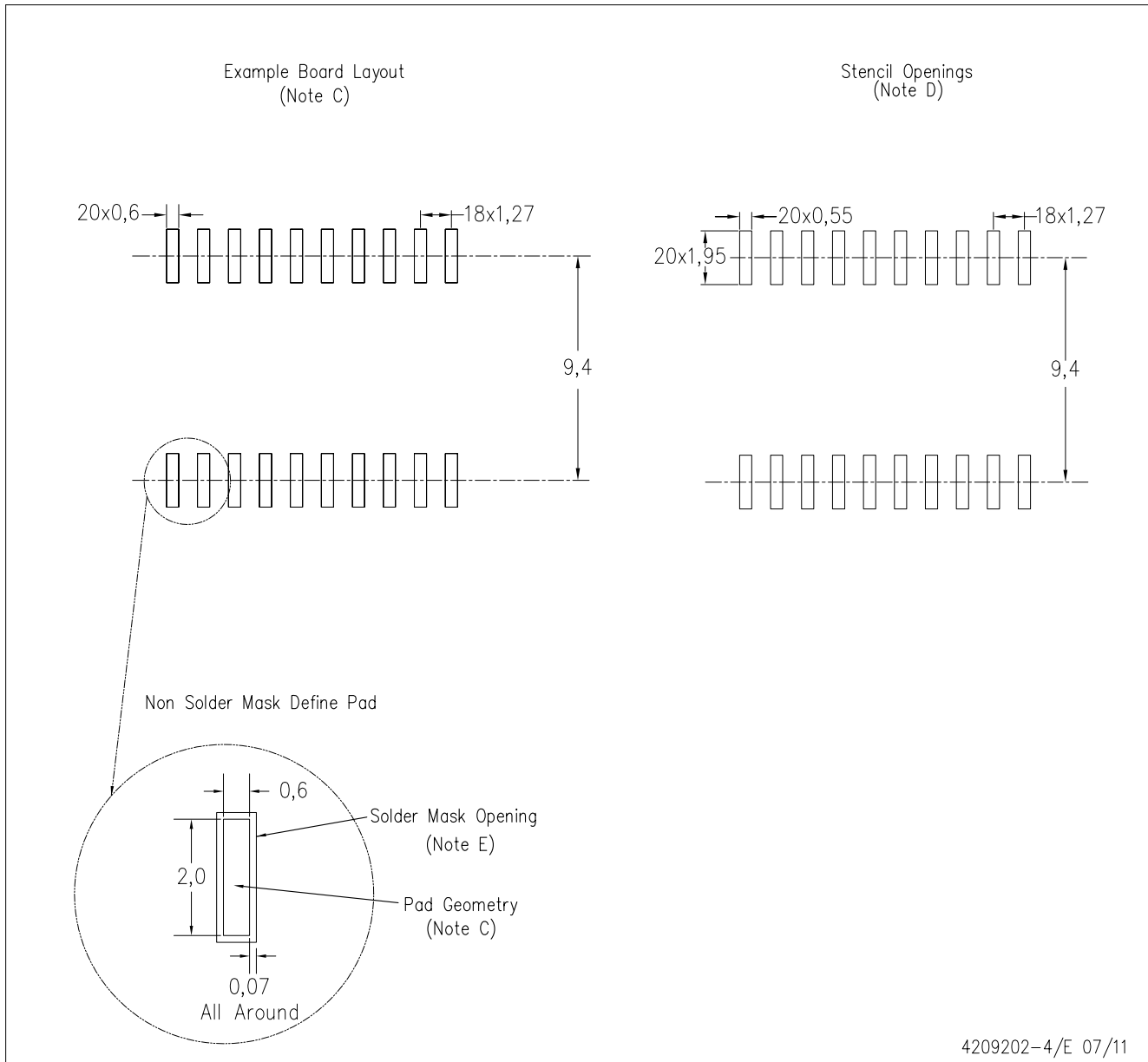


- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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