M5M418165BJ,TP-6,-7,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418165BXX-6,-6S	60	15	30	15	110	680
M5M418165BXX-7,-7S	70	20	35	20	130	590

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ------------------------ CMOS input level
- Low operating power dissipation
  M5M418165Bxx-6,-6S ------------------ 940.0mW (Max)
  M5M418165Bxx-7,-7S ------------------ 830.0mW (Max)
- Hyper-page mode, Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms ($A_0 \sim A_9$)

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
$A_0 \sim A_9$	Address inputs
$DQ_1 \sim DQ_{16}$	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)
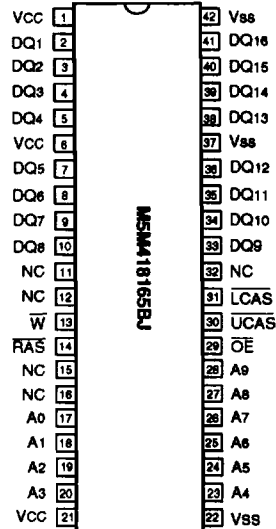
Outline 42P0K (400mil SOJ)
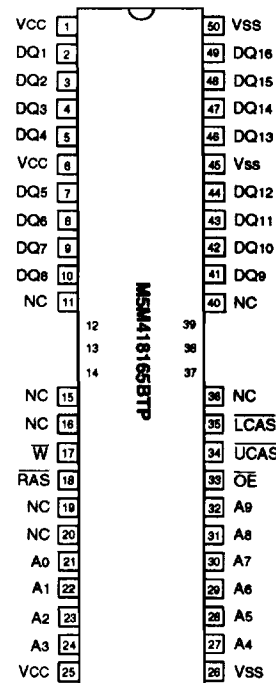
Outline 50P3W-L (400mil TSOP Normal Bend)

NC : NO CONNECTION

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FUNCTION

The M5M418165BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM
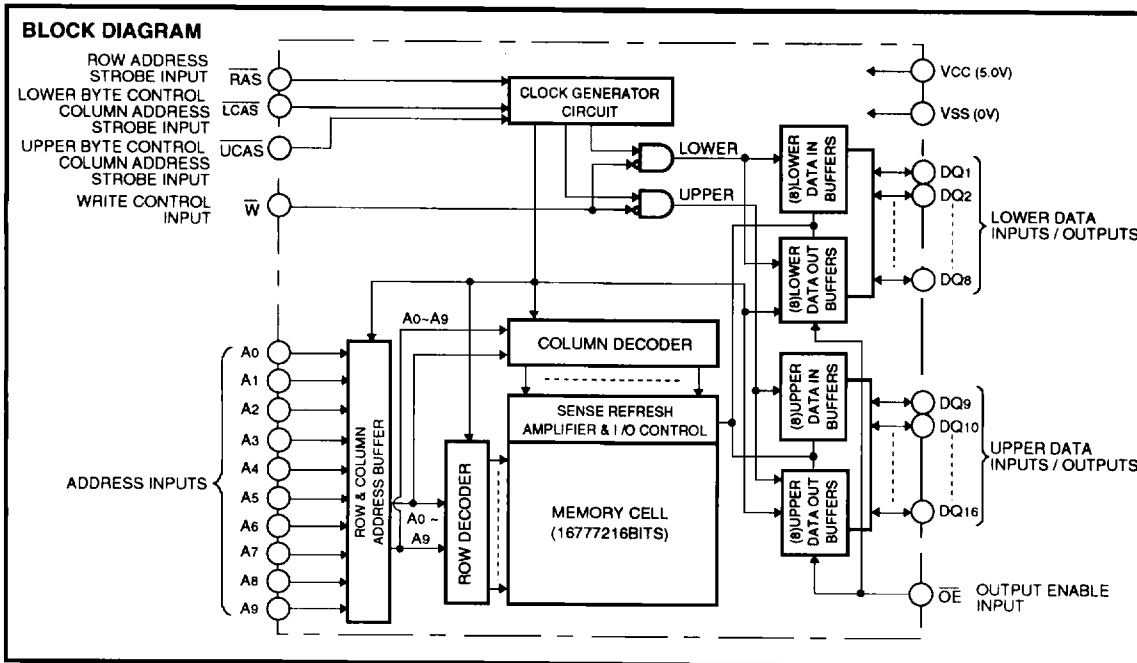
HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1~7	V
V I	Input voltage		-1~7	V
Vo	Output voltage		-1~7	V
I o	Output current		50	mA
Pd	Power dissipation	Ta=25 °C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.4		6.0	V
VIL	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to VSS.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH=-5.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL=4.2mA	0		0.4	V
Ioz	Off-state output current		Q floating 0V≤VOUT ≤5.5V	-10		10	μA
I I	Input current		0V≤ VIN ≤ 6V, Other inputs pins=0V	-10		10	μA
ICC1(AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M418165B-6,-6S	RAS, CAS cycling tRC=tWC=min. output open			170	mA
		M5M418165B-7,-7S				150	
ICC2	Supply current from Vcc, stand-by (Note 6)		RAS= CAS =VIH, output open			2	mA
		M5M418165B-6,-7	RAS= CAS≥Vcc -0.2V, output open			1	
		M5M418165B-6S,-7S	RAS= CAS≥Vcc -0.2V, output open			0.3	
ICC3(AV)	Average supply current from Vcc, refreshing (Note 3,5)	M5M418165B-6,-6S	RAS cycling, CAS=VIH tRC=min. output open			170	mA
		M5M418165B-7,-7S				150	
ICC4(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M418165B-6,-6S	RAS=VIL, CAS cycling tPC=min. output open			135	mA
		M5M418165B-7,-7S				115	
ICC6(AV)	Average supply current from Vcc CAS before RAS refresh mode (Note 3)	M5M418165B-6,-6S	CAS before RAS refresh cycling tRC=min. output open			170	mA
		M5M418165B-7,-7S				150	

Note 2: Current flowing into an IC is positive, out is negative.

3: ICC1 (AV), ICC3 (AV) and ICC4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: ICC1 (AV) and ICC4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column address can be changed once or less while RAS=VIL and LCAS/UCAS=VIH .

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CAPACITANCE (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_I (A)$	Input capacitance, address inputs	Vɪ=Vss f=1MHz Vɪ=25mVrms			5	pF
$C_I (\overline{OE})$	Input capacitance, $\overline{OE}$ input				7	pF
$C_I (\overline{W})$	Input capacitance, write control input				7	pF
$C_I (\overline{RAS})$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_I (\overline{CAS})$	Input capacitance, $\overline{CAS}$ input				7	pF
C_I / O	Input/Output capacitance, data ports				8	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits				Unit
			M5M418165B-6,-6S		M5M418165B-7,-7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		60		70	ns
tAA	Columu address access time	(Note 7,10)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20	ns
tOHC	Output hold time from $\overline{CAS}$		5		5		ns
tOHR	Output hold time from $\overline{RAS}$	(Note 13)	5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)	0	15	0	20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)	0	15	0	20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)	0	15	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-5mA) / VOL=0.4V(IOL=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that tRCD ≥ tRCD(max) and tASC ≥ tASC(max). and tCP≥ tCP(max).

9: Assumes that tRCD ≤ tRCD(max) and tRAD ≤ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

10: Assumes that tRAD ≥ tRAD(max) and tASC ≤ tASC(max).

11: Assumes that tCP ≤ tCP(max) and tASC ≥ tASC(max).

12: tOEZ(max), tWEZ(max), tOFF(max) and tREZ(max) defines the time at which the output achieves the high impedance state (IOUT≤ |±10uA|) and is not reference to VOH(min) or VOL(max).

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Hyper-Page Mode Cycles)

(Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		M5M418165B-6,-6S Min	M5M418165B-6,-6S Max	M5M418165B-7,-7S Min	M5M418165B-7,-7S Max	Unit
tREF	Refresh cycle time	-6, -7		16.4		16.4	ms
tREF	Refresh cycle time	-6S, -7S		128		128	ms
tRP	RAS high pulse width		40		50		ns
tRCD	Delay time, RAS low to CAS low	(Note 16)	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low		5		5		ns
tRPC	Delay time, RAS high to CAS low		0		0		ns
tCPN	CAS high pulse width		10		10		ns
tRAD	Column address delay time from RAS low	(Note 17)	15	30	15	35	ns
tASR	Row address setup time before RAS low		0		0		ns
tASC	Column address setup time before CAS low	(Note 18)	0	10	0	13	ns
tRAH	Row address hold time after RAS low		10		10		ns
tCAH	Column address hold time after CAS low		10		10		ns
tDZC	Delay time, data to CAS low	(Note 19)	0		0		ns
tDZO	Delay time, data to OE low	(Note 19)	0		0		ns
tRDD	Delay time, RAS high to data	(Note 20)	15		20		ns
tCDD	Delay time, CAS high to data	(Note 20)	15		20		ns
tODD	Delay time, OE high to data	(Note 20)	15		20		ns
tT	Transition time	(Note 21)	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD ≥ tRAD(max) and tASC ≤ tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD ≥ tRCD(max) and tASC ≥ tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		M5M418165B-6,-6S Min	M5M418165B-6,-6S Max	M5M418165B-7,-7S Min	M5M418165B-7,-7S Max	Unit
tRC	Read cycle time		110		130		ns
tRAS	RAS low pulse width		60	10000	70	10000	ns
tCAS	CAS low pulse width		10	10000	13	10000	ns
tCSH	CAS hold time after RAS low		48		55		ns
tRSH	RAS hold time after CAS low		15		20		ns
tRCS	Read setup time before CAS low		0		0		ns
tRCH	Read hold time after CAS high	(Note 22)	0		0		ns
tRRH	Read hold time after RAS high	(Note 22)	10		10		ns
tRAL	Column address to RAS hold time		30		35		ns
tCAL	Column address to CAS hold time		18		23		ns
tORH	RAS hold time after OE low		15		20		ns
tOCH	CAS hold time after OE low		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		M5M418165B-6,-6S		M5M418165B-7,-7S		Unit
			Min	Max	Min	Max	
t_{WC}	Write cycle time		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 24)		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		13		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		10		13		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		10		13		ns
t_{WP}	Write pulse width		10		13		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		M5M418165B-6,-6S		M5M418165B-7,-7S		Unit
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 23)		133		161		ns
t_{RAS}	$\overline{RAS}$ low pulse width		89	10000	107	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		44	10000	57	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		82		99		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		44		57		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 24)		32		42		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 24)		77		92		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 24)		47		57		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

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Hyper page Mode Cycle
(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, HI-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter		Limits				Unit
			M5M418165B-6,-6S		M5M418165B-7,-7S		
			Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time		25		30		ns
tHPRWC	Hyper page mode read write/read modify write cycle time		66		79		ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle	(Note 26)	77	100000	92	100000	ns
tCP	$\overline{CAS}$ high pulse width	(Note 27)	10	18	13	18	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 24)	52		62		ns
tCHOL	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access		7		7		ns
tOEPE	$\overline{OE}$ Pulse width (Hi-Z control)		7		7		ns
tWPE	$\overline{W}$ Pulse width (Hi-Z control)		7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read		32		42		ns
tHAWD	Delay time, address to $\overline{W}$ low after read		62		72		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read		72		82		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read		15		20		ns
tHAOD	Delay time, address to $\overline{OE}$ high after read		30		35		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read		35		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

26: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.

27: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits				Unit
		M5M418165B-6,-6S		M5M418165B-7,-7S		
		Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

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Timing Diagrams (Note 29)
Read Cycle
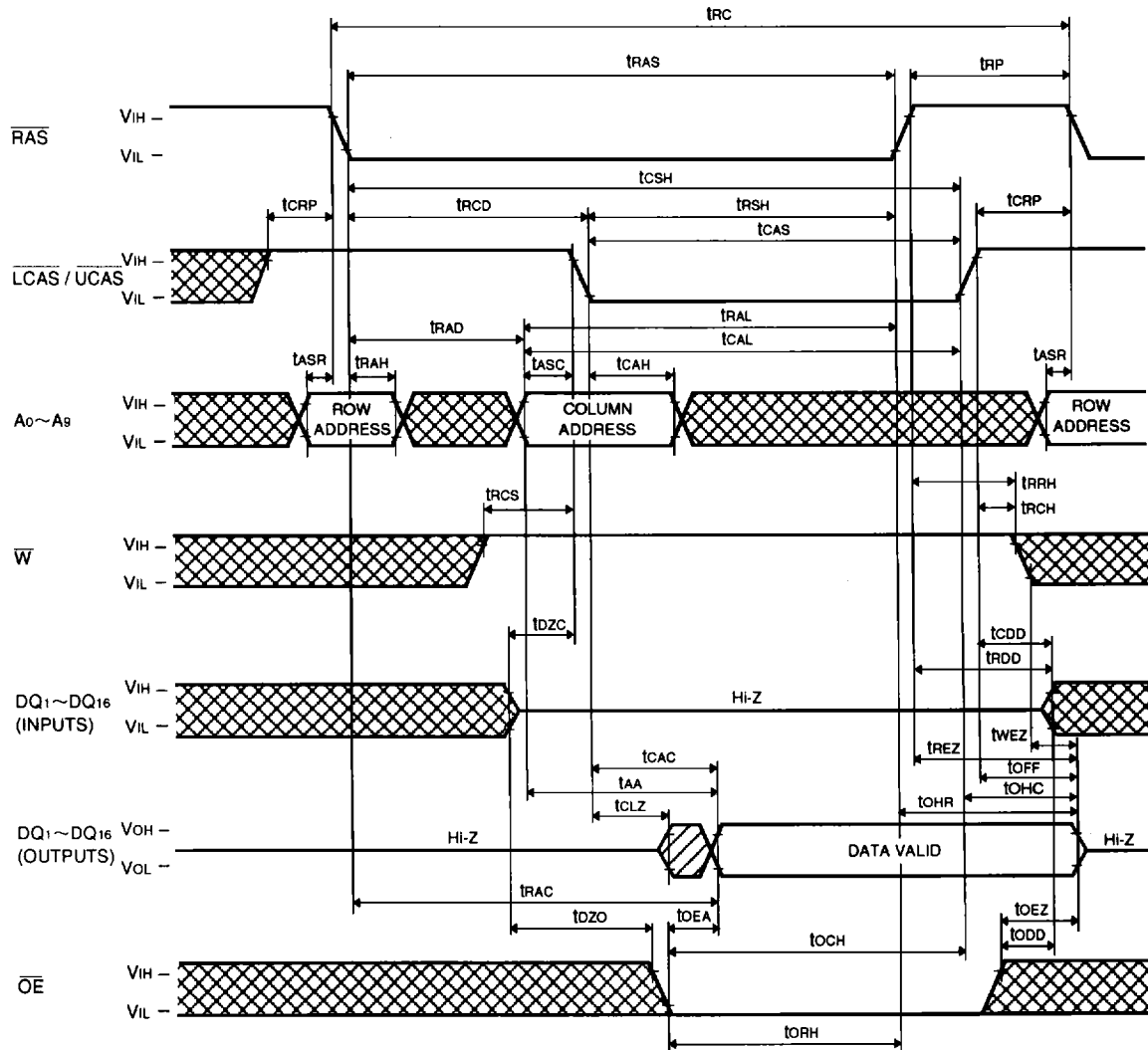
Note 29

Indicates the don't care input.
$V_{IH(min)} \le V_{IN} \le V_{IH(max)}$ or $V_{IL(min)} \le V_{IN} \le V_{IL(max)}$

Indicates the invalid output.

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM
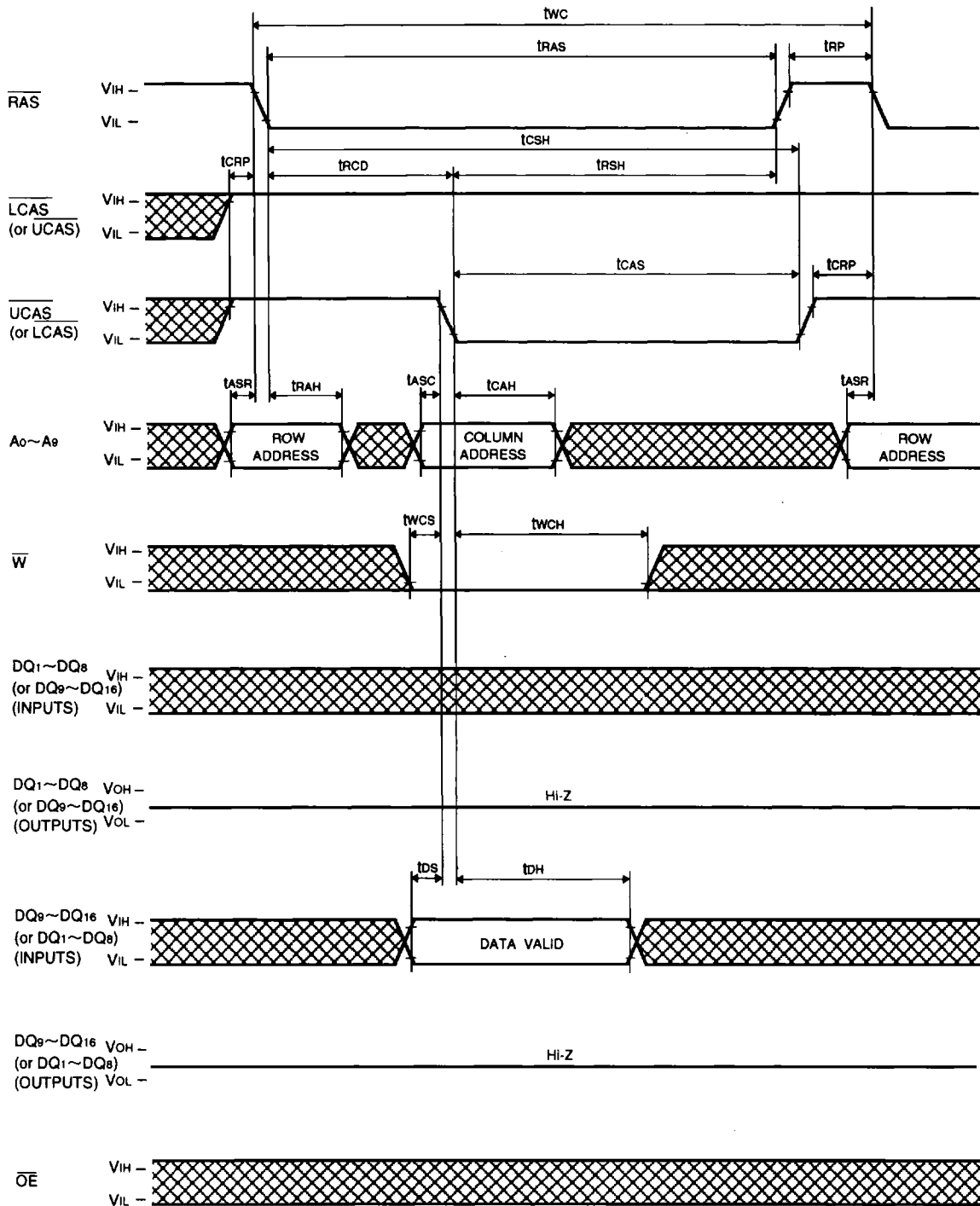
Byte Read Cycle
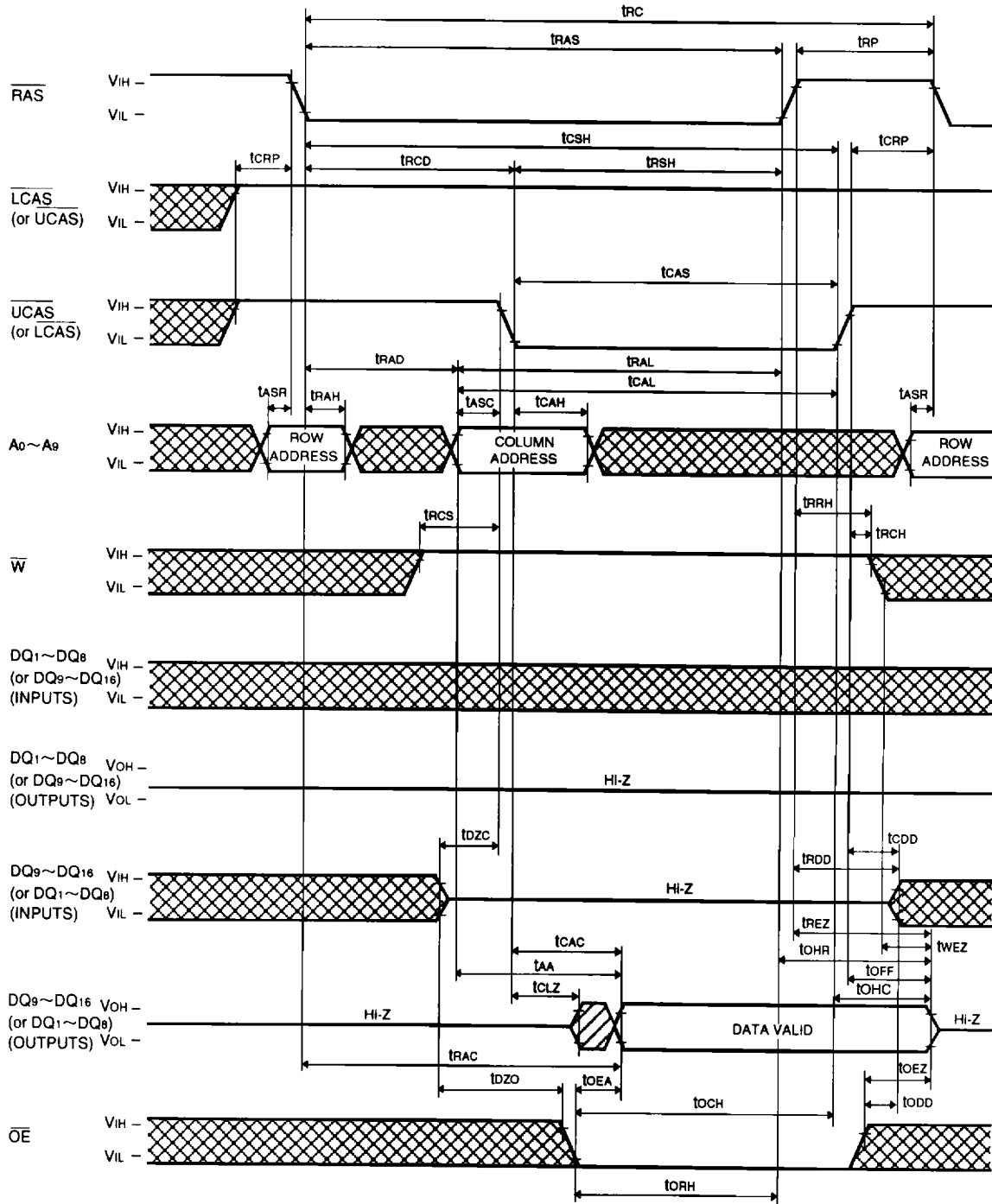
MITSUBISHI ELECTRIC

Early Write Cycle

Byte Early Write Cycle

MITSUBISHI
ELECTRIC
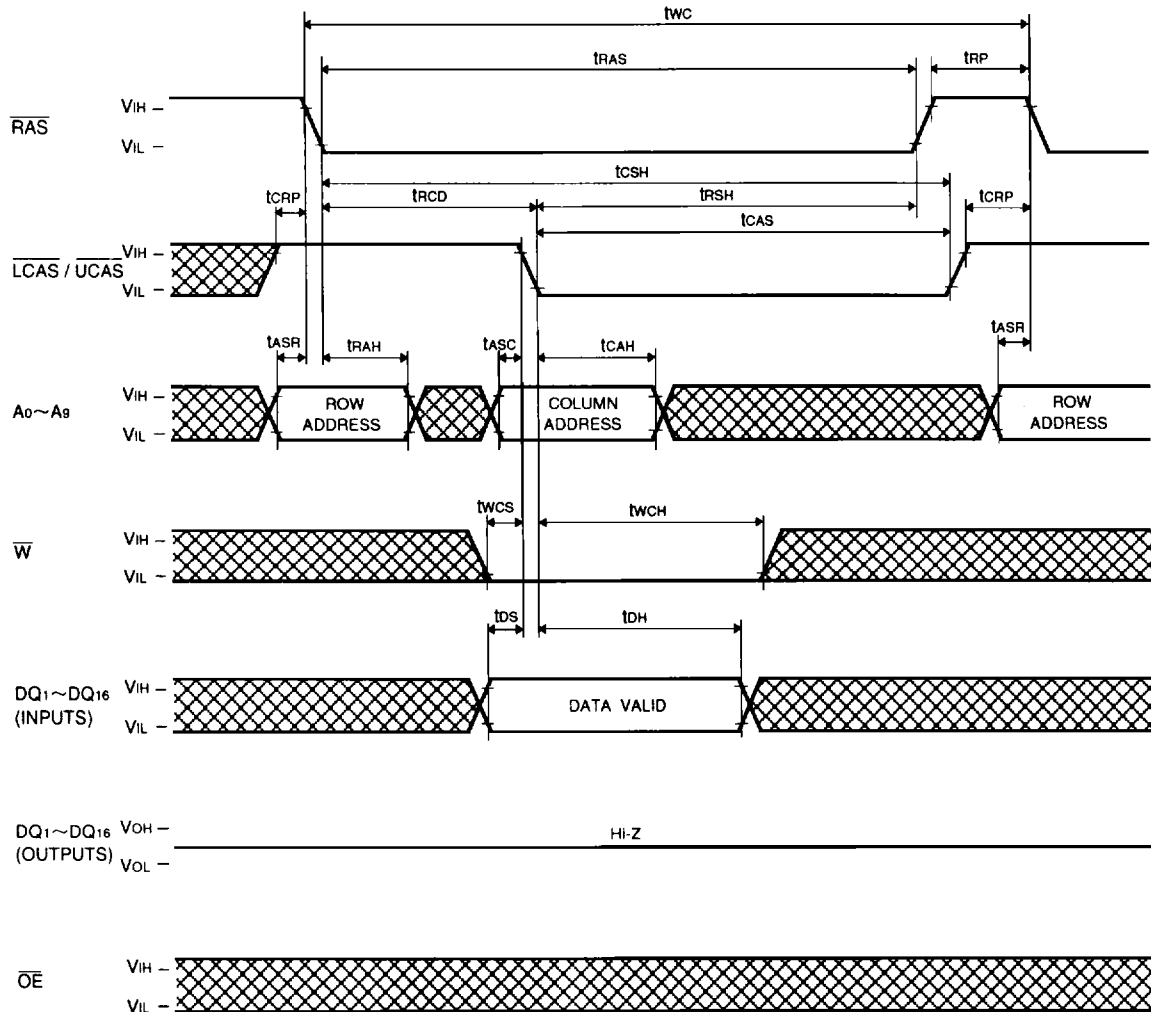
Delayed Write Cycle

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Byte Delayed Write Cycle
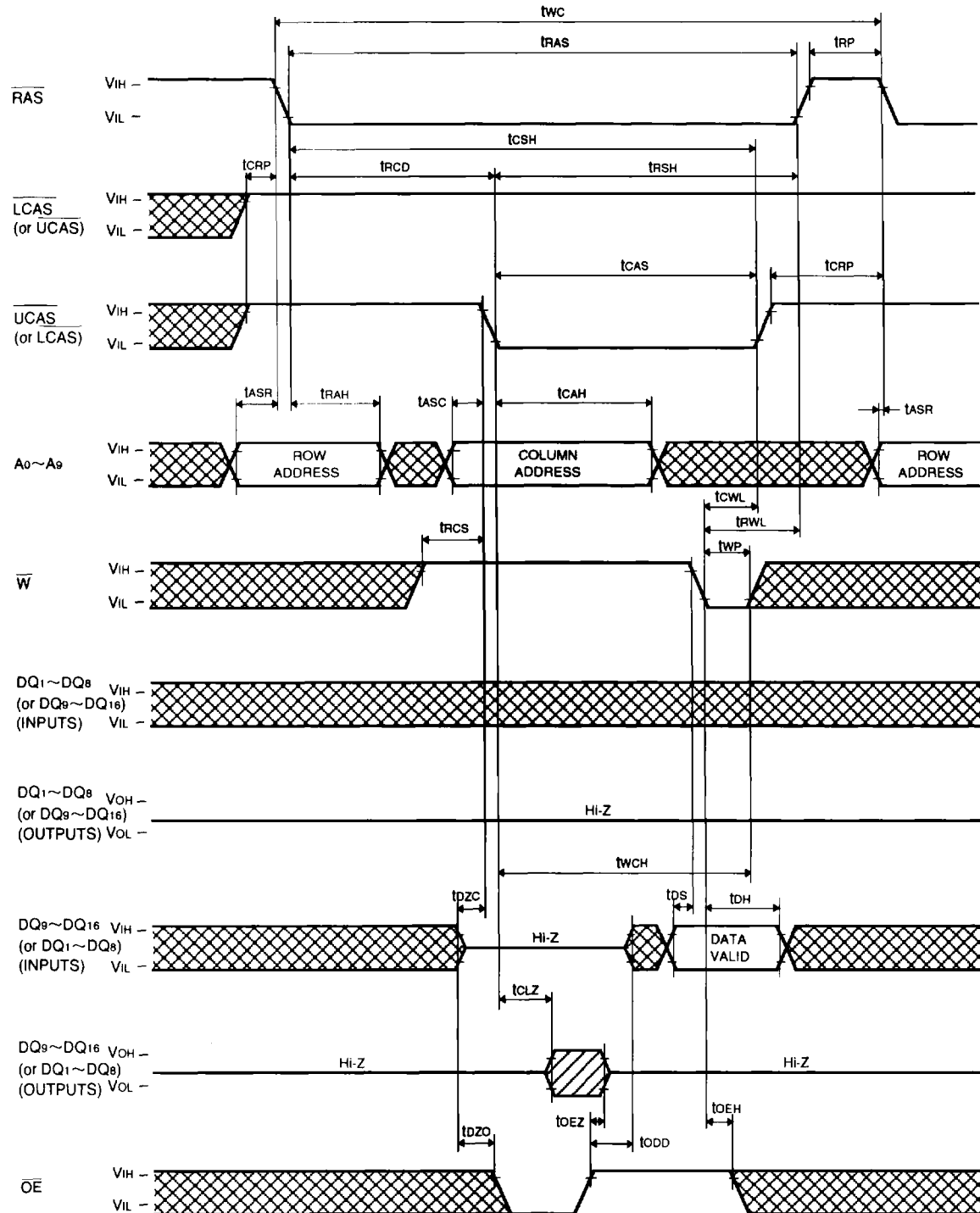
MITSUBISHI ELECTRIC

Read-Write, Read-Modify-Write Cycle
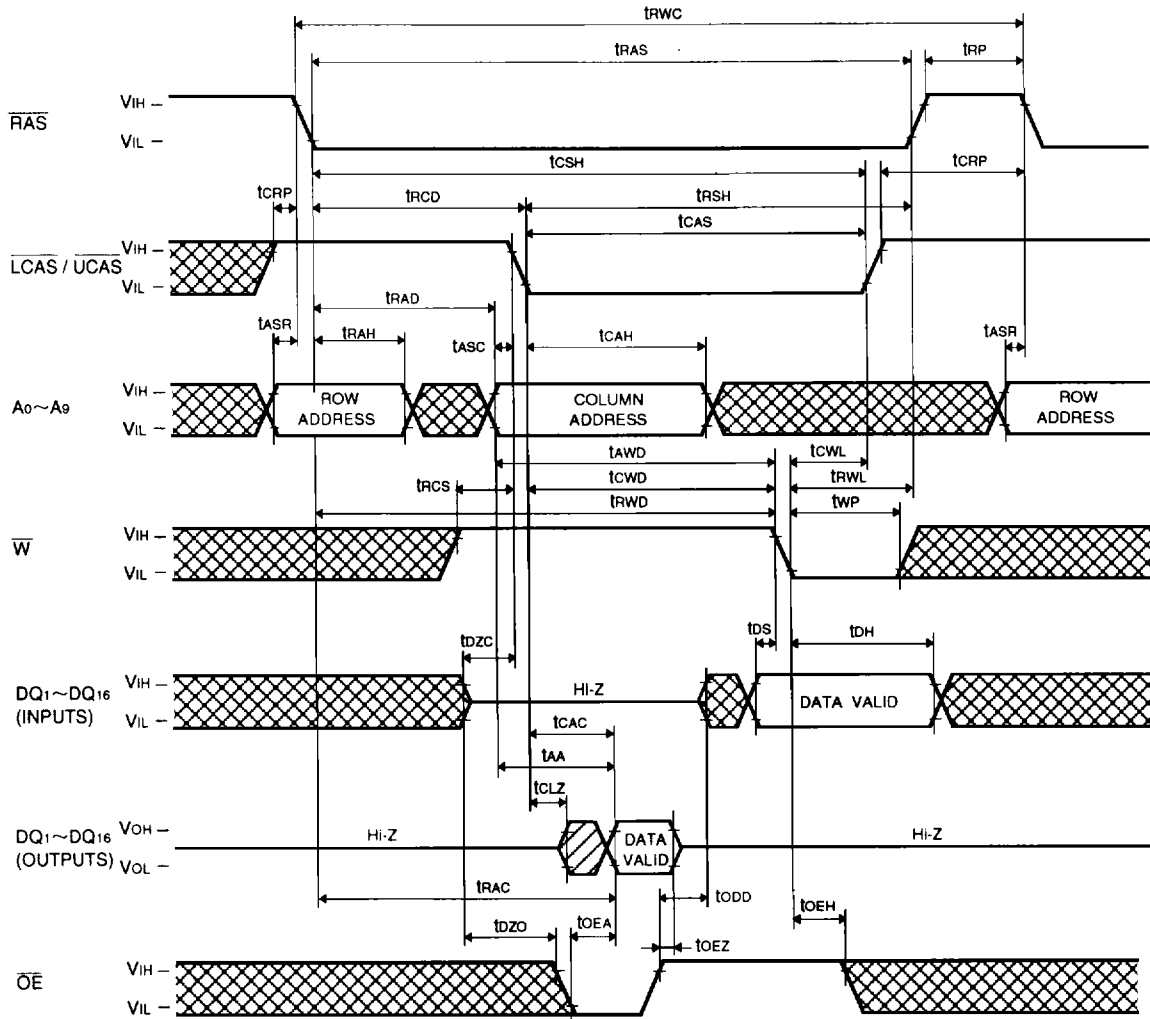
HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Byte Read-Write, Read-Modify-Write Cycle

MITSUBISHI ELECTRIC
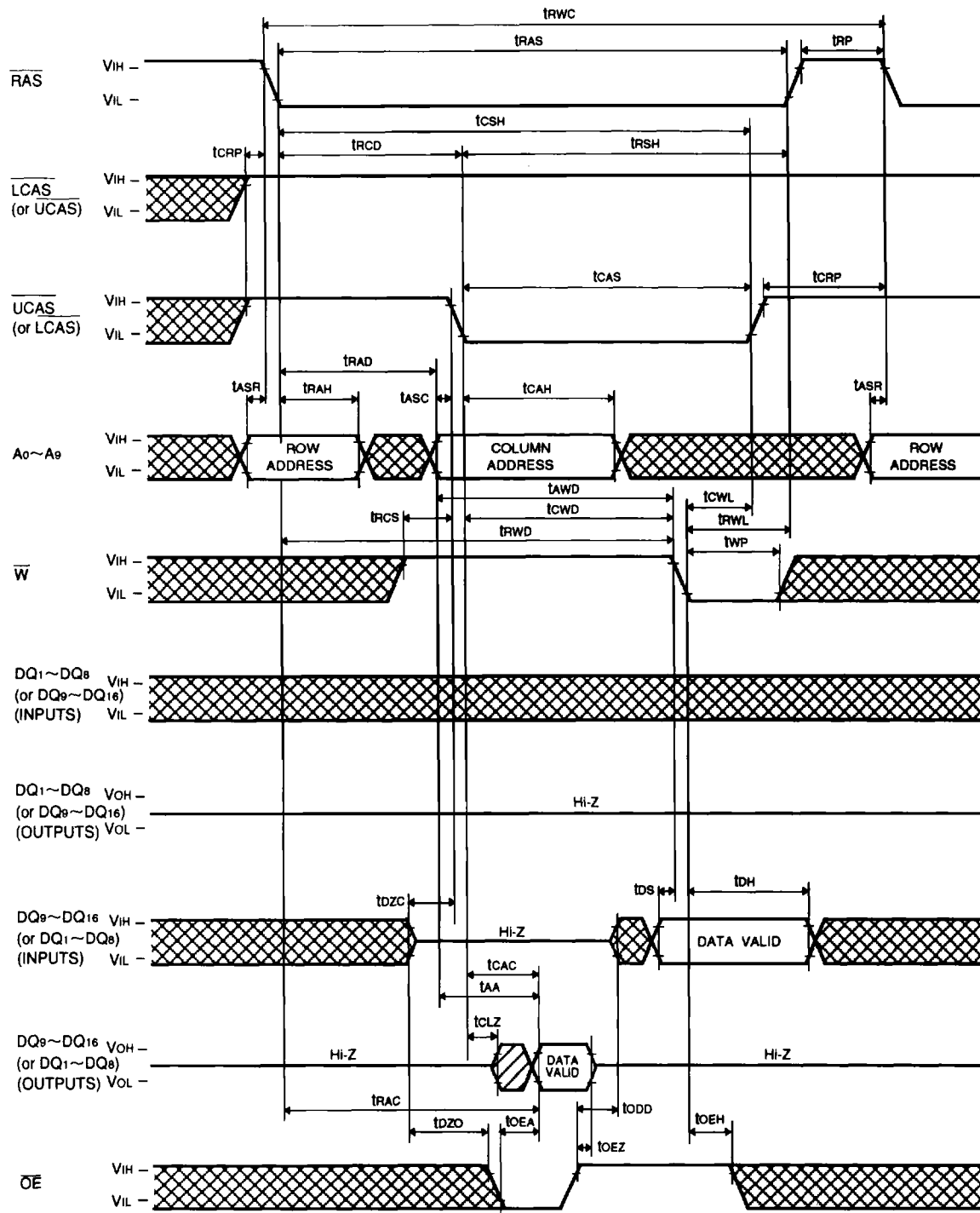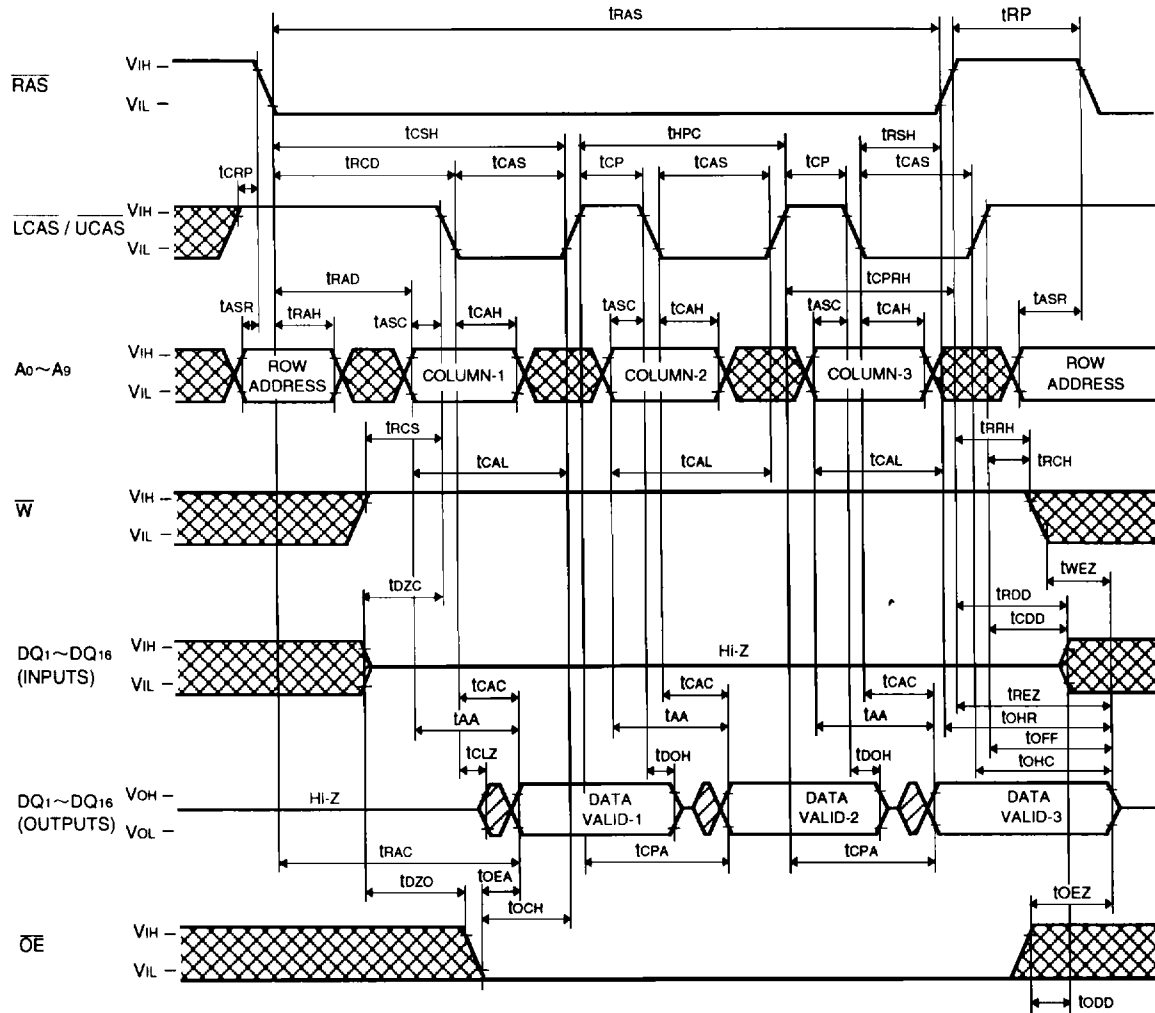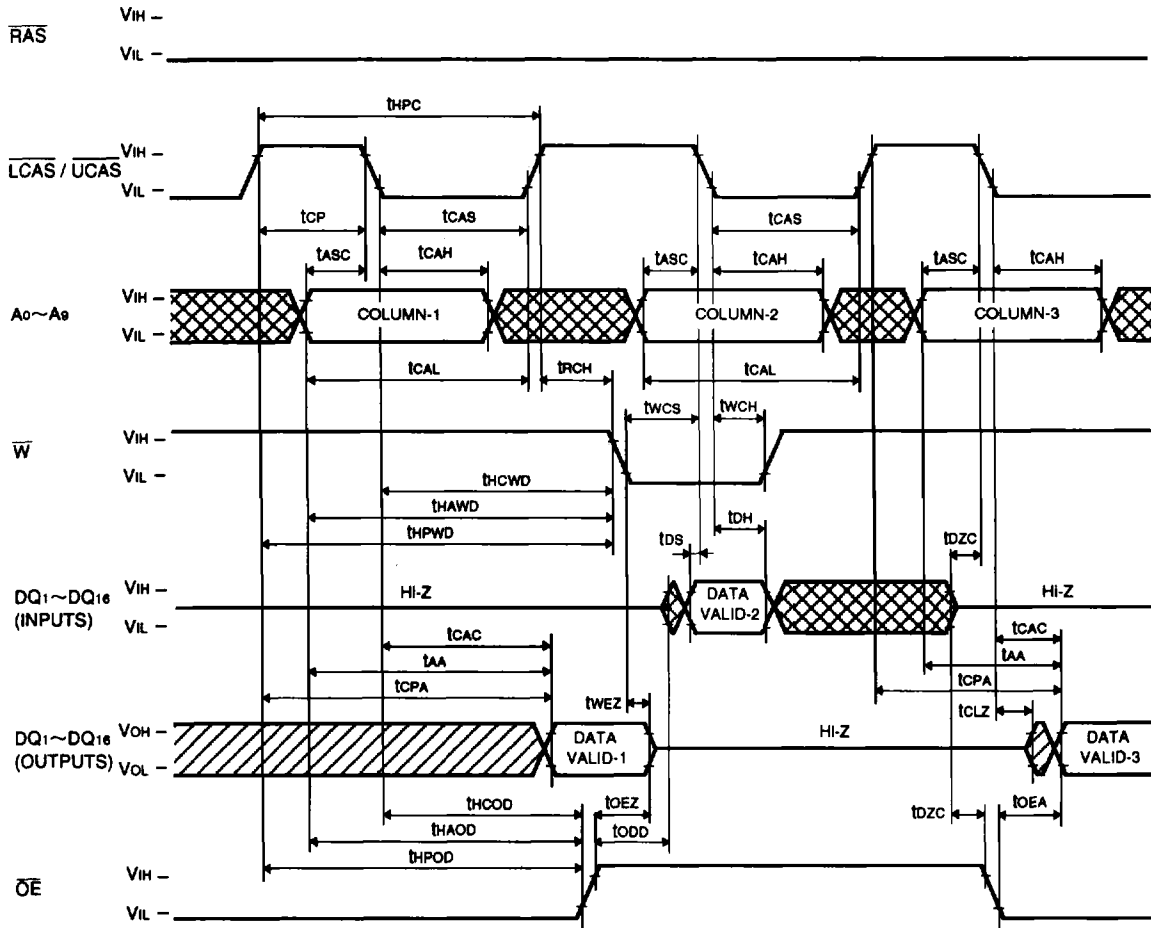
HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Read Cycle

Hyper Page Mode Byte Read Cycle

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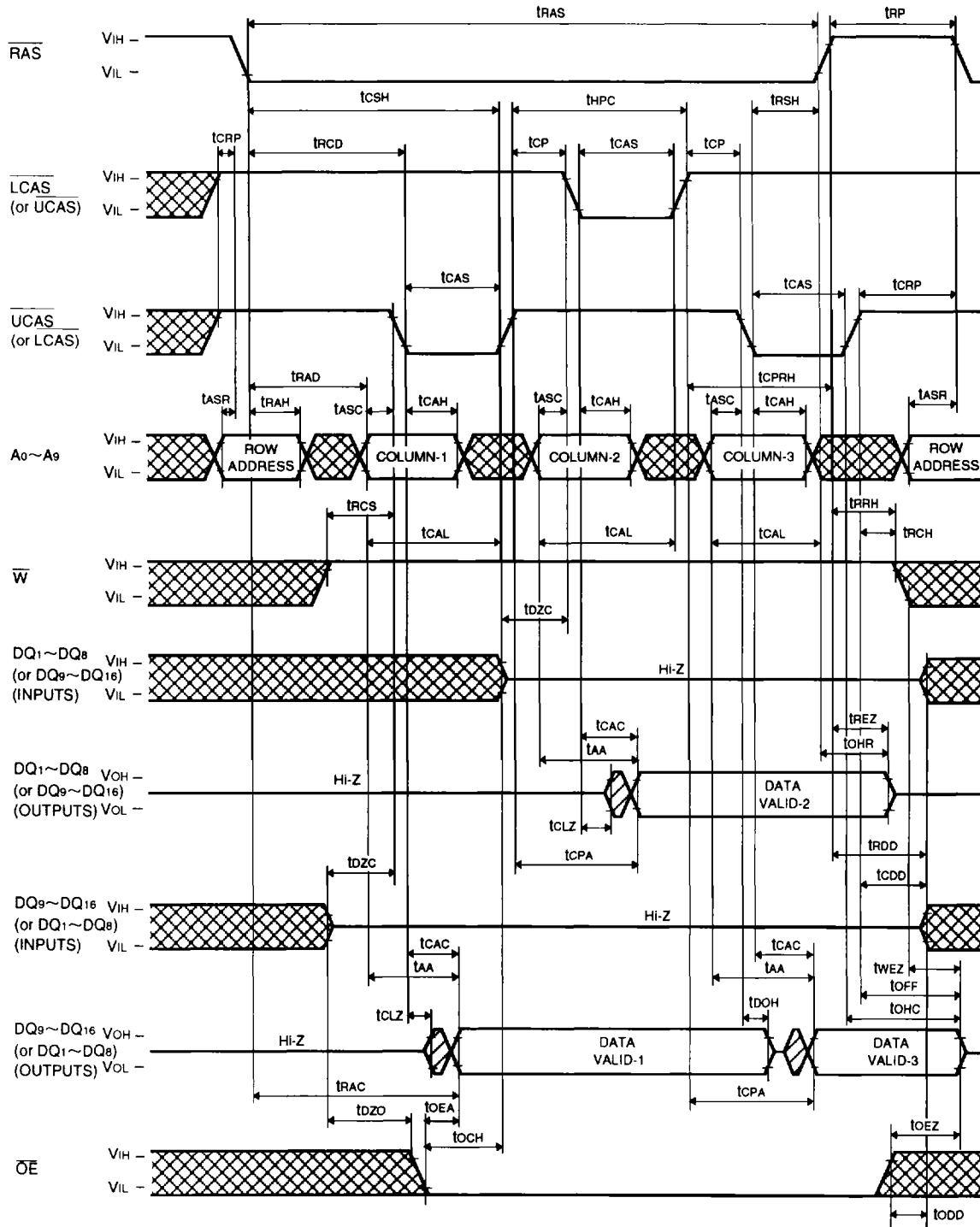
Hyper Page Mode Early Write Cycle
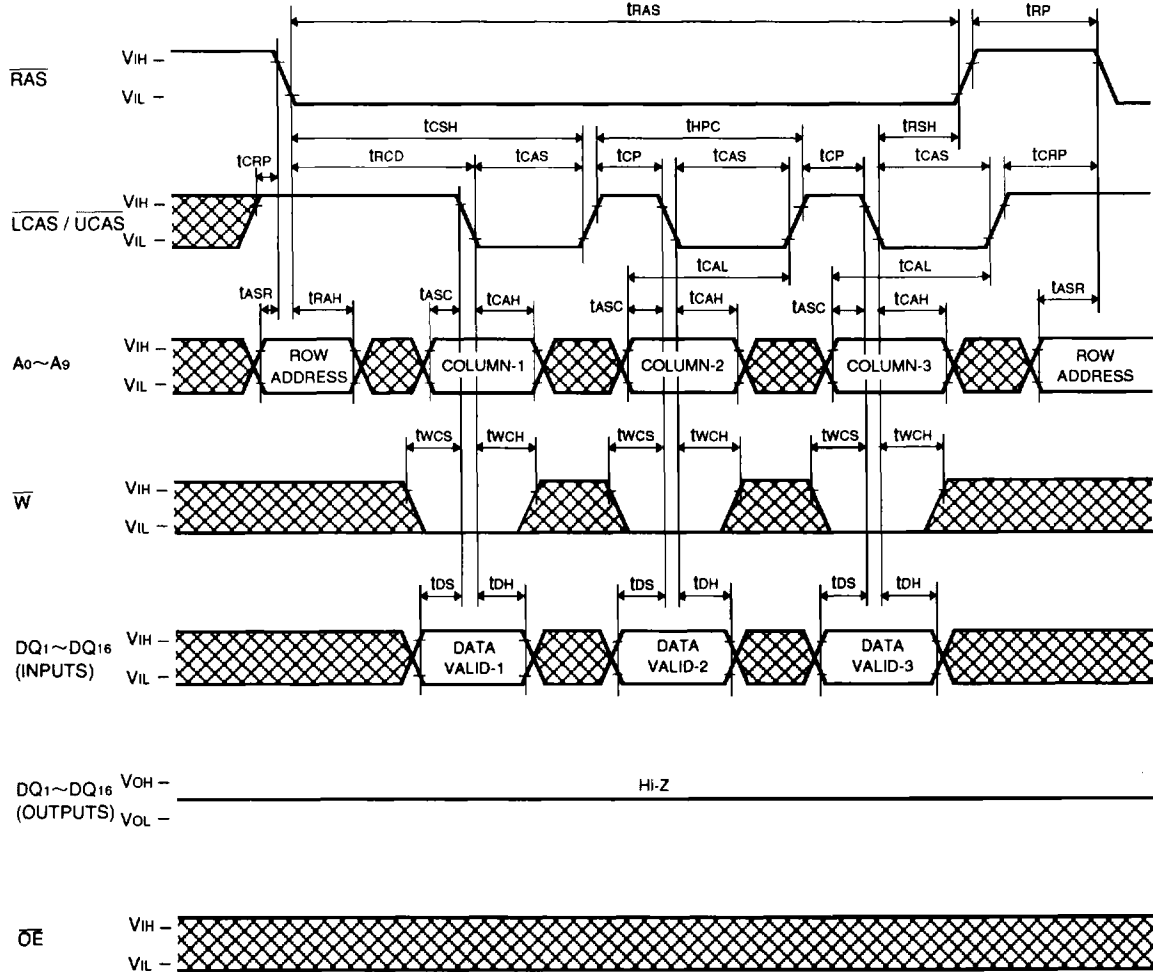
Hyper Page Mode Byte Early Write Cycle
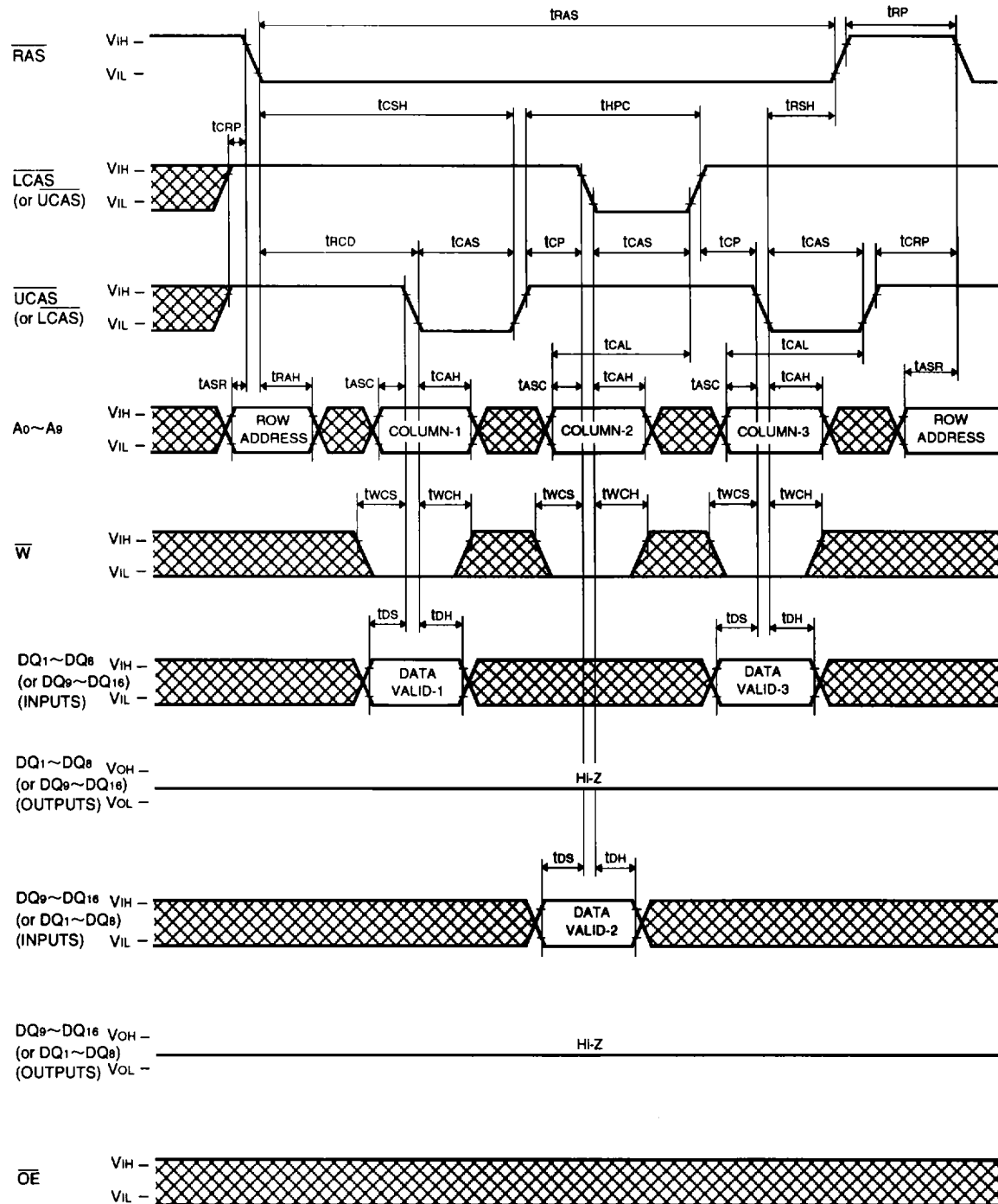
MITSUBISHI ELECTRIC

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM
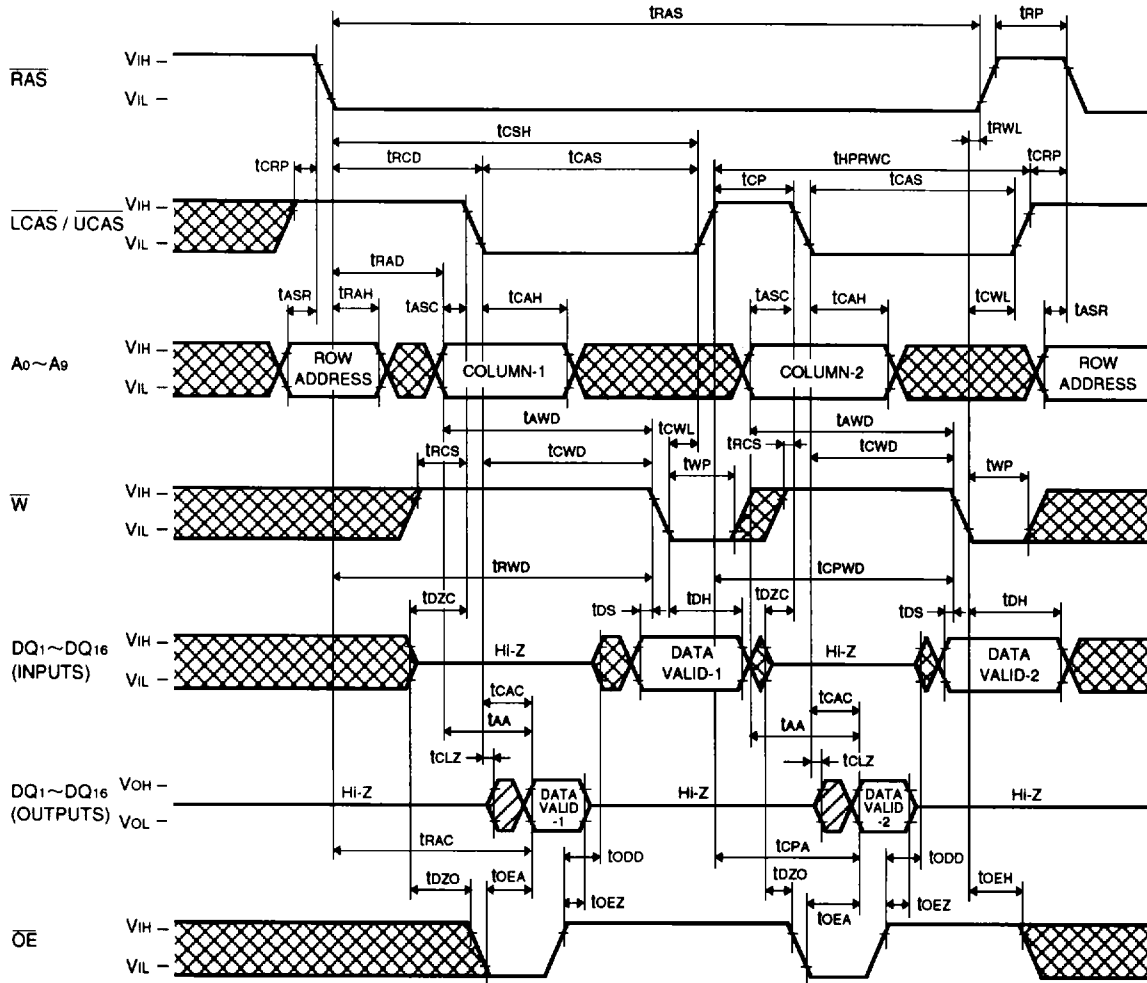
Hyper Page Mode Read-Write, Read-Modify-Write Cycle

Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle

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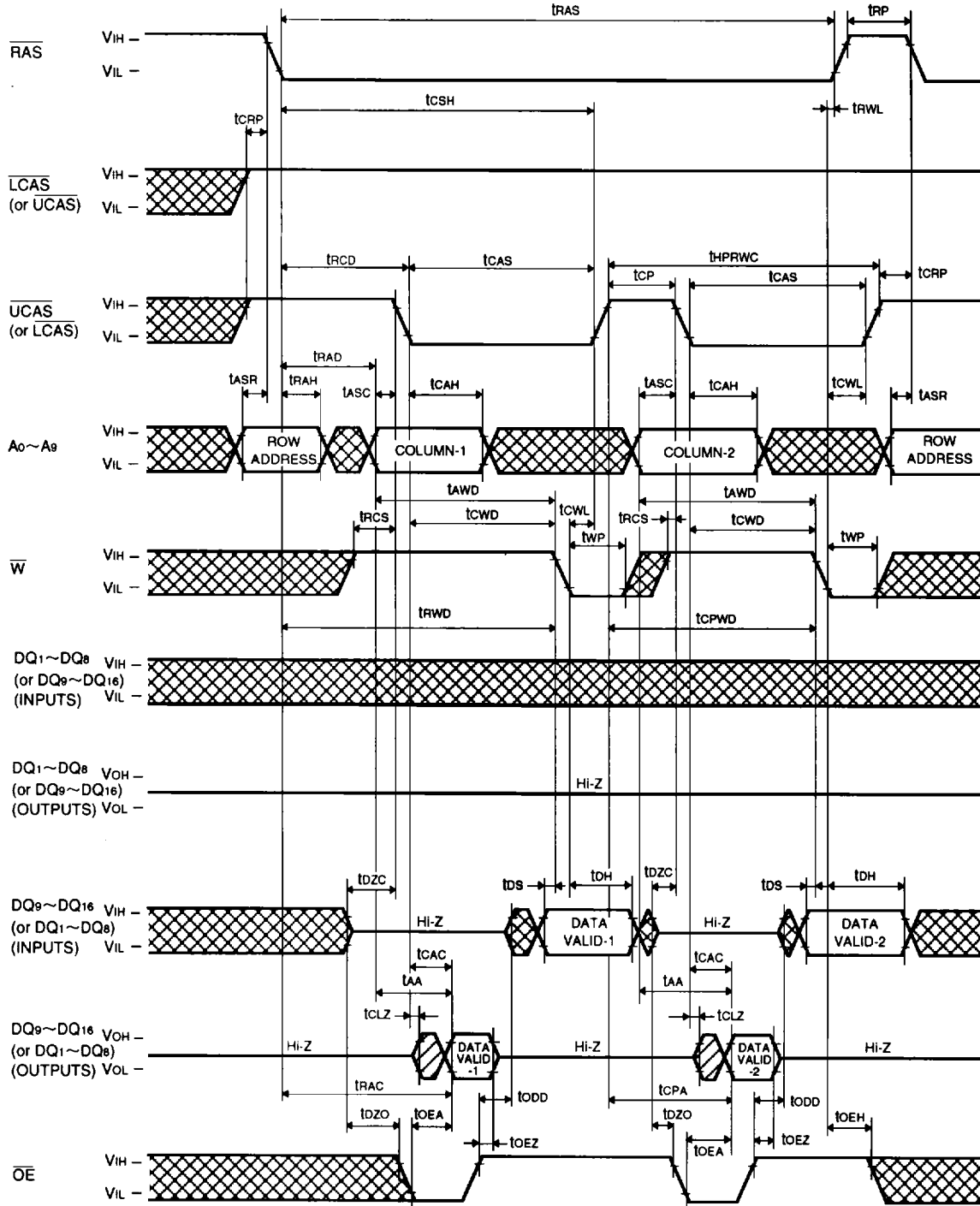
Hyper Page Mode Mix Cycle (1)

Hyper Page Mode Mix Cycle (2)

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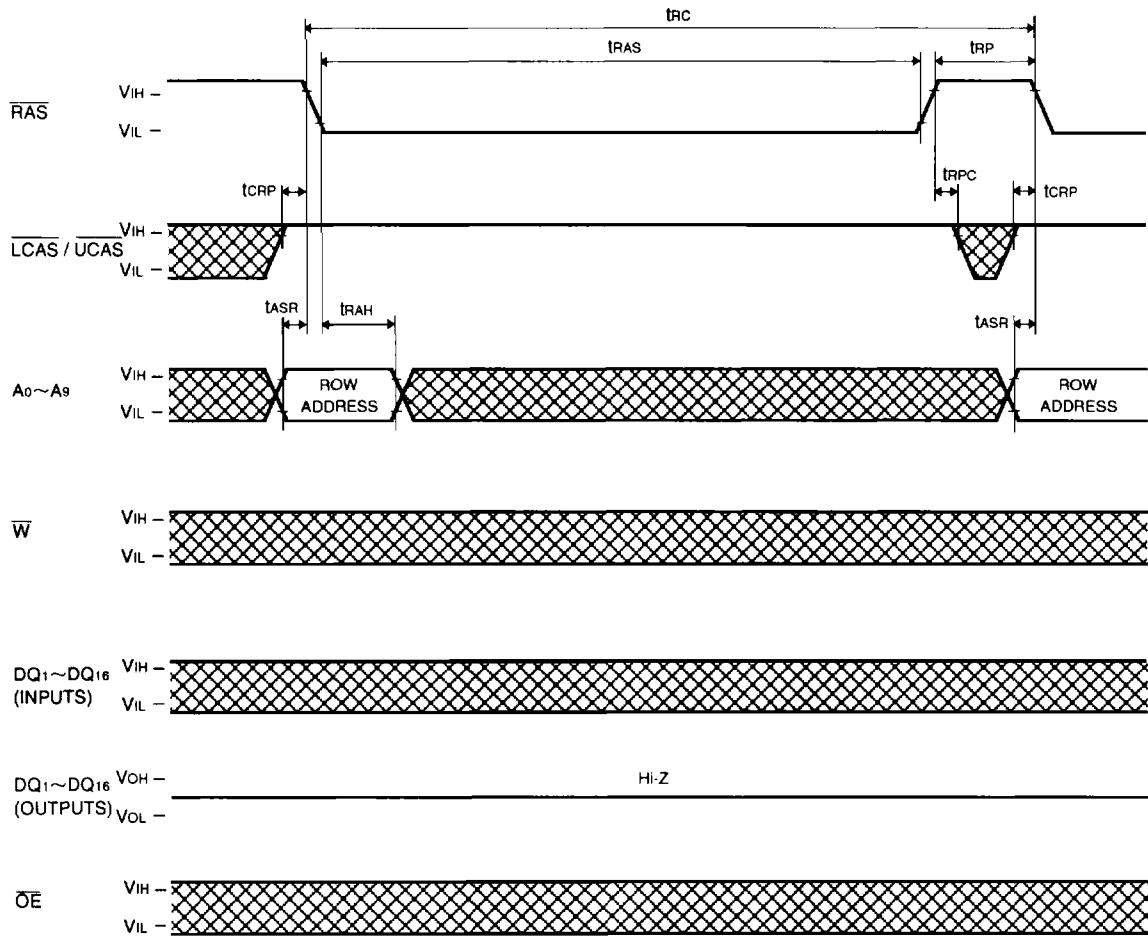
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)

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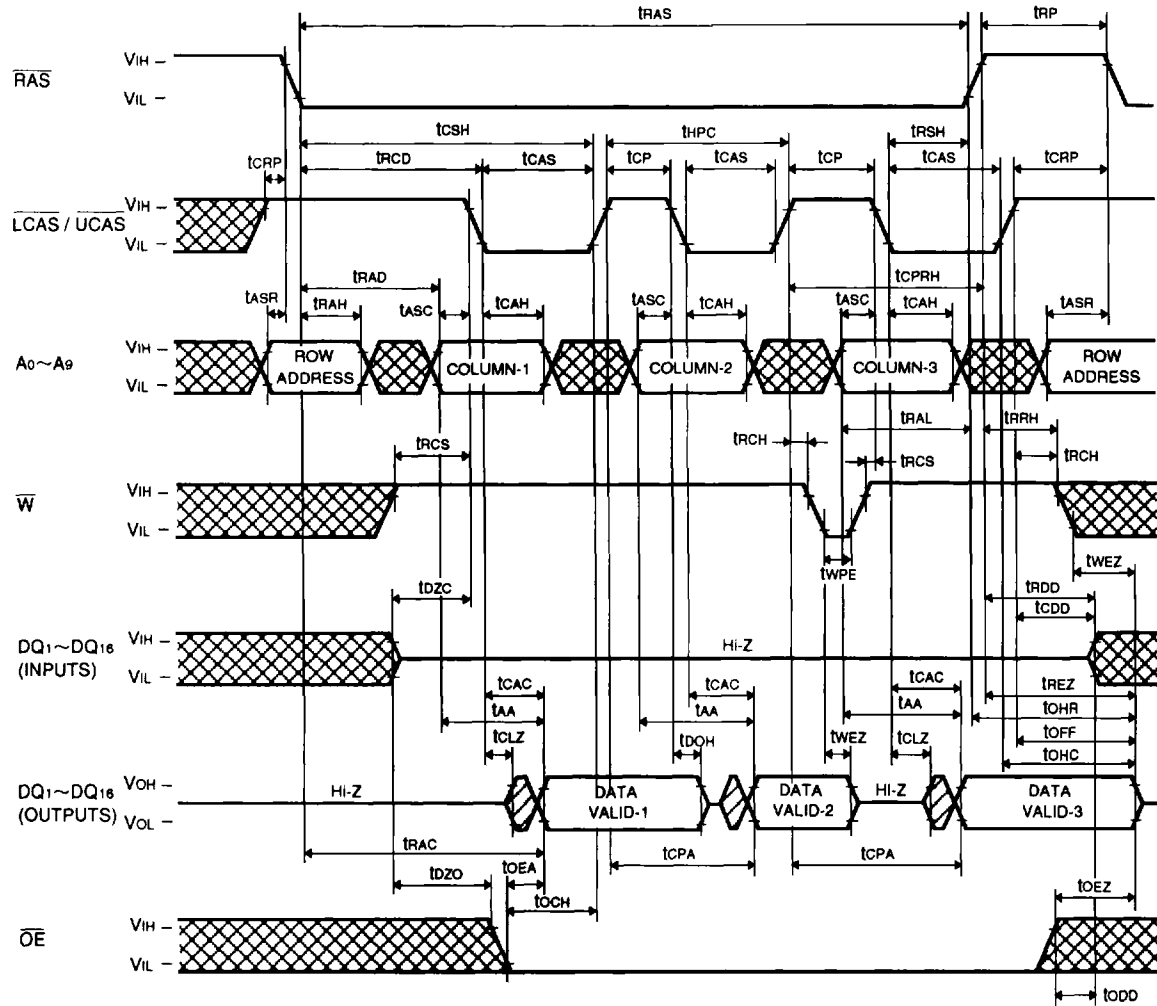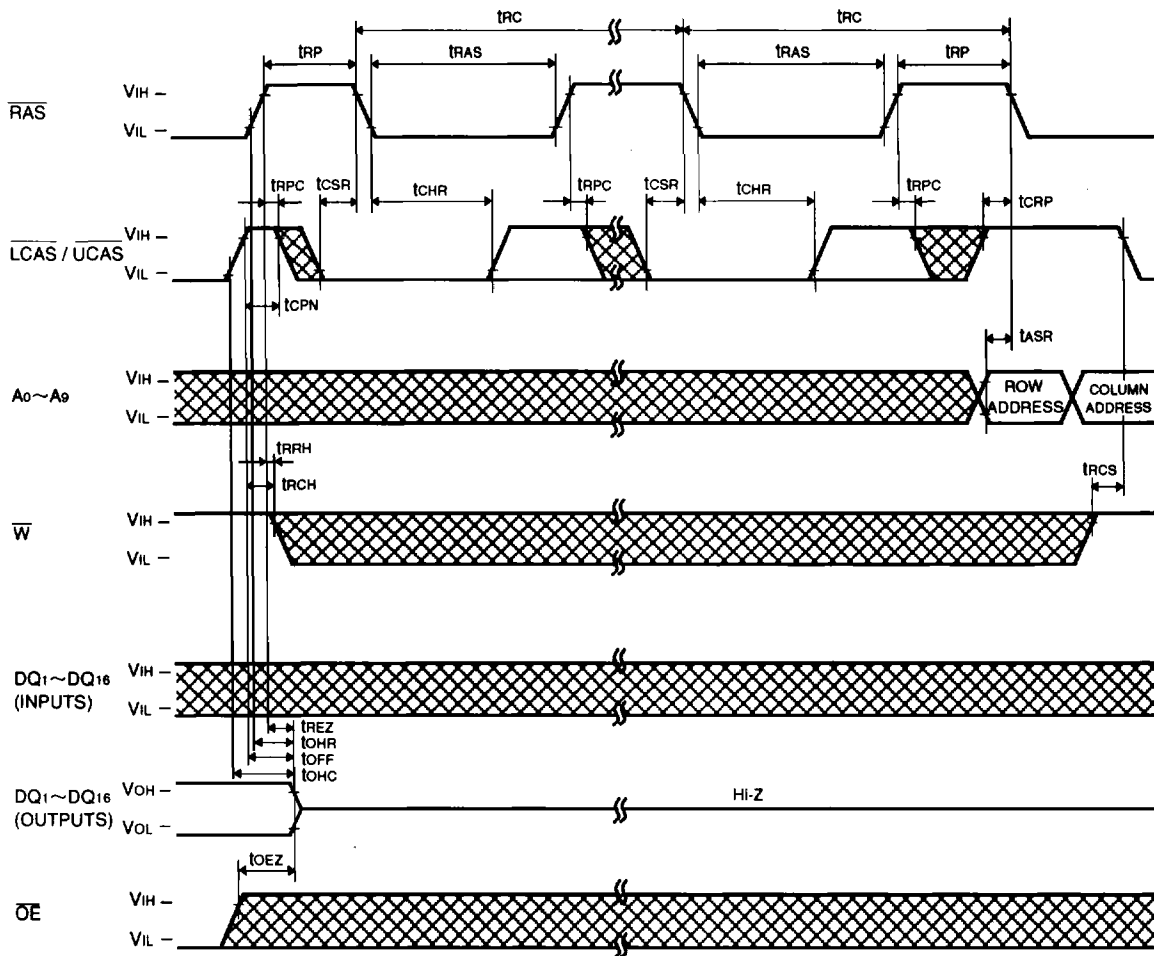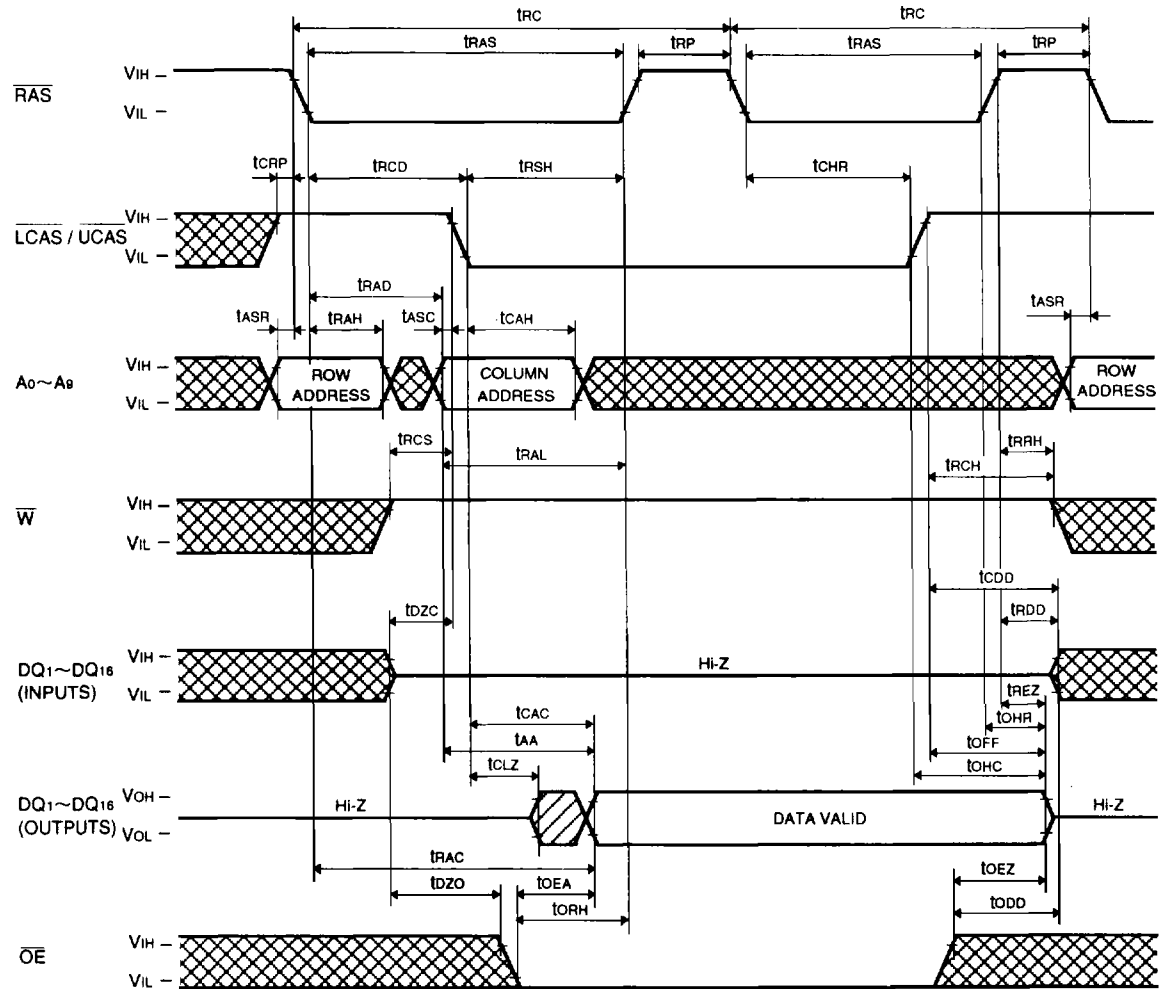
HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

RAS-only Refresh Cycle

tRC

tRAS

tRP

$\overline{\text{RAS}}$ VIH — VIL —

tCRP

$\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ VIH — VIL —

tRPC tCRP

tASR tRAH tASR

A0～A9 VIH — VIL —

ROW ADDRESS

ROW ADDRESS

$\overline{\text{W}}$ VIH — VIL —

DQ1～DQ16 (INPUTS) VIH — VIL —

DQ1～DQ16 (OUTPUTS) VOH — VOL —

Hi-Z

$\overline{\text{OE}}$ VIH — VIL —

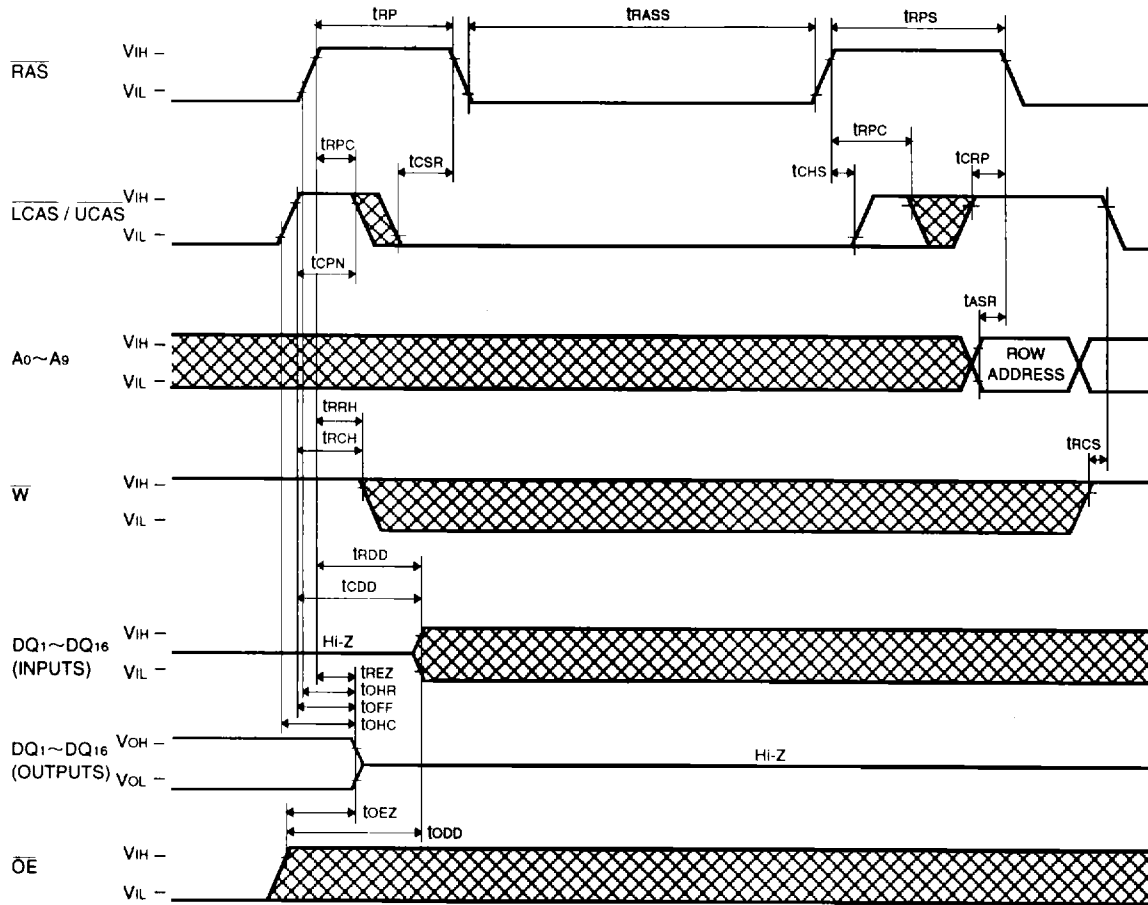CAS before RAS Refresh Cycle, Extended Refresh Cycle*

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Hidden Refresh Cycle (Read) (Note 30)

Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle * (Note 31)

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HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted) (Note 2)

| Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
ICC8(AV)	Average supply current from Vcc Extended refresh mode	M5M418165B (S)	$\overline{RAS}$ cycling $\overline{CAS} \leqq 0.2V$ or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W} \leqq 0.2V$ or $\geqq Vcc-0.2V$ $\overline{OE} \leqq 0.2V$ or $\geqq Vcc-0.2V$ $A_0 \sim A_9 \leqq 0.2V$ or $\geqq Vcc-0.2V$ tREF=128ms, output open tRAS=tRASmin~1 μs			500	μA
ICC9(AV)	Average supply current from Vcc Self-refresh cycle	M5M418165B (S)	$\overline{RAS} = \overline{CAS} \leqq 0.2V$			400	μA

TIMING REQUIREMENTS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M418165B-6S		M5M418165B-7S		
		Min	Max	Min	Max	
tRASS	Self refresh $\overline{RAS}$ low pulse width	100		100		μs
tRPS	Self refresh $\overline{RAS}$ high precharge time	110		130		ns
tCHS	Self refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS≦16.4ms and tSN≦16.4ms.
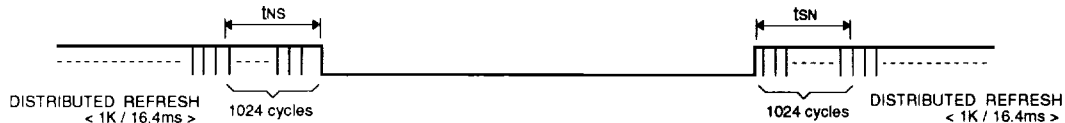
(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS +tSN≦16.4ms.