8-Bit Latches/Registers with Readback-Advanced CMOS-TTL Compatible

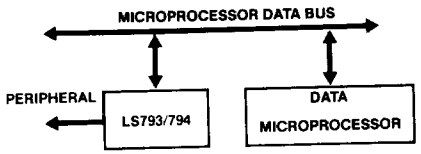
74ACT793 74ACT794

Features/Benefits

- **I/O port configuration enables output data back onto input bus**
- **Low quiescent supply current of < 10 μA (typical)**
- **Eighth bits matches byte boundaries**
- **Ideal for microprocessor interface**
- **Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to + 85°C**

Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an ACT793/4, for verification and/or updating.



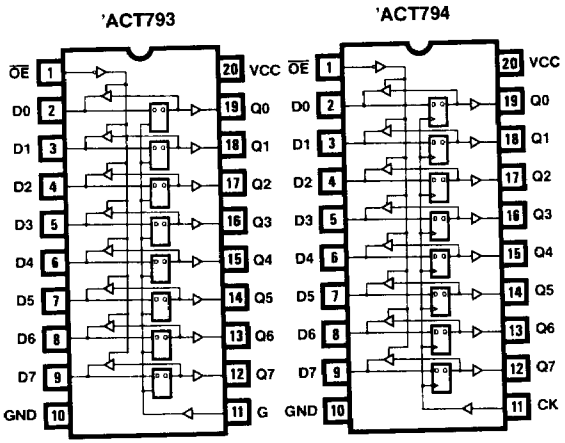
The data is loaded in the registers on the low-to-high transition of the clock (CK), for the ACT794. The data is passed through the ACT793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, $\overline{OE}$ is used to enable data on D7-D0. When $\overline{OE}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an outut bus so that the host can perform a read operation. When $\overline{OE}$ is High, D7-D0 are inputs to the latches/registers configuring D as an input bus.

The output drive of these commercial parts for any output pin is I_{OL} = 12 mA.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	TECH
74ACT793	N,J	Com	Non-invert	Latch	CMOS
74ACT794	N,J	Com		Register	

Logic Symbols



'ACT793 Function Table

G	$\overline{OE}$	Q	D
L	L	Q_0**	Output, Q
L	H	Q_0**	Input
H†	L	D*	Output, Q*
H	H	D	Input

* In this case the output of the latch feeds the input, and a "race" condition results.

** Q_0 represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards.

'ACT794 Function Table

CK	$\overline{OE}$	Q	D
L or H or ↓	L	Q_0	Output, Q
L or H or ↓	H	Q_0	Input
↑	L	Q_0	Output, Q*
↑	H	D	Input

* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_0.

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Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... -0.5 V to 7.0 V
DC input voltage, V_I ..... -0.5 V to V_{CC} +0.5 V
DC output voltage, V_O ..... -0.5 V to V_{CC} +0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
V_I <0 ..... -20 mA
V_I >V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O <0 ..... -20 mA
V_O >V_{CC} ..... +20 mA
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		-40		85	°C
t_w	Width of Clock/Gate	High	15			ns
		Low	15			
t_{su}	Setup time	'ACT793	8↓			ns
		'ACT794	25↑			
t_h	Hold time	'ACT793	8↑			
		'ACT794	0↑			
t_r	Input rise time at V_I = 4.5 V		0		500	ns
t_f	Input fall time at V_I = 4.5 V		0		500	ns
I_{OH}	High-level output current				-6	mA
I_{OL}	Low-level output current				12	mA

↑ ↓ The arrows indicates the transition of the clock/gate input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
I_{IN}	Input current	V_{CC} = MAX	V_I = V_{CC} or GND			±1.0	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20 µA			0.1	V
			I_{OL} = 6 mA			0.37	
			I_{OL} = 12 mA			0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -20 µA	3.4			V
			I_{OH} = -6 mA	2.4			
I_{OZ}	Off-state output current	V_{CC} = MAX	V_O = V_{CC} or GND			±30	µA
I_{CC}	Quiescent supply current	V_{CC} = MAX	V_I = V_{CC} or GND			80	µA

Switching Characteristics for 'ACT793

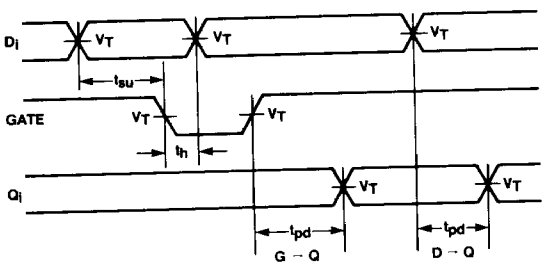
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF		40	ns
t_{PHL}				40	
t_{PLH}	Gate to output delay			40	ns
t_{PHL}				40	
t_{PZL}	Output enable delay†	R_L = 1 K Ω C_L = 50 pF		30	ns
t_{PZH}				30	
t_{PLZ}	Output disable delay†			33	ns
t_{PHZ}				33	

† For the 'ACT793, G should remain LOW during these tests.

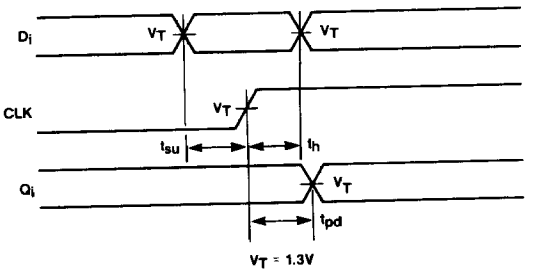
Switching Characteristics for 'ACT794

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{PLH}	Clock to output delay	C_L = 50 pF		40	ns
t_{PHL}				40	
t_{PZL}	Output enable delay	R_L = 1 K Ω C_L = 50 pF		30	ns
t_{PZH}				30	
t_{PLZ}	Output disable delay			30	ns
t_{PHZ}				30	

'ACT793 Timing Diagrams

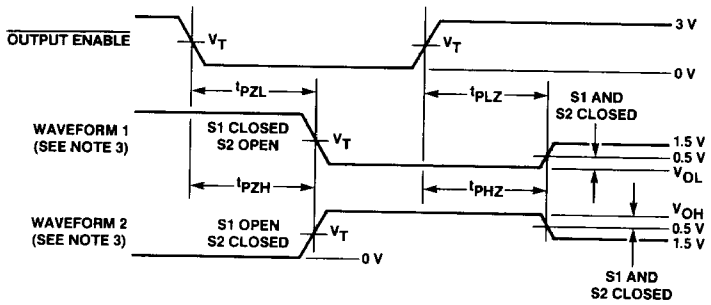


'ACT794 Timing Diagrams

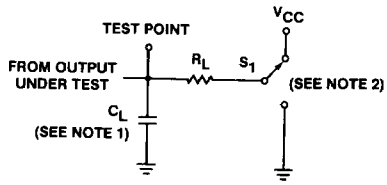


The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. (V_T = 1.3V).

Enable/Disable Waveforms



Standard Test Load



Notes 1. C_L includes probbe and jig capacitance.

2. When measuring t_{PLZ} and t_{PZL}, S_1 is tied to V_{CC}. When measuring t_{PHZ} and t_{PZH}, S_1 is tied to ground.

   When measuring propagation delay times of three-state outputs, S_1 is open, i.e., not connected to V_{CC} or ground.

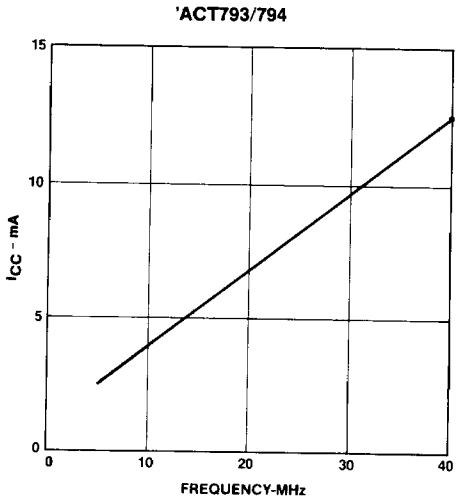
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.

   Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.

4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

5. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $t_r \leq 5$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\,\Omega$.

Typical I_{CC} vs Frequency



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