MX29LV040C

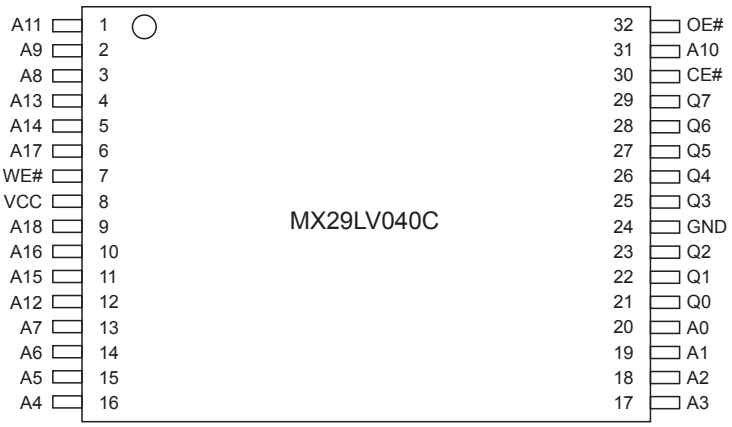
4M-BIT [512K x 8] CMOS SINGLE VOLTAGE 3V ONLY EQUAL SECTOR FLASH MEMORY

FEATURES

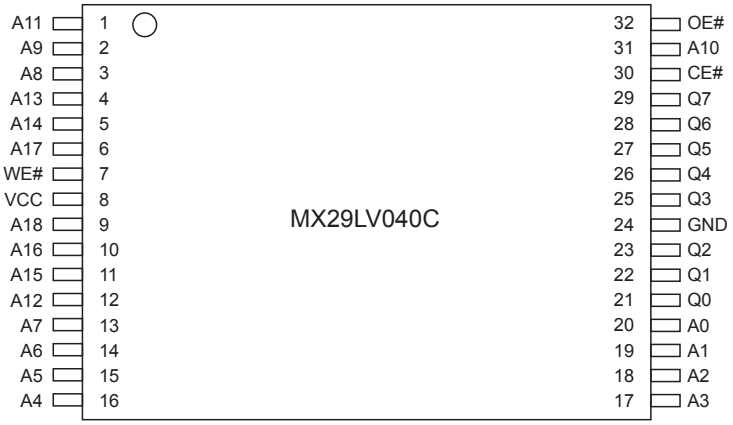
- Extended single - supply voltage range 2.7V to 3.6V
- 524,288 x 8 only
- Single power supply operation
  - 3.0V only operation for read, erase and program operation
- **Fully compatible with MX29LV040 device**
- Fast access time: 55R/70/90ns
- Low power consumption
  - 30mA maximum active current
  - 0.2uA typical standby current
- Command register architecture
  - 8 equal sector of 64K-Byte each
  - Byte Programming (9us typical)
  - Sector Erase (Sector structure 64K-Byte x8)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability
  - Automatically program and verify data at specified address
- Erase suspend/Erase Resume
  - Suspends sector erase operation to read data from, or program data to, any sector that is not being erased, then resumes the erase
- Status Reply
  - Data# Polling & Toggle bit for detection of program and erase operation completion
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Any combination of sectors can be erased with erase suspend/resume function
- CFI (Common Flash Interface) compliant
  - Flash device parameters stored on the device and provide the host system to access
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Package type:
  - 32-pin PLCC
  - 32-pin TSOP (8mmx20mm, 8mmx14mm)
  - **All Pb-free devices are RoHS Compliant**

PIN CONFIGURATIONS

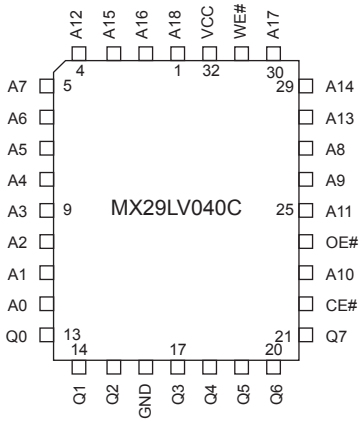
32 TSOP (Standard Type) (8mm x 20mm)



32 TSOP (8mm x 14mm)



32 PLCC



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
GND	Ground Pin
VCC	+3.0V single power supply

BLOCK DIAGRAM

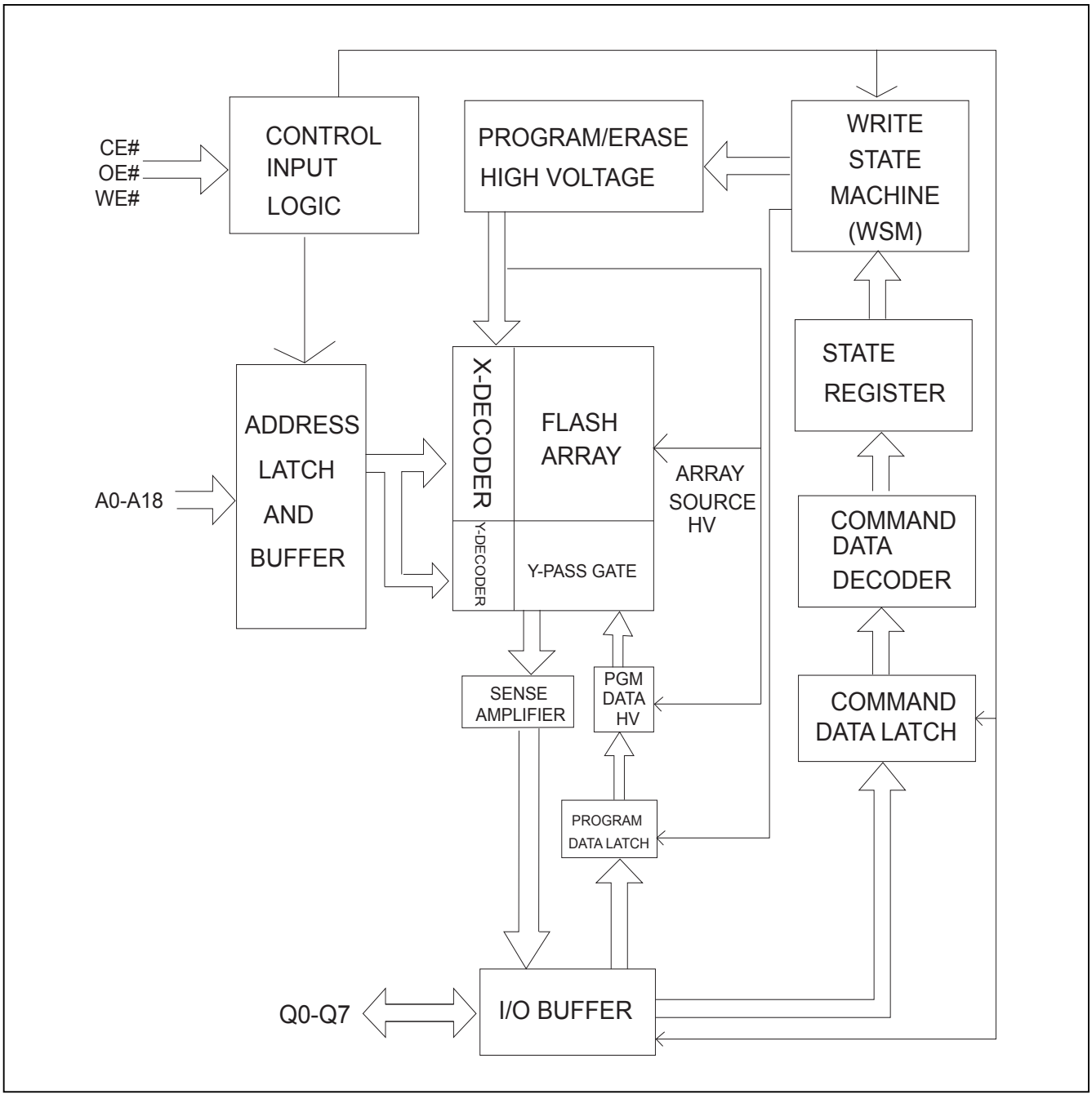


Table 1. SECTOR (GROUP) STRUCTURE

Sector	A18	A17	A16	Address Range
SA0	0	0	0	00000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

Note:All sectors are 64 Kbytes in size.

Table 2-1. BUS OPERATION

Operation	CE#	OE#	WE#	Address	Q0~Q7
Read Mode	L	L	H	AIN	DOUT
Write	L	H	L	AIN	DIN
Standby Mode	Vcc±0.3V	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z

Table 2-2. BUS OPERATION

Operation	CE#	OE#	WE#	A0	A1	A6	A9	Q0~Q7
Read Silicon ID Manufactures Code	L	L	H	L	L	X	Vhv	C2H
Read Silicon ID Device Code	L	L	H	H	L	X	Vhv	4FH
Sector Protect	L	Vhv	L	X	X	L	Vhv	X
Chip Unprotected	L	Vhv	L	X	X	H	Vhv	X
Sector Protect Verify	L	L	H	X	H	X	Vhv	Code(1)

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. AM: MSB of address.
3. Sector addresses: A18~A16.
4. Vhv is 11.5V to 12.5V.
5. X means don't care.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in the array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready1 and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

SECTOR PROTECT OPERATION

When a sector is protected, program or erase operation will be disabled on that protected sector. MX29LV040C provides a methods for sector protection.

The method is asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LV040C provides one methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sector groups are unprotected when shipped from the factory.

The method is asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR PROTECT STATUS OPERATION

MX29LV040C provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires Vhv on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A16 to A18 pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than 1.4V. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than 1.4V and write cycles are ignored until Vcc is greater than 1.4V. System must provide proper signals on control pins after Vcc is larger than 1.4V to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29LV040C is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

TABLE 3. MX29LV040C COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select			Program	Chip Erase	Sector Erase	CFI Read	Erase Suspend	Erase Resume
				Silicon ID	Device ID	Sector Protect Verify						
1st Bus Cyc	Addr	Addr	XXX	555	555	555	555	555	555	AA	XXX	XXX
	Data	Data	F0	AA	AA	AA	AA	AA	AA	98	B0	30
2nd Bus Cyc	Addr			2AA	2AA	2AA	2AA	2AA	2AA			
	Data			55	55	55	55	55	55			
3rd Bus Cyc	Addr			555	555	555	555	555	555			
	Data			90	90	90	A0	80	80			
4th Bus Cyc	Addr			X00	X01	(Sector) X02	Addr	555	555			
	Data			C2	4F	00/01	Data	AA	AA			
5th Bus Cyc	Addr							2AA	2AA			
	Data							55	55			
6th Bus Cyc	Addr							555	Sector			
	Data							10	30			

Notes:
1. It is not allowed to adopt any other code which is not in the above command definition table.

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC PROGRAMMING

The MX29LV040C can provide the user program function by the form of Byte-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

The typical chip program time at room temperature of the MX29LV040C is less than 4.5 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5
In progress*1	Q7#	Toggling	0
Finished	Q7	Stop toggling	0
Exceed time limit	Q7#	Toggling	1

*1: The status "in progress" means both program mode and erase-suspended program mode.
*2: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programing the data in the protected sector.

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware reset or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2
In progress	0	Toggling	0	Toggling
Finished	1	Stop toggling	0	1
Exceed time limit	0	Toggling	1	Toggling

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q3	Q2
Time-out period	0	Toggling	0	0	Toggling
In progress	0	Toggling	0	1	Toggling
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	1	Toggling

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.
*2: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1 (<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

Status	Q7	Q6	Q5	Q3	Q2
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 400uS interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV040C features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh", the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4.

Once user enters CFI query mode, user can not issue any other commands except reset command. The reset command is required to exit CFI mode and go back to the mode before entering CFI. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Byte Mode)	Data (h)
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0002
	14	0000
Address for primary algorithm extended query table	15	0040
	16	0000
Alternate vendor command set and control interface ID code (none)	17	0000
	18	0000
Address for alternate algorithm extended query table (none)	19	0000
	1A	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address (h) (Byte Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	0027
Vcc supply maximum program/erase voltage	1C	0036
VPP supply minimum program/erase voltage	1D	0000
VPP supply maximum program/erase voltage	1E	0000
Typical timeout per single word/byte write, 2^n us	1F	0004
Typical timeout for maximum-size buffer write, 2^n us	20	0000
Typical timeout per individual block erase, 2^n ms	21	000A
Typical timeout for full chip erase, 2^n ms	22	0000
Maximum timeout for word/byte write, 2^n times typical	23	0005
Maximum timeout for buffer write, 2^n times typical	24	0000
Maximum timeout per individual block erase, 2^n times typical	25	0004
Maximum timeout for chip erase, 2^n times typical	26	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address (h) (Byte Mode)	Data (h)
Device size = 2^n in number of bytes	27	0013
Flash device interface description (02=asynchronous x8/x16)	28	0000
	29	0000
Maximum number of bytes in buffer write = 2^n (not support)	2A	0000
	2B	0000
Number of erase regions within device	2C	0001
Index for Erase Bank Area 1	2D	0007
	2E	0000
	2F	0000
	30	0001
Index for Erase Bank Area 2	31	0000
	32	0000
	33	0000
	34	0000
Index for Erase Bank Area 3	35	0000
	36	0000
	37	0000
	38	0000
Index for Erase Bank Area 4	39	0000
	3A	0000
	3B	0000
	3C	0000

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Byte Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	0050
	41	0052
	42	0049
Major version number, ASCII	43	0031
Minor version number, ASCII	44	0030
Unlock recognizes address (0= recognize, 1= don't recognize)	45	0001
Erase suspend (2= to both read and program)	46	0002
Sector protect (N= # of sectors/group)	47	0001
Temporary sector unprotect (1=supported)	48	0001
Sector protect/Chip unprotect scheme	49	0004
Simultaneous R/W operation (0=not supported)	4A	0000
Burst mode (0=not supported)	4B	0000
Page mode (0=not supported)	4C	0000

ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias		-65°C to +125°C
Storage Temperature		-65°C to +150°C
Voltage Range	VCC	-0.5V to +4.0 V
	A9 and OE#	-0.5 V to +12.5 V
	The other pins	-0.5V to Vcc +0.5V
Output Short Circuit Current (less than one second)		200 mA

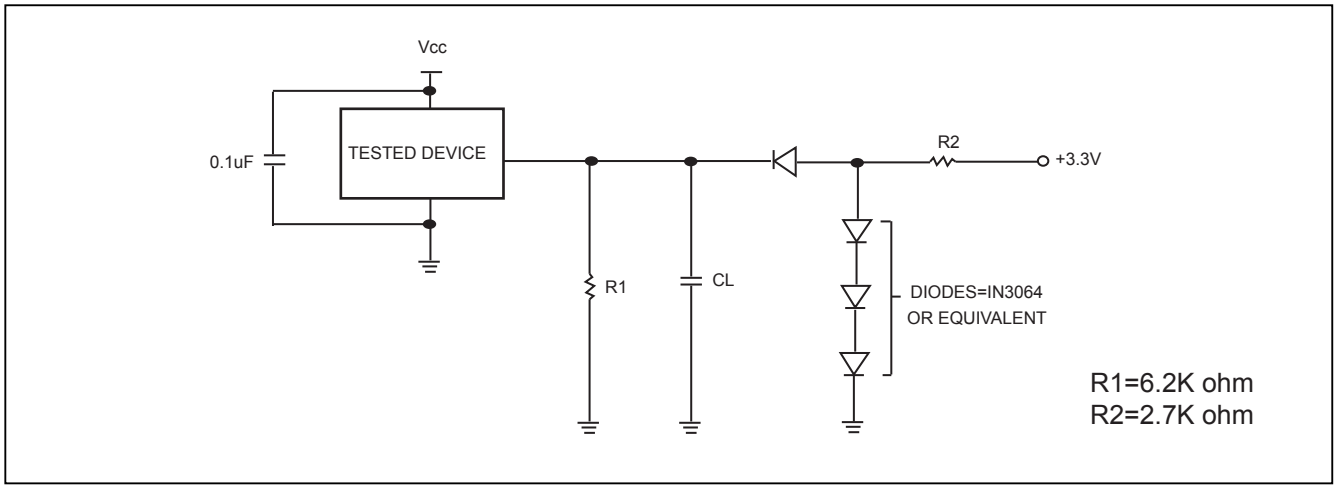
OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade	Surrounding Temperature (T_A)	0°C to +70°C
Industrial (I) Grade	Surrounding Temperature (T_A)	-40°C to +85°C
VCC Supply Voltages	VCC range	+2.7 V to 3.6 V

DC CHARACTERISTICS

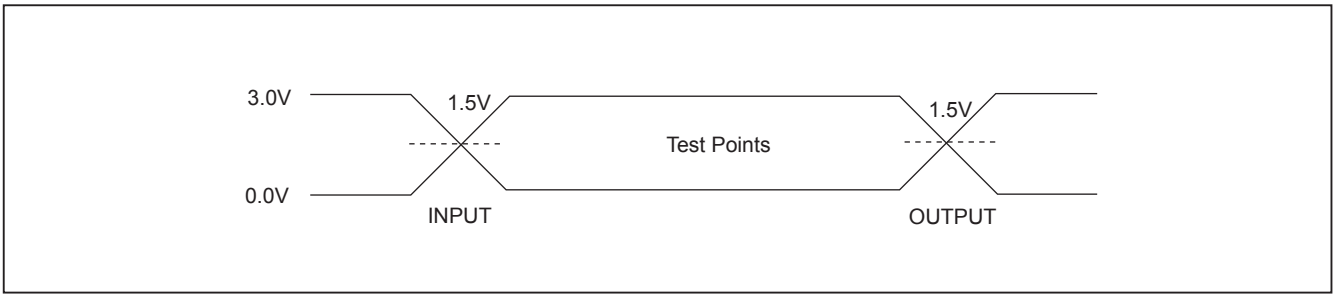
Symbol	Description	Min	Typ	Max	Remark
Iilk	Input Leak			± 1.0uA	
Iilk9	A9 Leak			35uA	A9=12.5V
Iolk	Output Leak			± 1.0uA	
Icr1	Read Current(5MHz)		7mA	12mA	CE#=Vil, OE#=Vih
Icr2	Read Current(1MHz)		2mA	4mA	CE#=Vil, OE#=Vih
Icw	Write Current		15mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		0.2uA	5uA	Vcc=Vcc max, other pin disable
Isbs	Sleep Mode Current		0.2uA	5uA	
Vil	Input Low Voltage	-0.5V		0.8V	
Vih	Input High Voltage	0.7xVcc		Vcc+0.3V	
Vhv	Very High Voltage for hardware Protect/Unprotect/Auto Select	11.5V		12.5V	
Vol	Output Low Voltage			0.45V	Iol=4.0mA
Voh1	Ouput High Voltage	0.85xVcc			Ioh1=-2mA
Voh2	Ouput High Voltage	Vcc-0.4V			Ioh2=-100uA

SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 30pF(70ns)/100pF(90ns)
Rise/Fall Times : 5ns
In/Out reference levels :1.5V

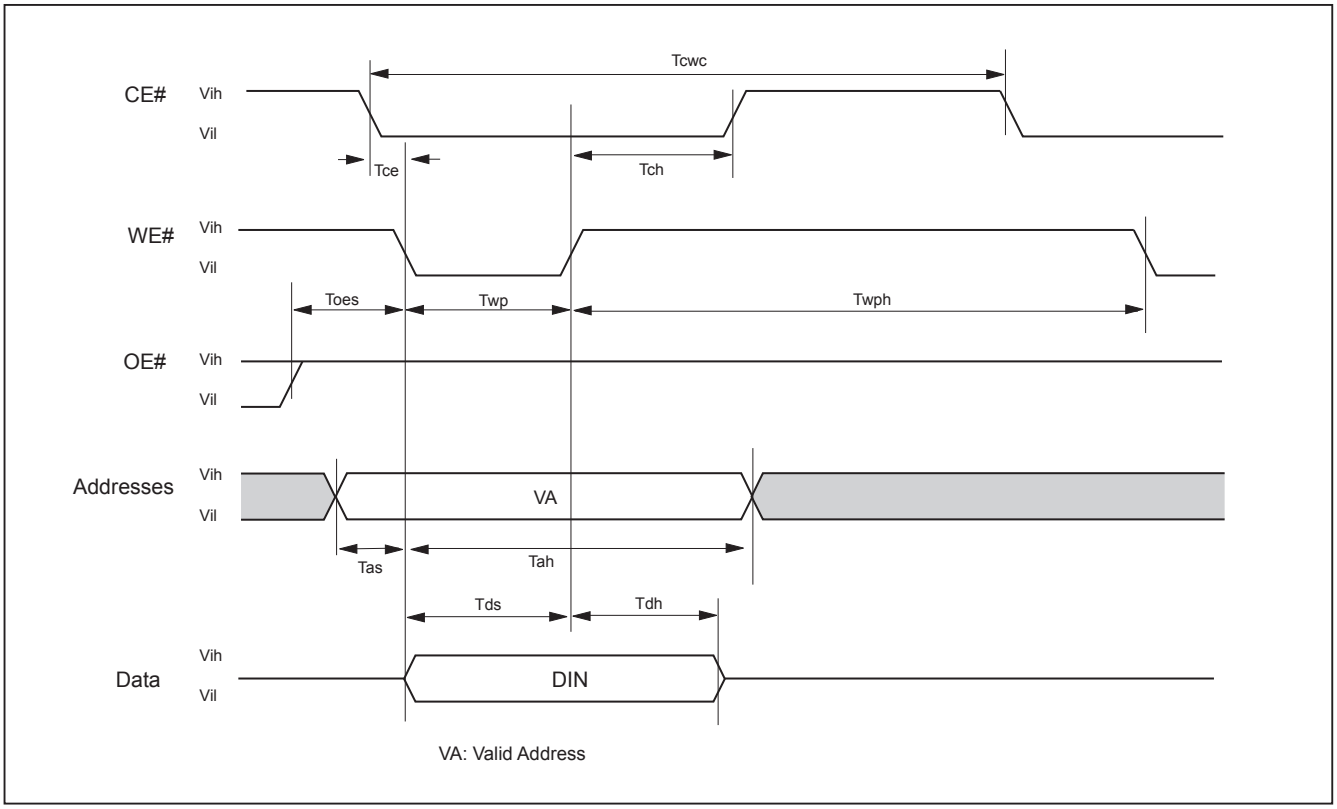
SWITCHING TEST WAVEFORMS



AC CHARACTERISTICS

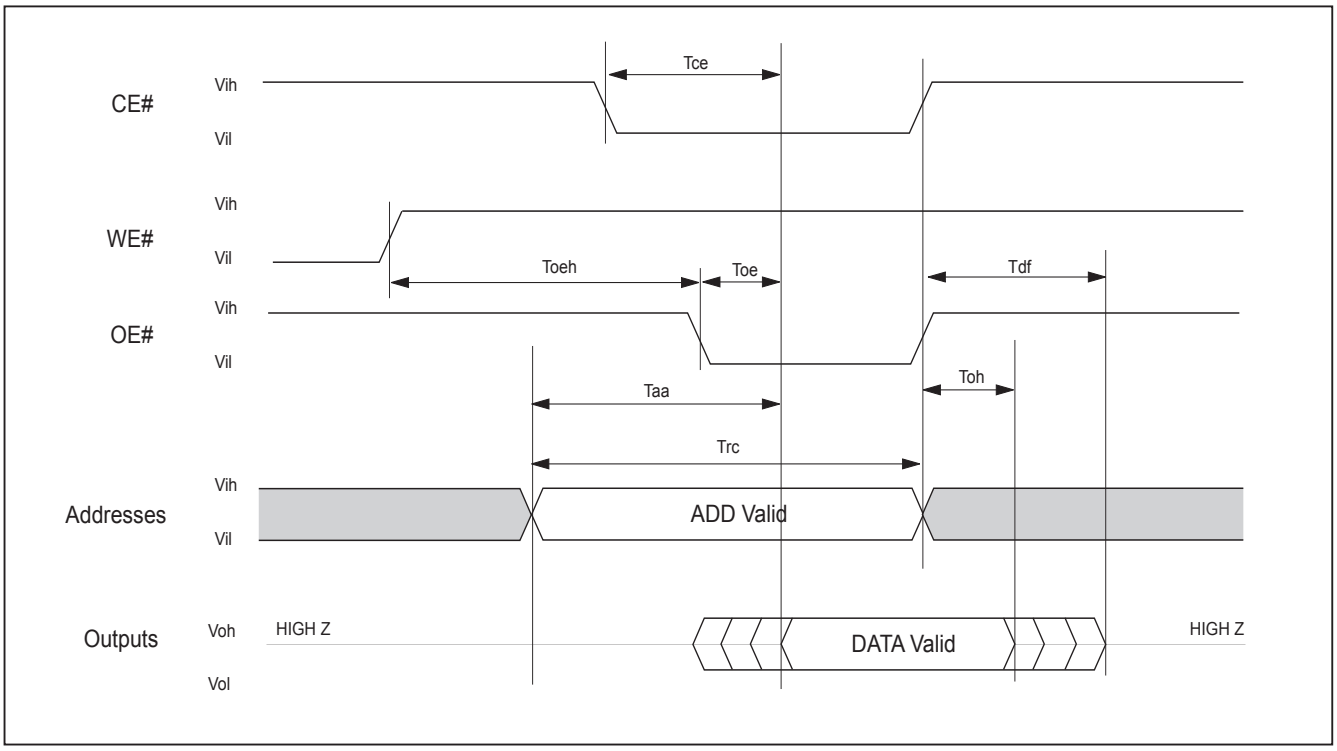
Symbol	Description		Min	Typ	Max	Unit
Taa	Valid data output after address				55/70/90	ns
Tce	Valid data output after CE# low				55/70/90	ns
Toe	Valid data output after OE# low				30/30/35	ns
Tdf	Data output floating after OE# high				25/25/30	ns
Toh	Output hold time from the earliest rising edge of address, CE#, OE#		0			ns
Trc	Read period time		55/70/90			ns
Twc	Write period time		70/90			ns
Tcwc	Command write period time		70/90			ns
Tas	Address setup time		0			ns
Tah	Address hold time		45			ns
Tds	Data setup time		35/45			ns
Tdh	Data hold time		0			ns
Tvcs	Vcc setup time		50			us
Tcs	Chip enable Setup time		0			ns
Tch	Chip enable hold time		0			ns
Toes	Output enable setup time		0			ns
Toeh	Output enable hold time	Read	0			ns
		Toggle & Data# Polling	10			ns
Tws	WE# setup time		0			ns
Twh	WE# hold time		0			ns
Tcep	CE# pulse width		35			ns
Tceph	CE# pulse width high		30			ns
Twp	WE# pulse width		35			ns
Twph	WE# pulse width high		30			ns
Tghwl	Read recover time before write		0			ns
Tghel	Read recover time before write		0			ns
Twhwh1	Program operation			9		us
Twhwh2	Sector erase operation			0.7		sec
Tbal	Sector add hold time				50	us

Figure 1. COMMAND WRITE OPERATION



READ OPERATION

Figure 2. READ TIMING WAVEFORMS



ERASE/PROGRAM OPERATION

Figure 3. AUTOMATIC CHIP ERASE TIMING WAVEFORM

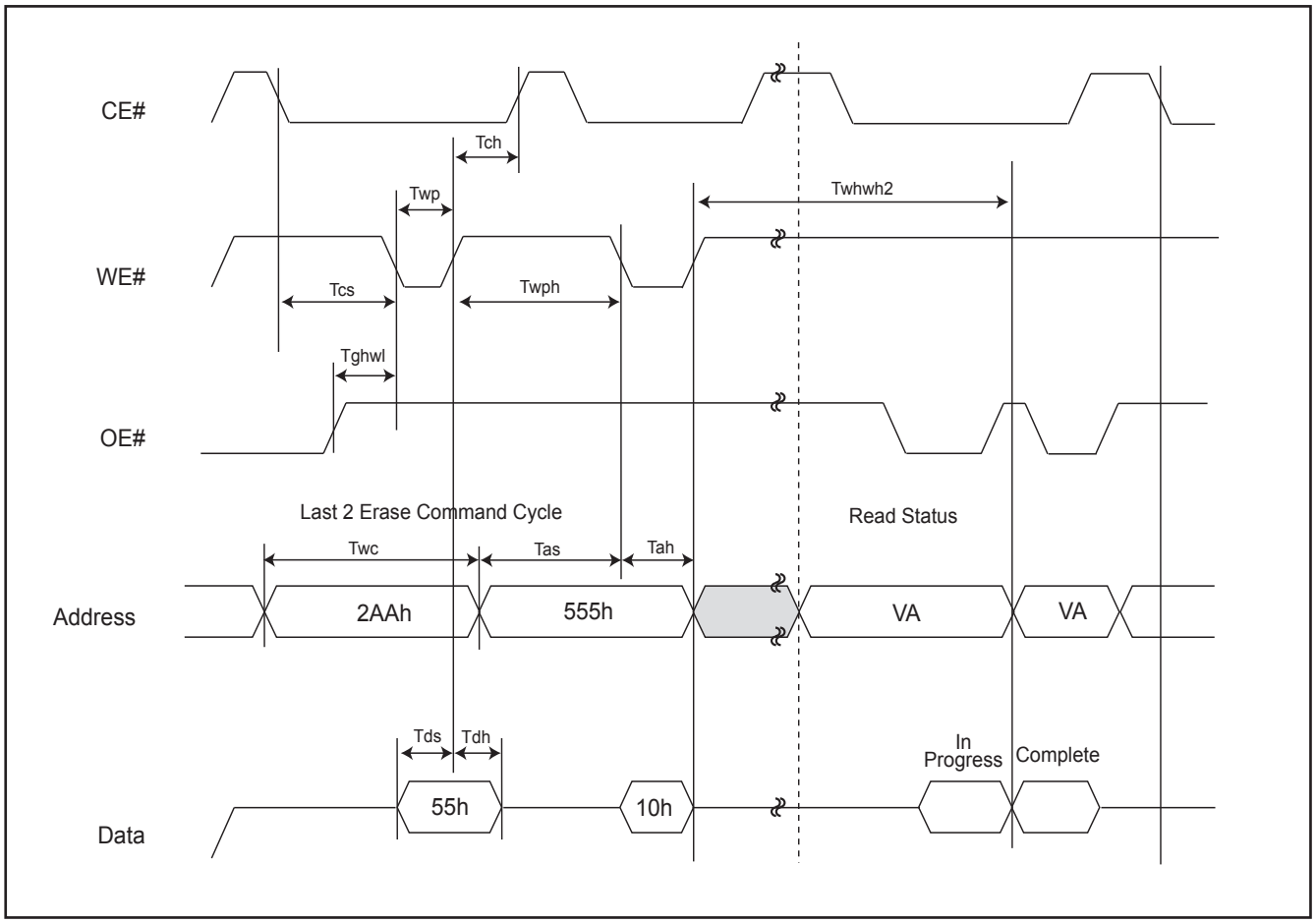


Figure 4. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

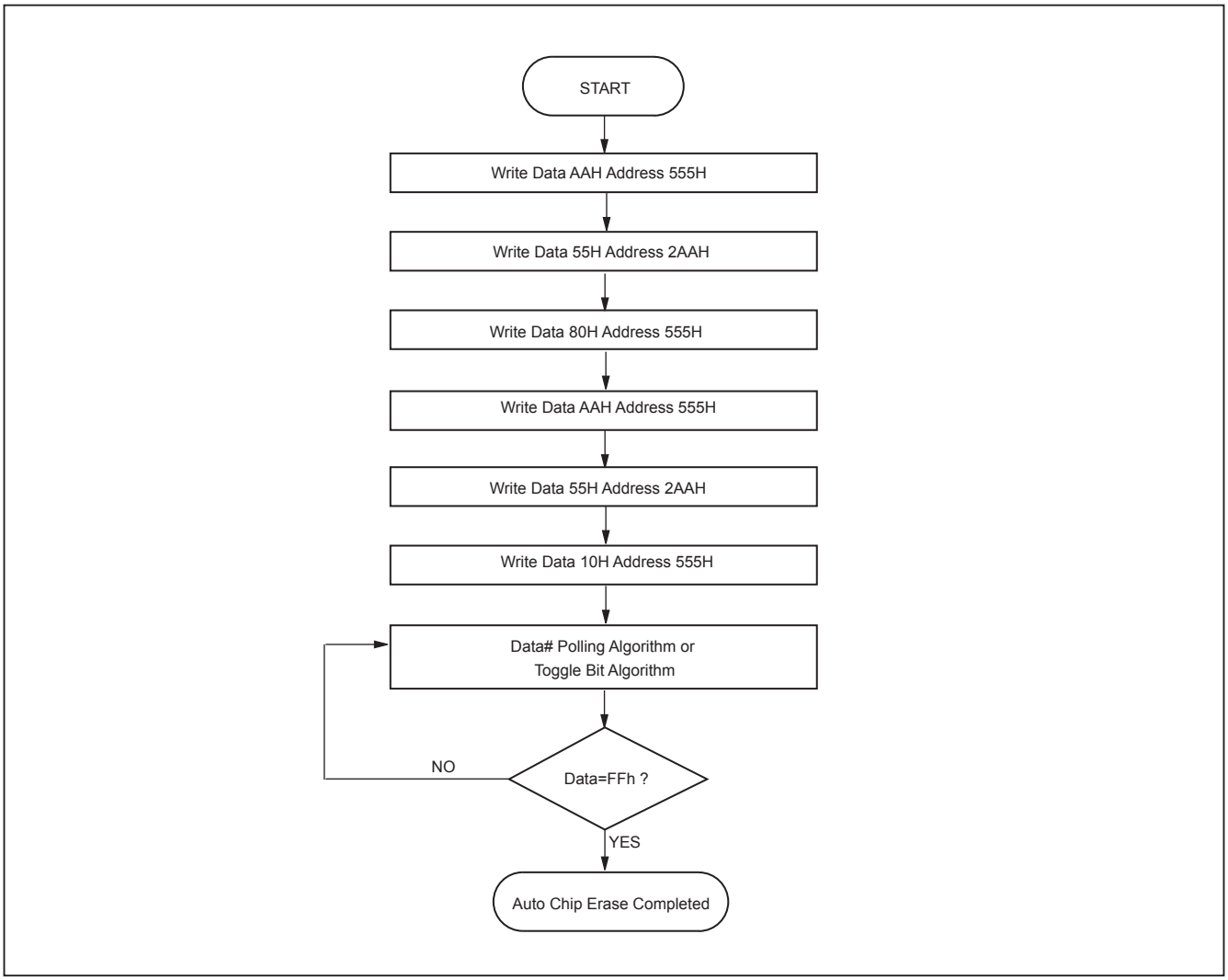


Figure 5. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

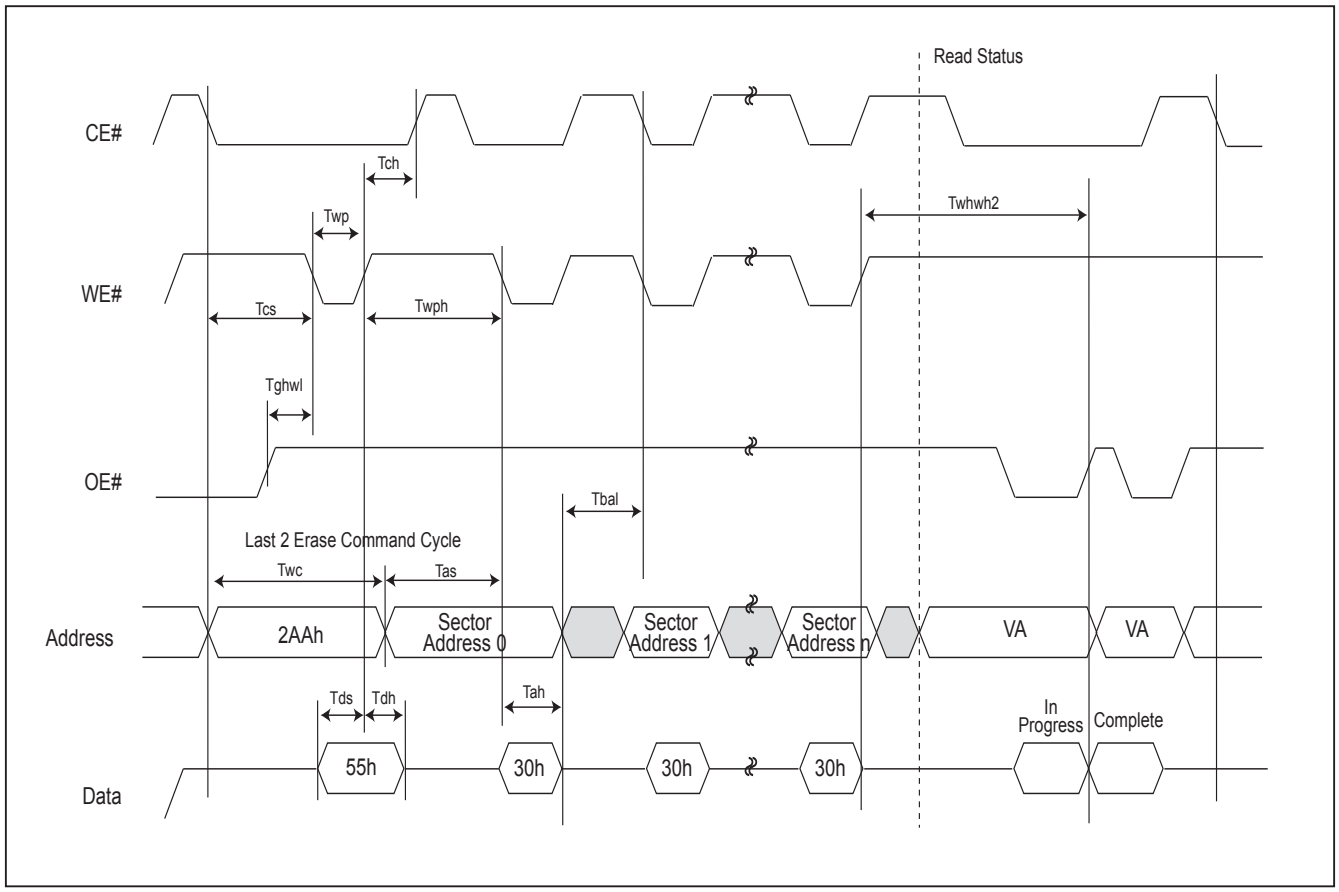


Figure 6. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

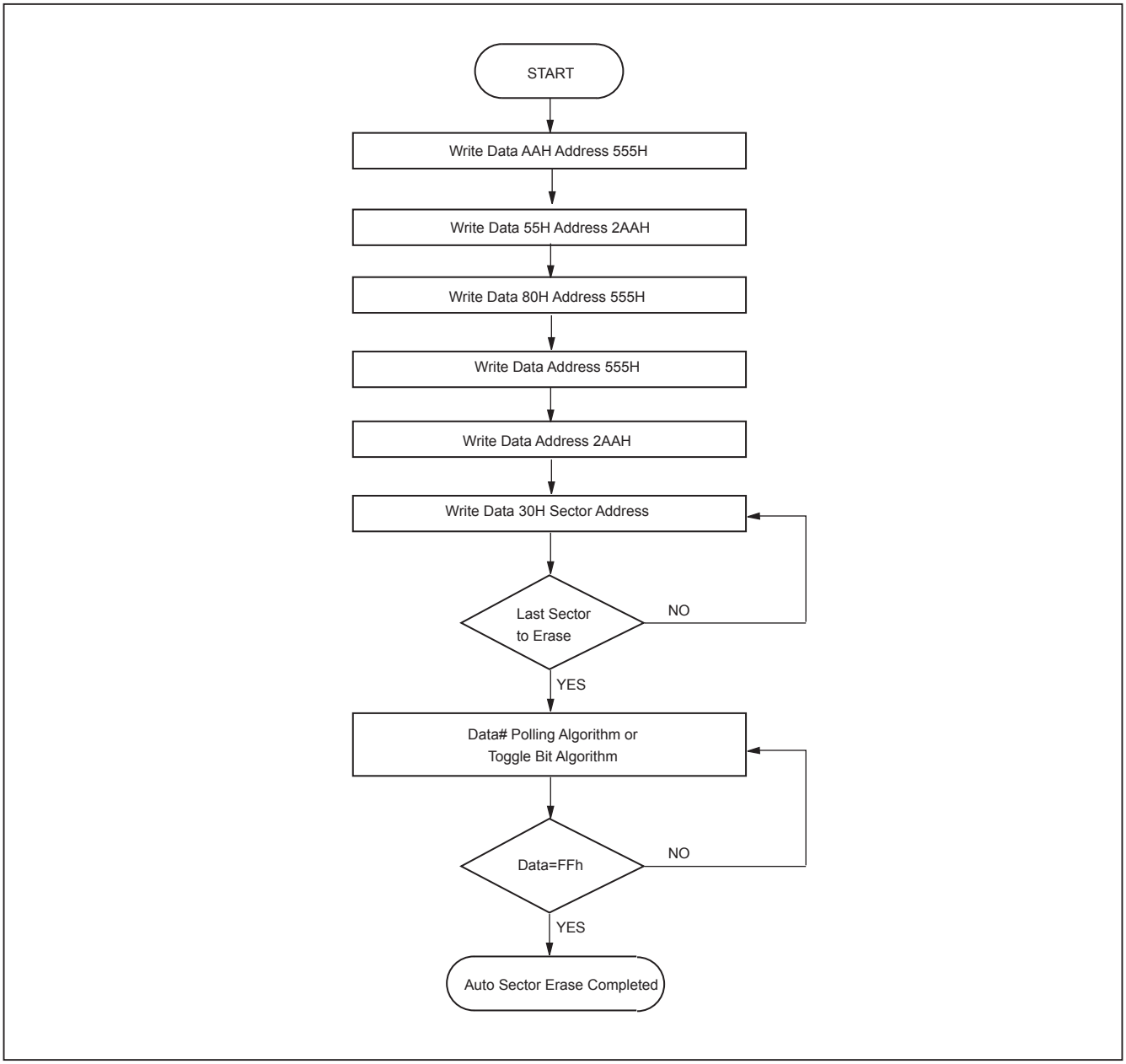


Figure 7. ERASE SUSPEND/RESUME FLOWCHART

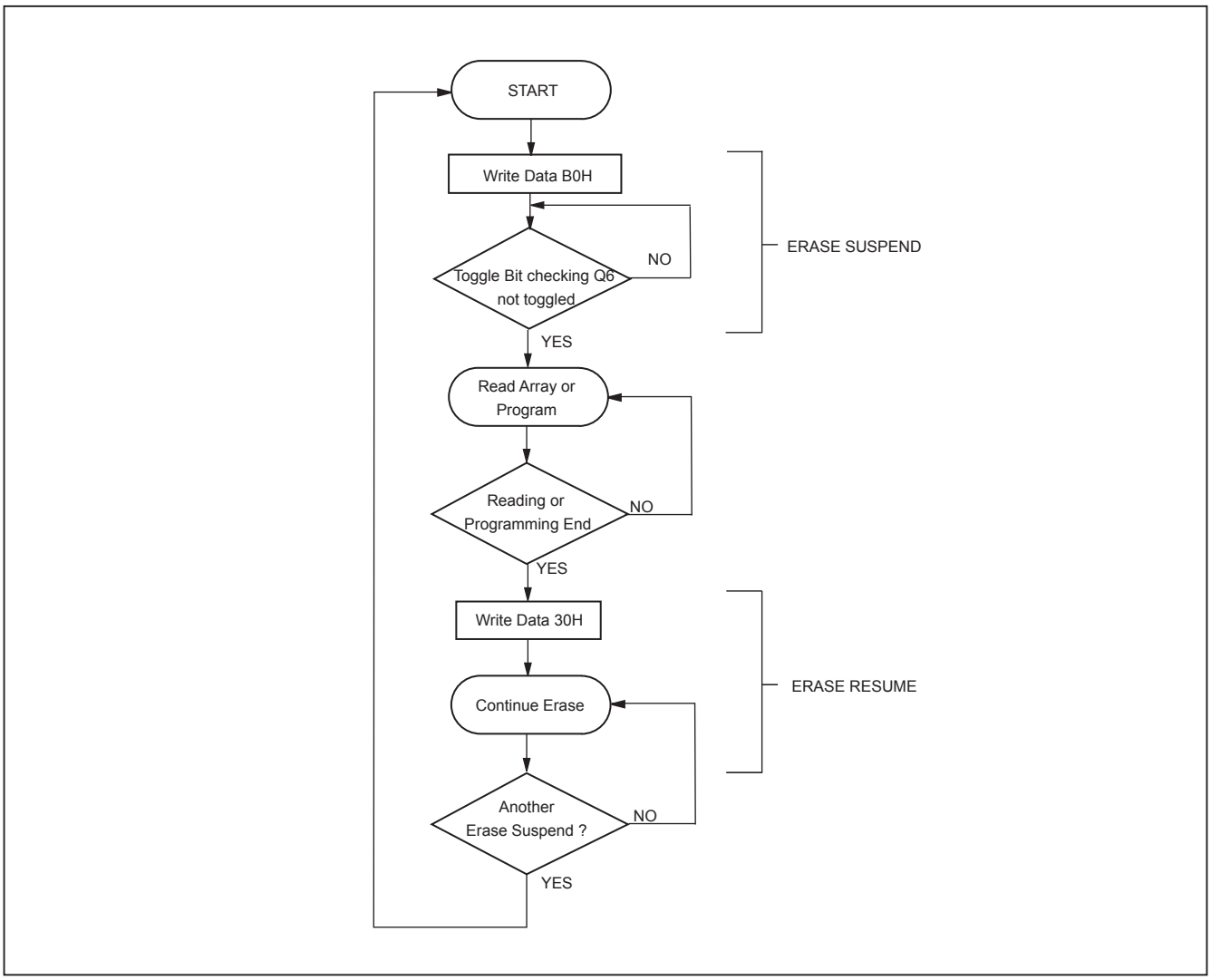


Figure 8. AUTOMATIC PROGRAM TIMING WAVEFORMS

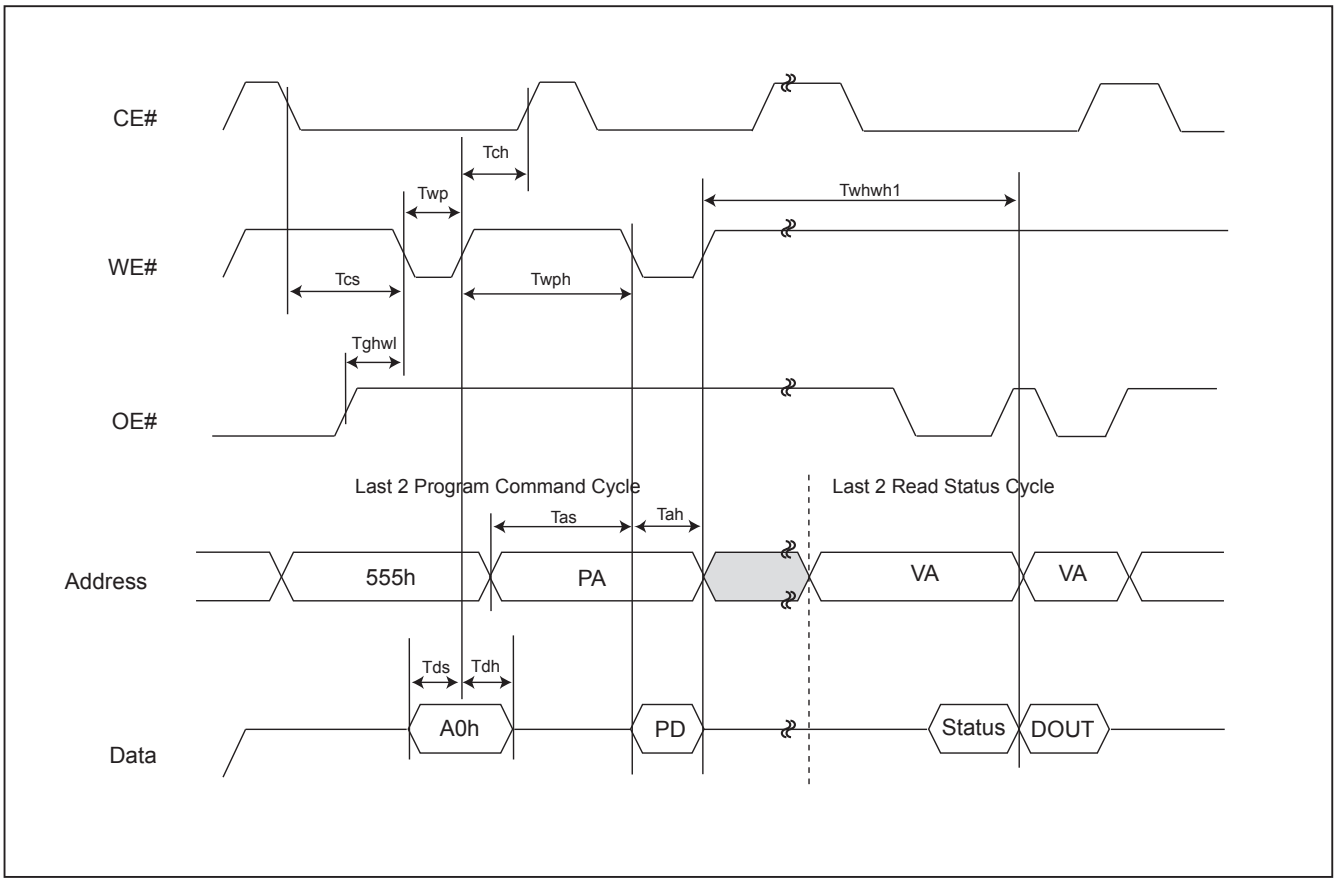


Figure 9. CE# CONTROLLED WRITE TIMING WAVEFORM

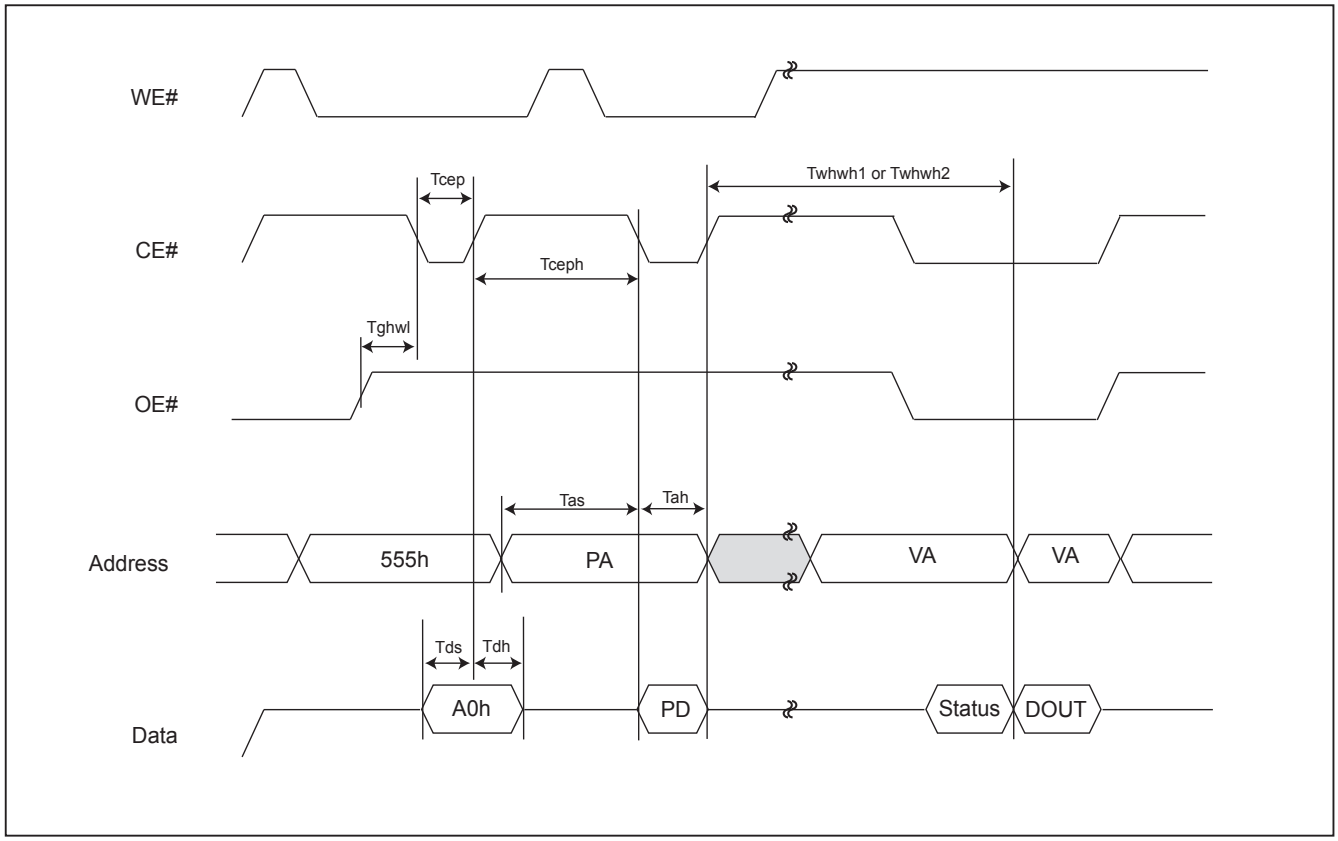
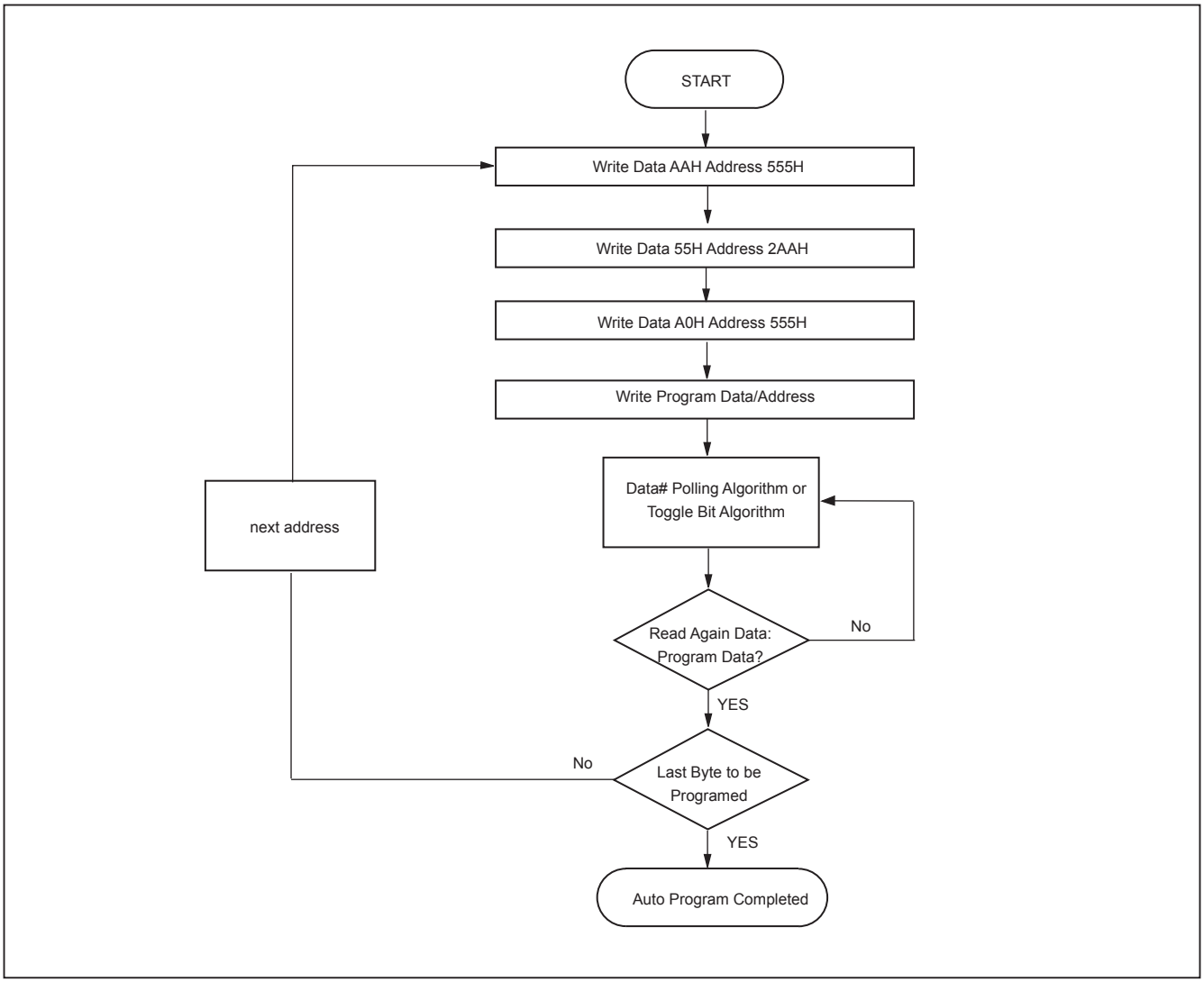


Figure 10. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



SECTOR PROTECT/CHIP UNPROTECT

Figure 11. SECTOR PROTECT/CHIP UNPROTECT WAVEFORM

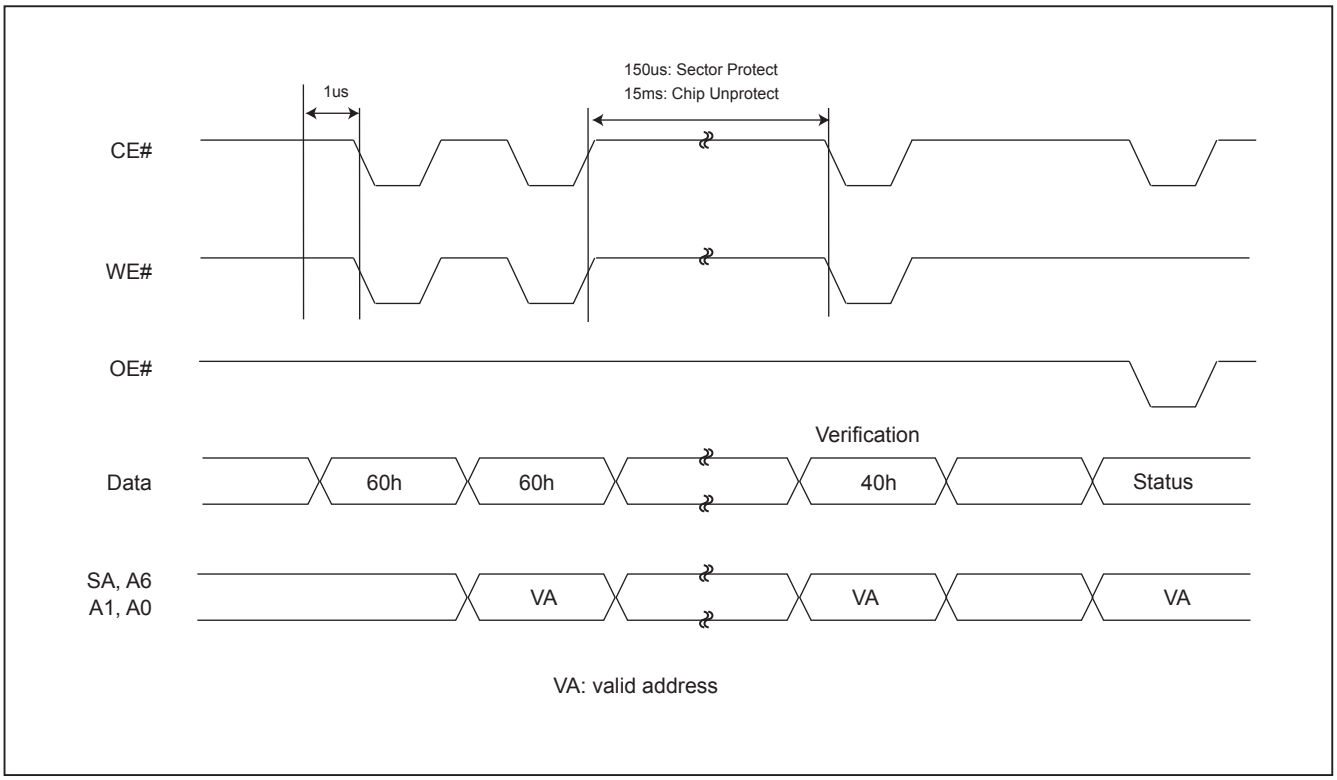
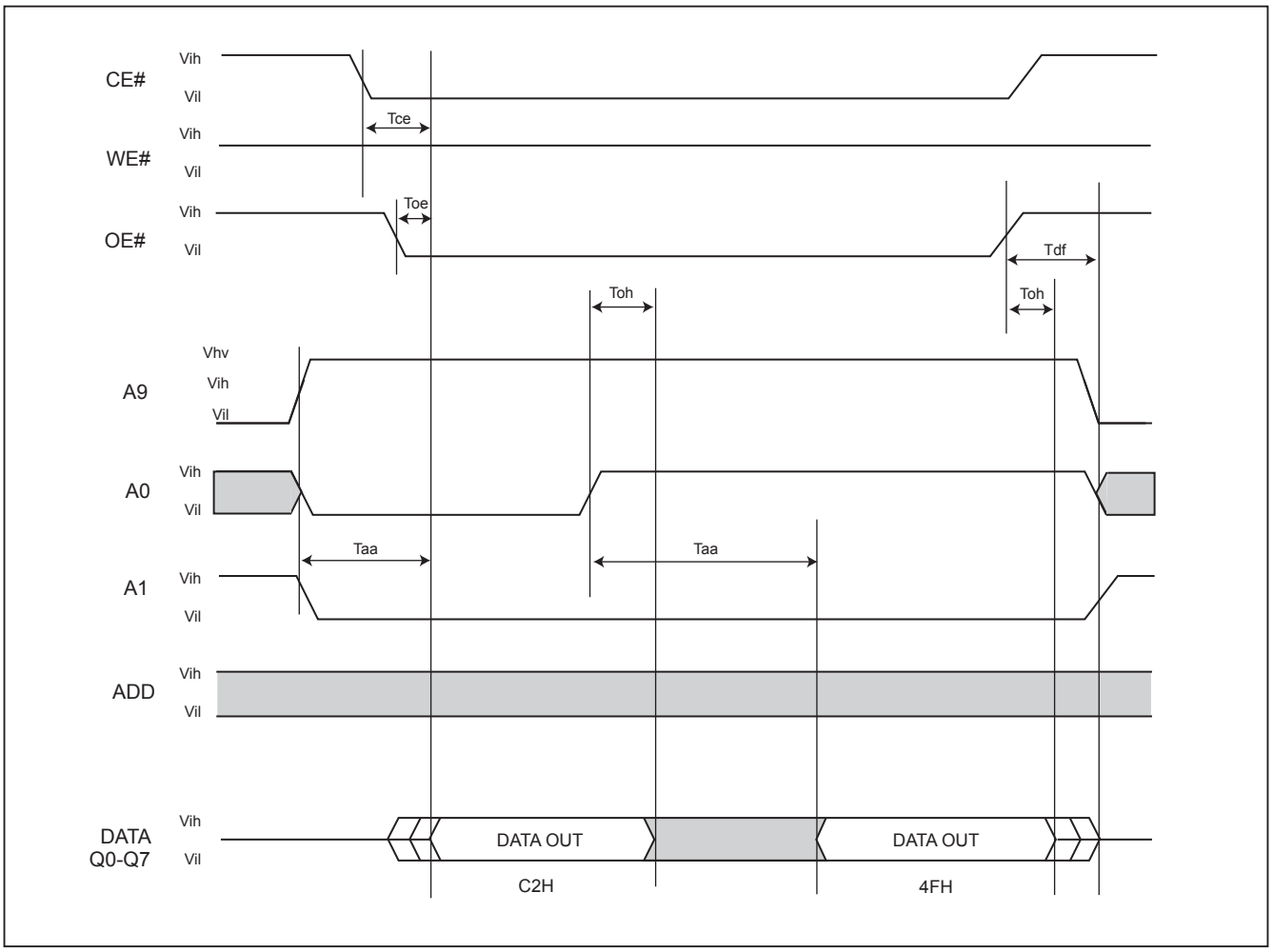


Figure 12. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 13. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

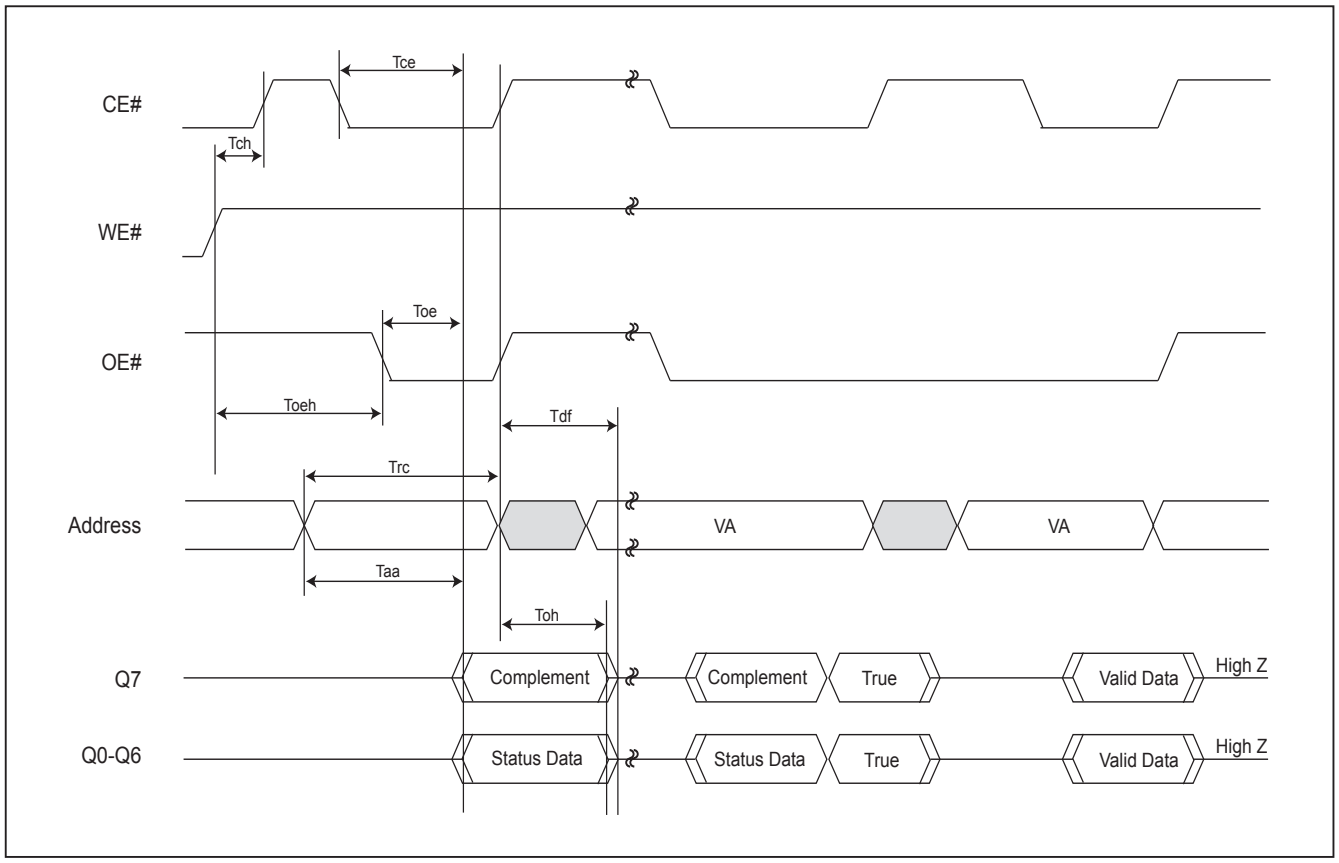
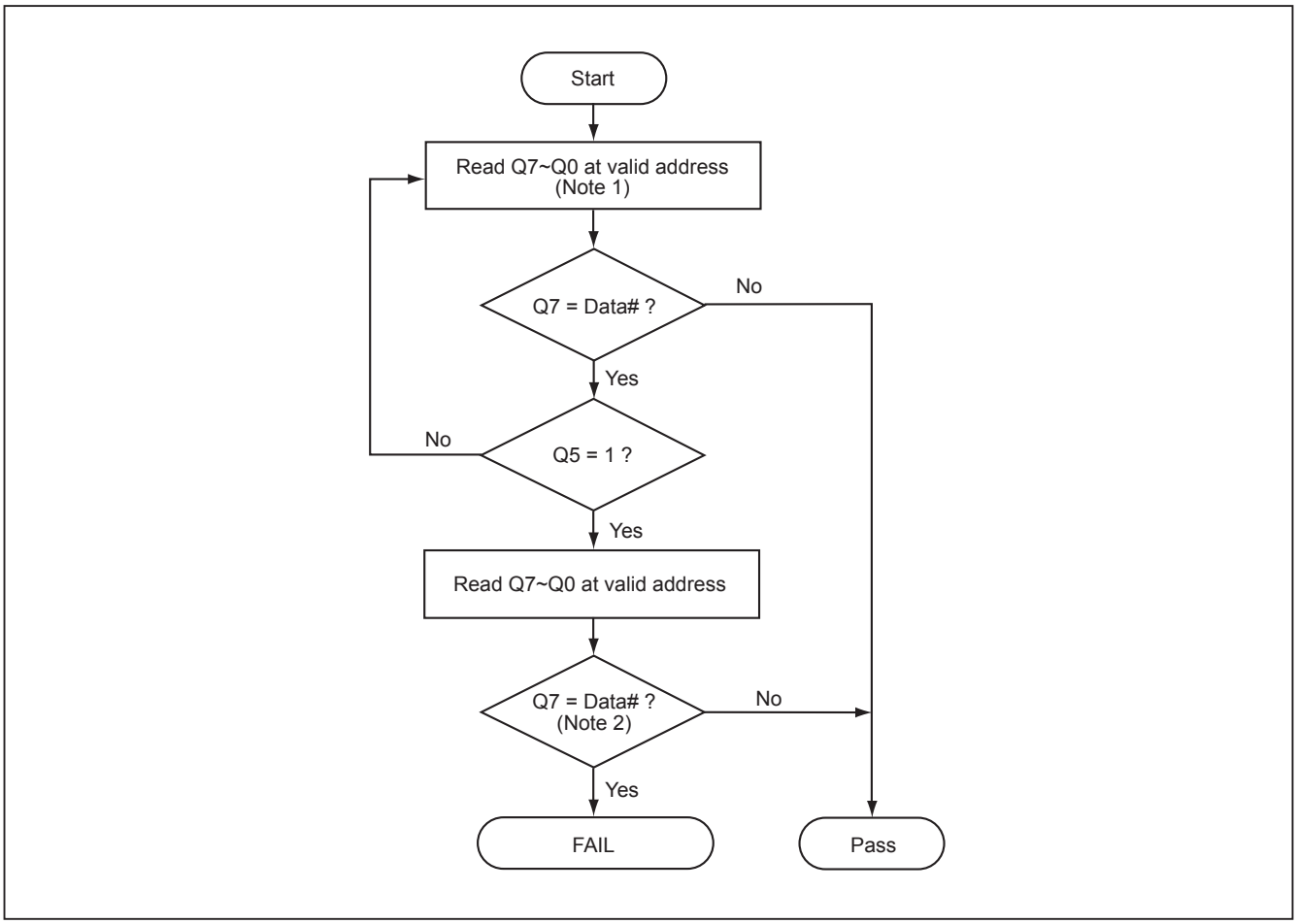


Figure 14. DATA# POLLING ALGORITHM



Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 15. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

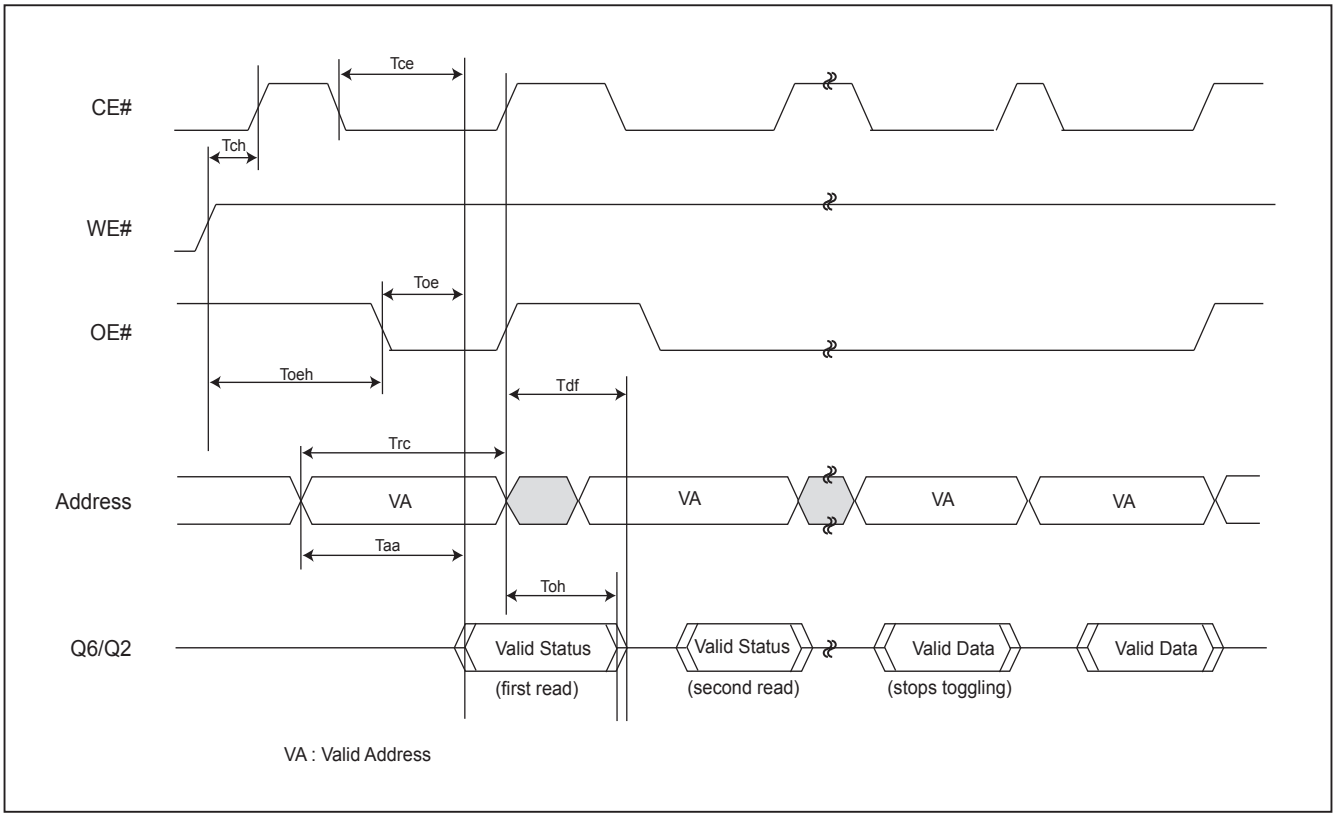
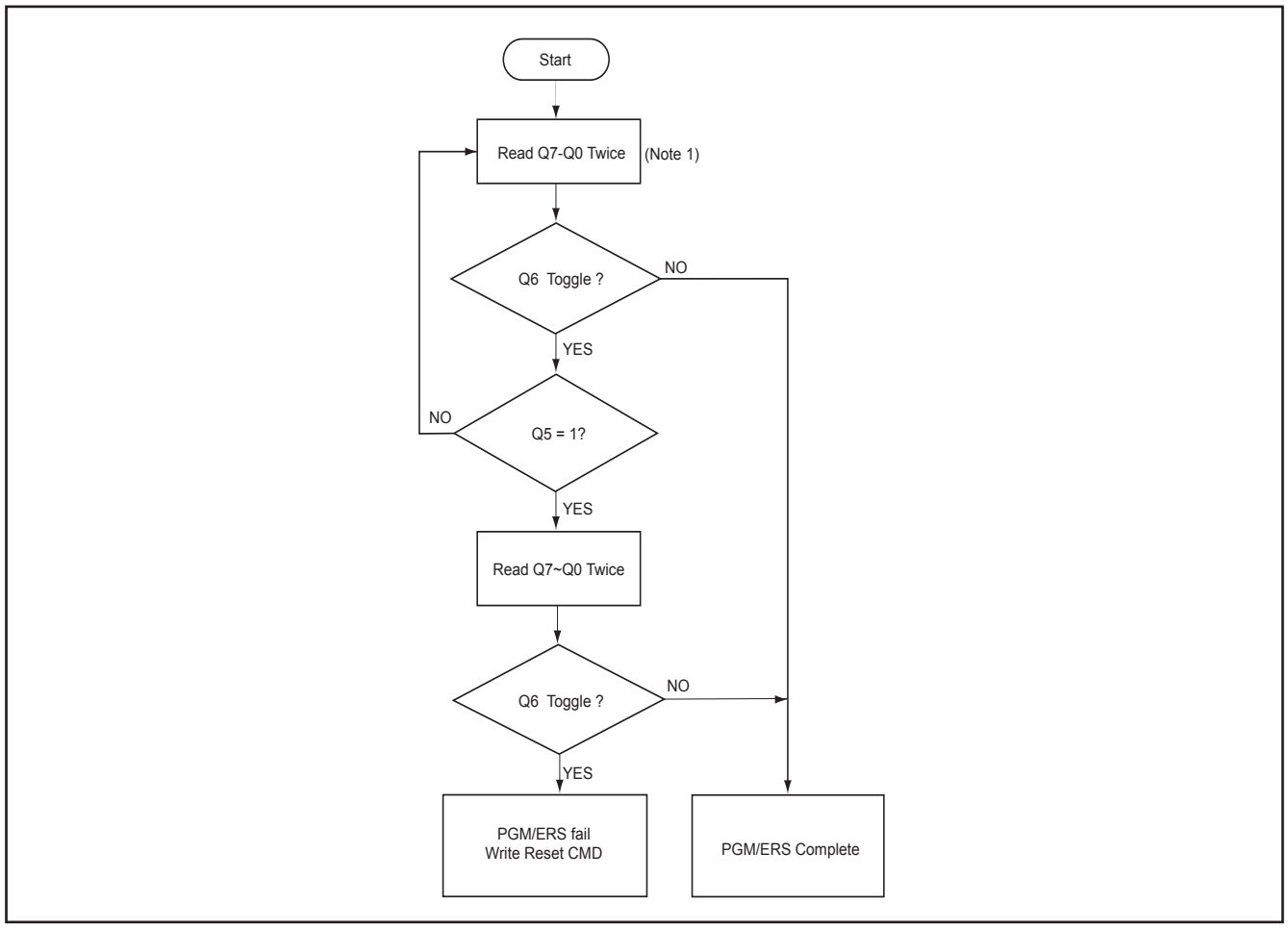


Figure 16. TOGGLE BIT ALGORITHM



Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

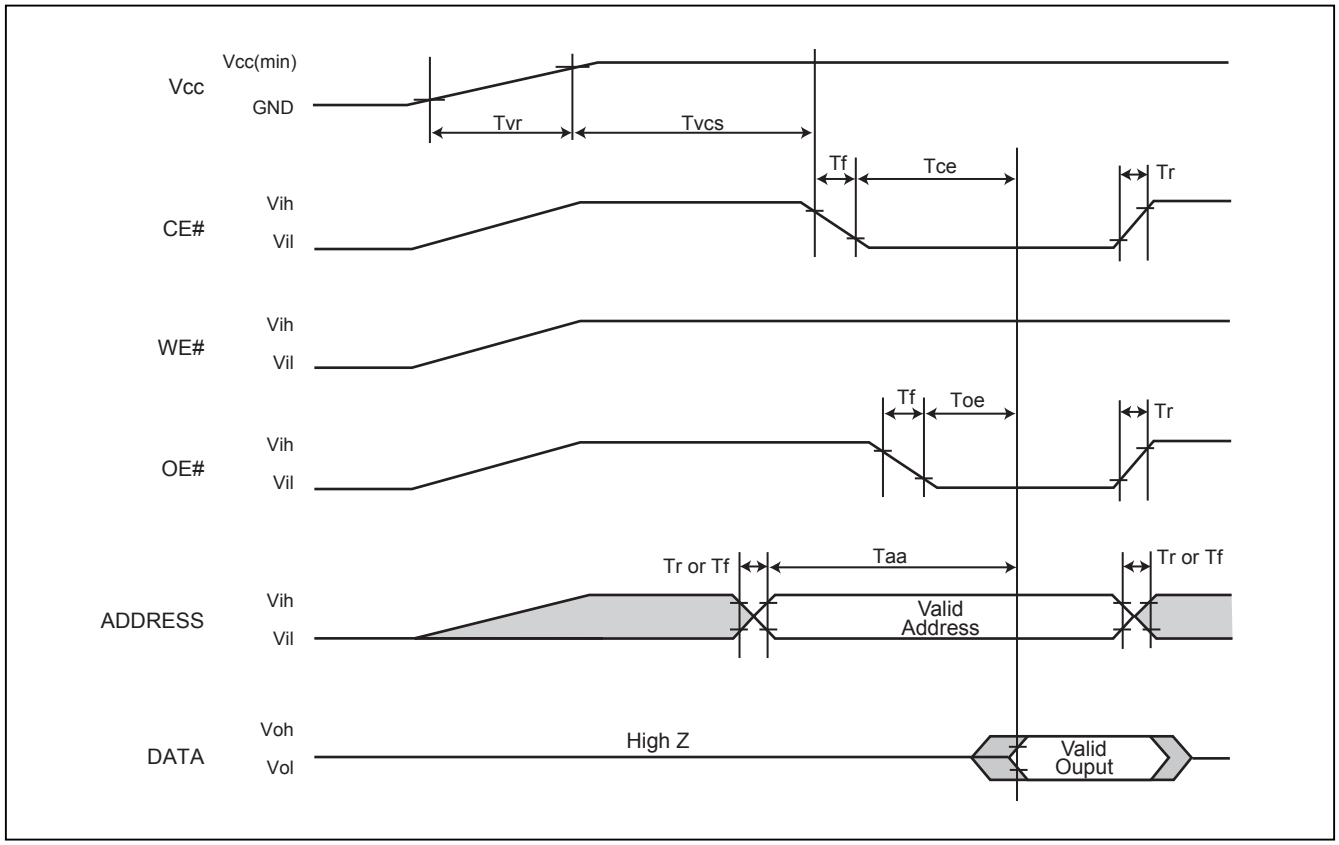


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Chip Erase Time		4	32	sec
Sector Erase Time		0.7	15	sec
Erase/Program Cycles	100,000			Cycles
Chip Programming Time		4.5	13.5	sec
Byte Programming Time		9	300	us

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage difference with GND on A9, OE# pins	-1.0V	12.5V
Input Voltage difference with GND on all I/O pins	-1.0V	Vcc + 1.0V
Input current pulse	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing		

TSOP PIN CAPACITANCE

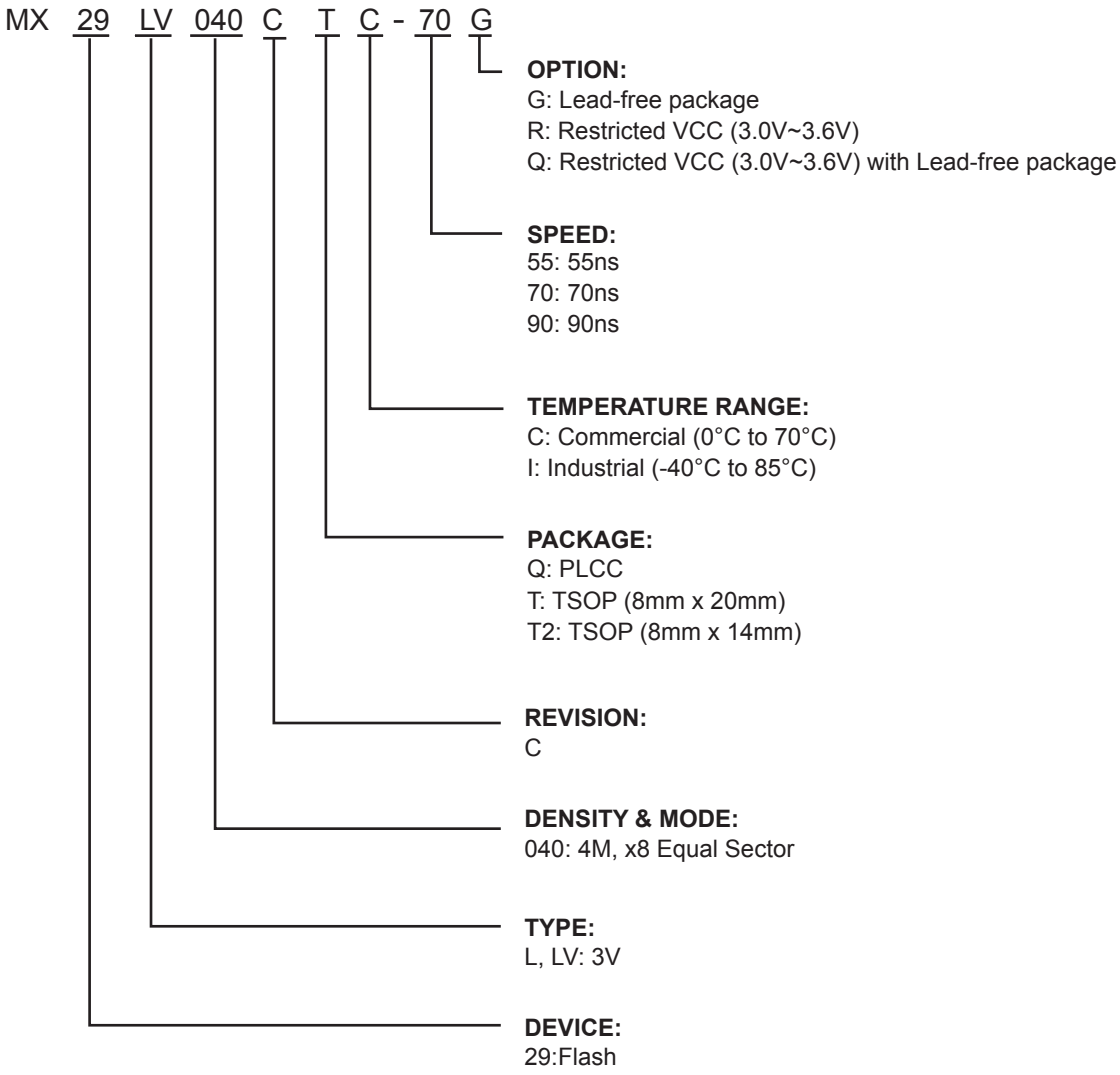
Parameter Symbol	Parameter Description	Test Set	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	12	pF
COUT	Output Capacitance	VOUT=0	12	pF
CIN	Input Capacitance	VIN=0	8	pF

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (uA)	PACKAGE	Remark
MX29LV040CTC-55R	55	30	5	32 Pin TSOP (8x20 mm)	
MX29LV040CTC-70	70	30	5	32 Pin TSOP (8x20 mm)	
MX29LV040CTC-90	90	30	5	32 Pin TSOP (8x20 mm)	
MX29LV040CQC-55R	55	30	5	32 Pin PLCC	
MX29LV040CQC-70	70	30	5	32 Pin PLCC	
MX29LV040CQC-90	90	30	5	32 Pin PLCC	
MX29LV040CTI-55R	55	30	5	32 Pin TSOP (8x20 mm)	
MX29LV040CTI-70	70	30	5	32 Pin TSOP (8x20 mm)	
MX29LV040CTI-90	90	30	5	32 Pin TSOP (8x20 mm)	
MX29LV040CQI-55R	55	30	5	32 Pin PLCC	
MX29LV040CQI-70	70	30	5	32 Pin PLCC	
MX29LV040CQI-90	90	30	5	32 Pin PLCC	
MX29LV040CTC-55Q	55	30	5	32 Pin TSOP (8x20 mm)	PB free
MX29LV040CTC-70G	70	30	5	32 Pin TSOP (8x20 mm)	PB free
MX29LV040CTC-90G	90	30	5	32 Pin TSOP (8x20 mm)	PB free
MX29LV040CQC-55Q	55	30	5	32 Pin PLCC	PB free
MX29LV040CQC-70G	70	30	5	32 Pin PLCC	PB free
MX29LV040CQC-90G	90	30	5	32 Pin PLCC	PB free
MX29LV040CTI-55Q	55	30	5	32 Pin TSOP (8x20 mm)	PB free
MX29LV040CTI-70G	70	30	5	32 Pin TSOP (8x20 mm)	PB free
MX29LV040CTI-90G	90	30	5	32 Pin TSOP (8x20 mm)	PB free
MX29LV040CQI-55Q	55	30	5	32 Pin PLCC	PB free
MX29LV040CQI-70G	70	30	5	32 Pin PLCC	PB free
MX29LV040CQI-90G	90	30	5	32 Pin PLCC	PB free
MX29LV040CT2I-70G*	70	30	5	32 Pin TSOP (8x14 mm)	PB free
MX29LV040CT2I-90G*	90	30	5	32 Pin TSOP (8x14 mm)	PB free

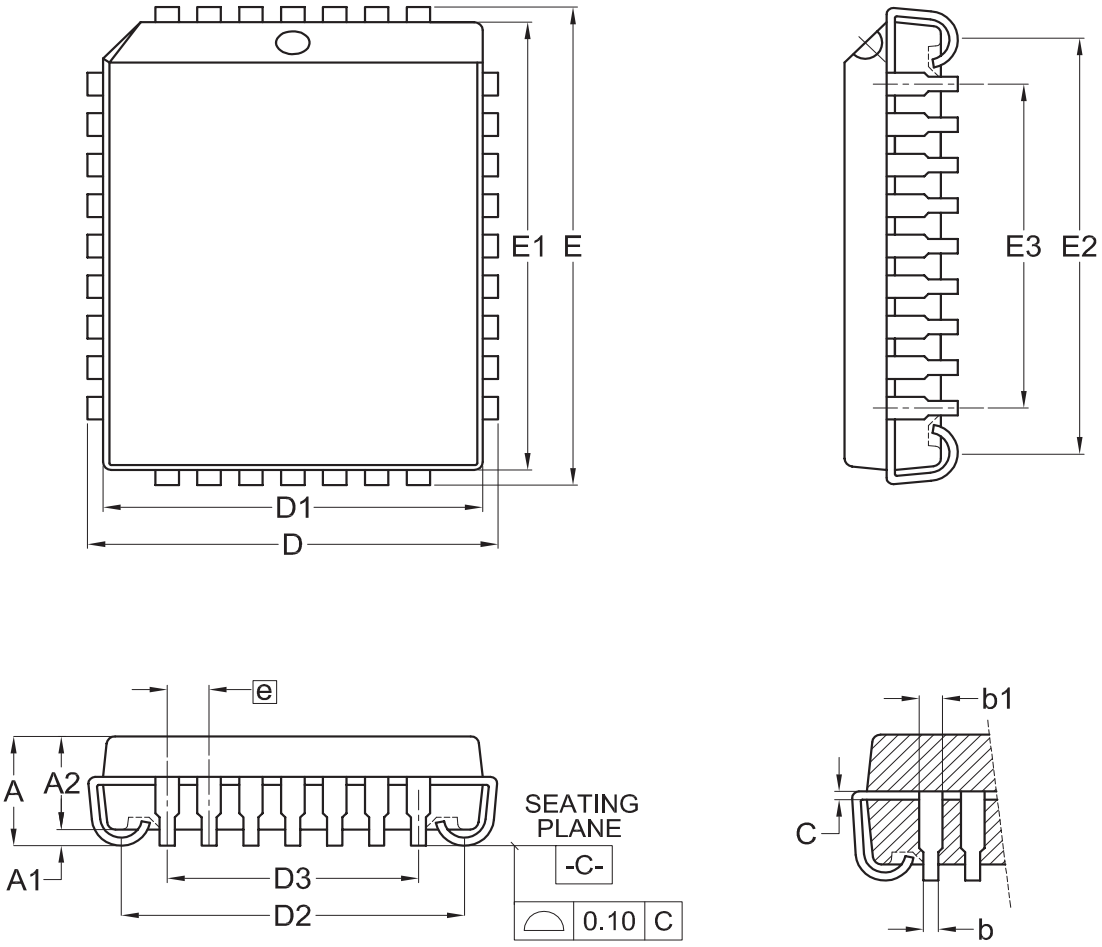
* Advanced Information

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for 32L PLCC

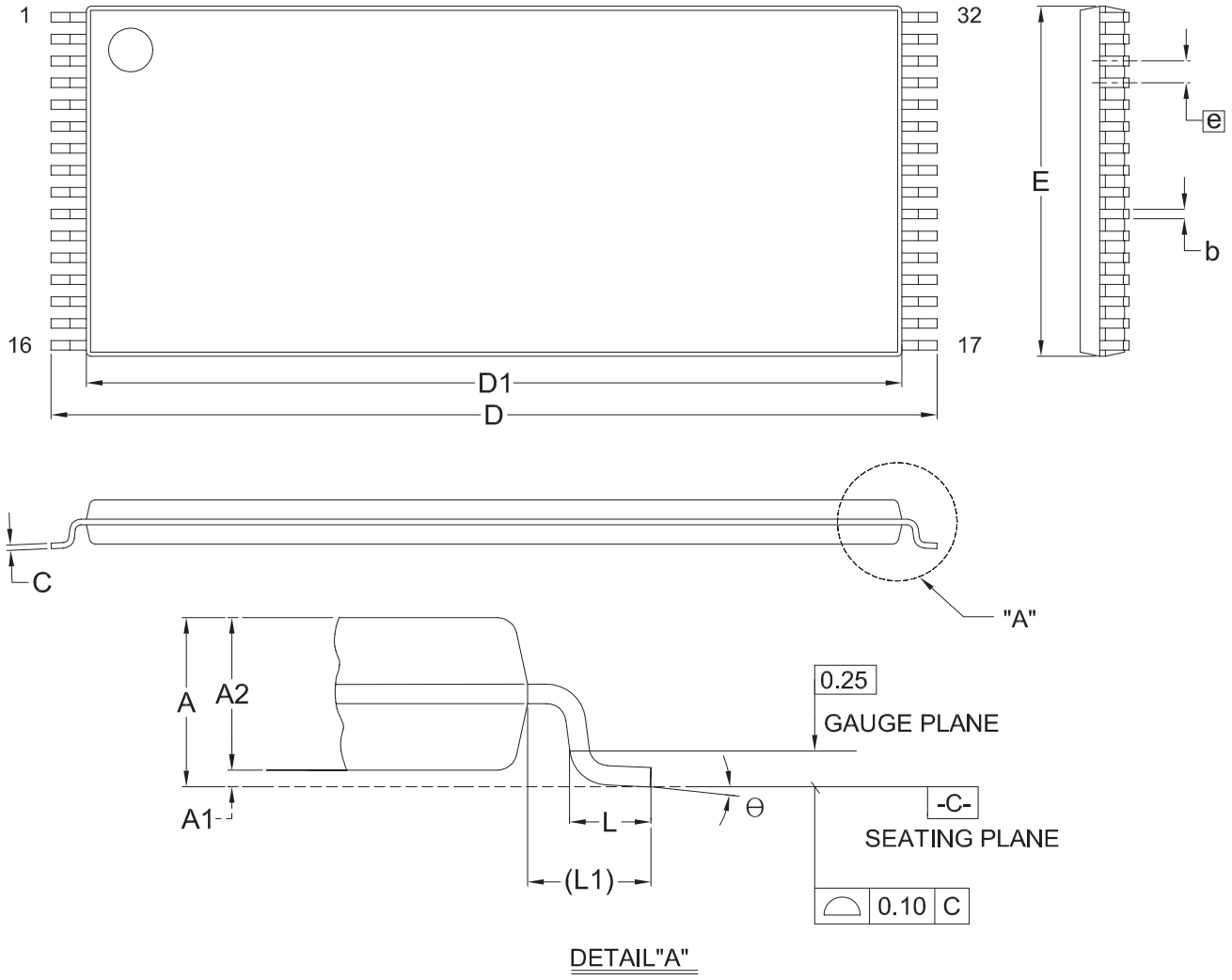


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	---	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	---	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	7	MS-016			12-10-'03

Title: Package Outline for TSOP(I) 32L (8X20mm)

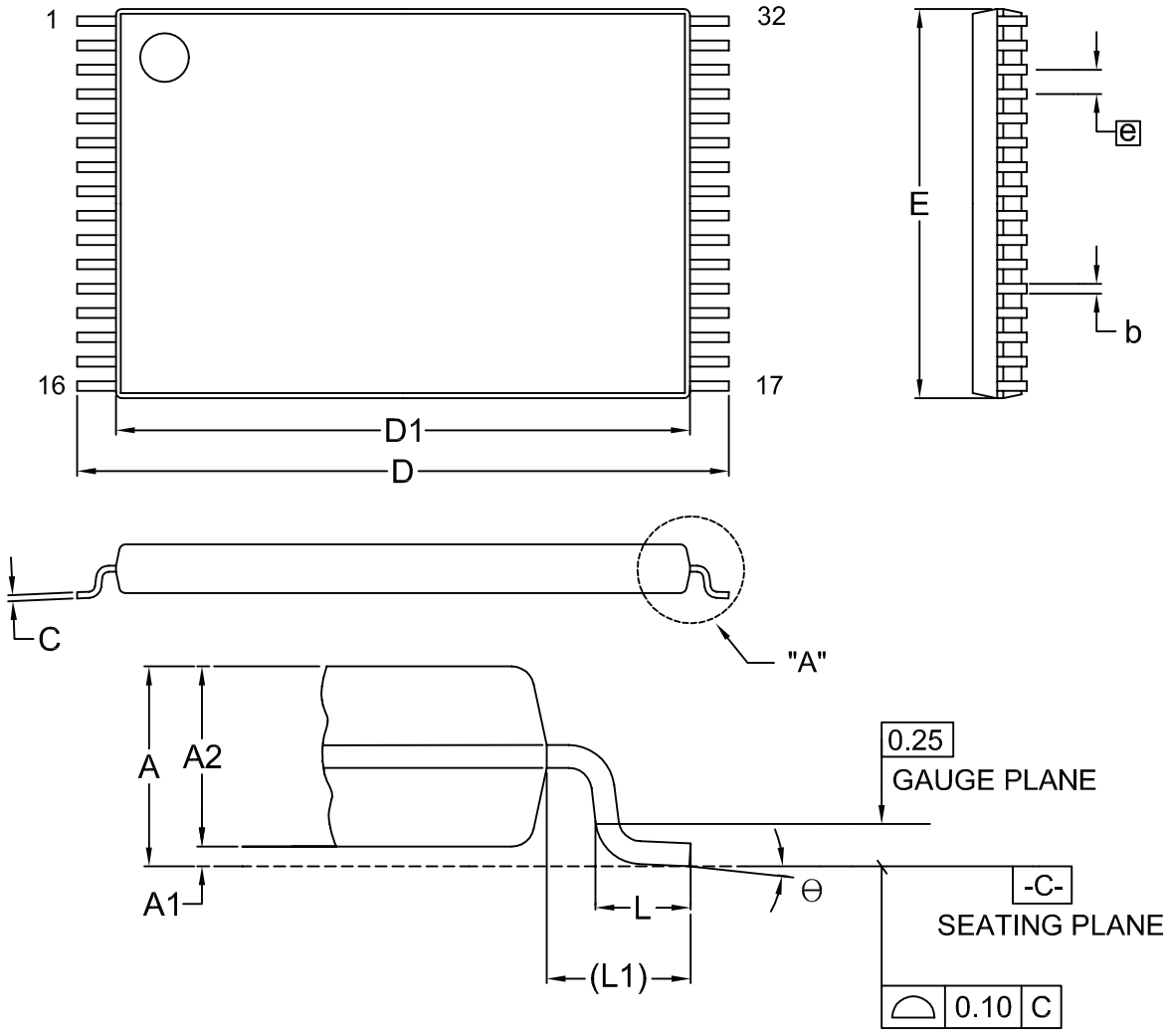


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	9	MO-142			11-26-'03

Title: Package Outline for TSOP(I) 32L (8X14mm)



DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	13.80	12.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	14.00	12.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	14.20	12.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.543	0.484	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.551	0.488	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.559	0.492	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1603	5	MO-142			11-26-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary"	P1	JUN/30/2005
	2. Added "Recommended Operating Conditions"	P43	
1.1	1. Modified "Low power consumption--active current" from 20mA(Max.) to 30mA(Max.)	P1	AUG/30/2005
	2. Added description about Pb-free devices are RoHS Compliant	P1	
1.2	1. Modified Erase Resume from delay 10ms to delay 400us	P12,32	JAN/17/2006
1.3	1. Modified table 15. CFI mode	P45,46	APR/24/2006
	2. Added VLKO description	P15,18	
1.4	1. Modified CFI mode	P45,46	JUL/11/2006
1.5	1. Datasheet format changed	All	AUG/15/2006
1.6	1. Data modification	All	AUG/16/2006
1.7	1. Data modification	All	AUG/17/2006
1.8	1. Added statement	P44	NOV/06/2006
1.9	1. Revised statement	P14	DEC/28/2007
2.0	1. Added note 1 into table 3. Command Definitions	P9	JAN/17/2008
2.1	1. Modified Figure 9. CE# Controlled Write Timing Waveform	P29	FEB/21/2008
2.2	1. Revised Twc, Tcwc, Tds AC timing spec	P20	JUL/31/2008
2.3	1. Added 32-TSOP (8mm x 14mm) package information	P1,2,39 P40,43	MAR/25/2009

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