MOTOROLA

4-Bit Decade Counter With Mode Control

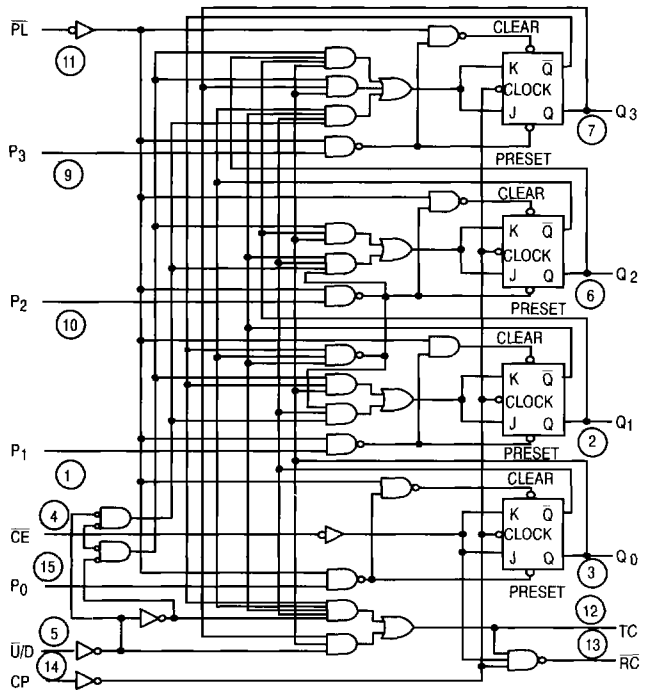
ELECTRICALLY TESTED PER:
MIL-M-38510/31513

The 54LS190 is an asynchronous UP/DOWN BCD Decade (8421) Counter and the 54LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load ($\overline{PL}$) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable ($\overline{CE}$) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U}$/D) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock ($\overline{RC}$) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

- Low Power . . . 90 mW Typical Dissipation
- High-Speed . . . 25 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Individual Preset Inputs
- Count Enable and Up/Down Control Inputs
- Cascadable
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC DIAGRAM



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Military 54LS190

AVAILABLE AS:

1) JAN: JM38510/31513BXA
2) SMD: 7603501
3) 883: 54LS190/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
P_1	1	1	2	V_{CC}
Q_1	2	2	3	V_{CC}
Q_0	3	3	4	V_{CC}
$\overline{CE}$	4	4	5	V_{CC}
$\overline{U}$/D	5	5	7	V_{CC}
Q_2	6	6	8	V_{CC}
Q_3	7	7	9	V_{CC}
GND	8	8	10	GND
P_3	9	9	12	V_{CC}
P_2	10	10	13	V_{CC}
$\overline{PL}$	11	11	14	GND
TC	12	12	15	OPEN
$\overline{RC}$	13	13	17	V_{CC}
CP	14	14	18	GND
P_0	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

MODE SELECT TABLE

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Clock Transition
⌐¬ = LOW Pulse

FUNCTIONAL DESCRIPTION

The 'LS190 is a synchronous Up/Down BCD Decade Counter and the 'LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the 'LS190 decade counter and the 'LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similarly, the U/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the 'LS190, 15 for the 'LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the RC output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input signal for a given stage is formed by combining the TC signals from all the proceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

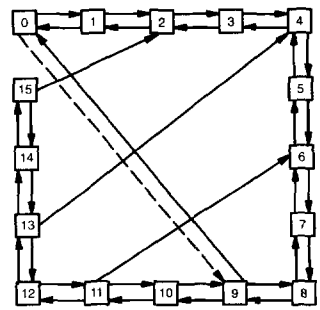
Pin Names		Loading (Note a)	
		HIGH	LOW
$\overline{CE}$	Count Enable (Active LOW) Input	1.5 U.L.	0.7 U.L.
CP	Clock Pulse (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{U}$/D	Up/Down Count Control Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Parallel Load Control (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{RC}$	Ripple Clock Output (Note b)	10 U.L.	5(2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. One TTL Unit Load (U.L.) = 40 μA HIGH/ 1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

RC TRUTH TABLE			
Inputs			Output
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⊓	⊓
H	X	X	H
X	L	X	H

*TC is generated internally

STATE DIAGRAM



LS190
UP: $TC = Q_0 \cdot Q_3 \cdot (\overline{U/D})$
DOWN: $TC = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (\overline{U/D})$

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Figure a. n-Stage Counter Using Ripple Clock

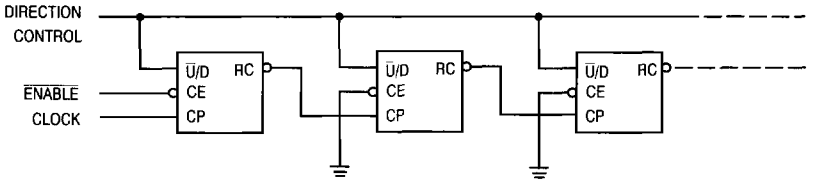


Figure b. Synchronous n-Stage Counter Using Carry/Borrow

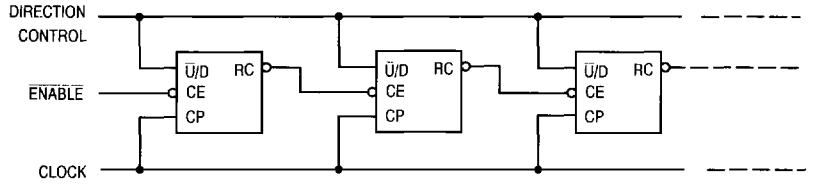
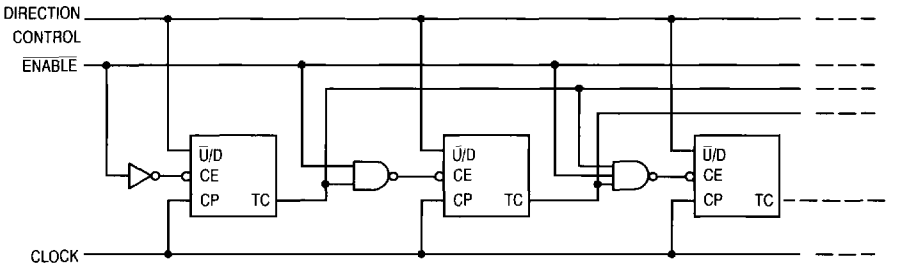


Figure c. Synchronous n-Stage Counter with Parallel Gated Carry/Borrow



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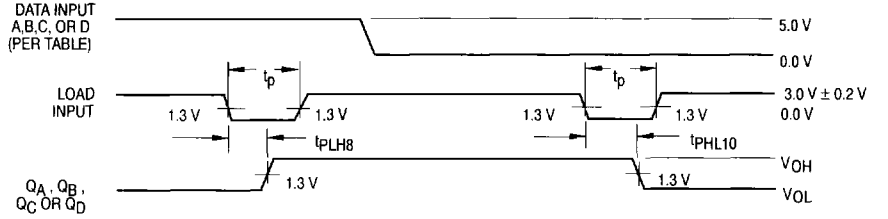
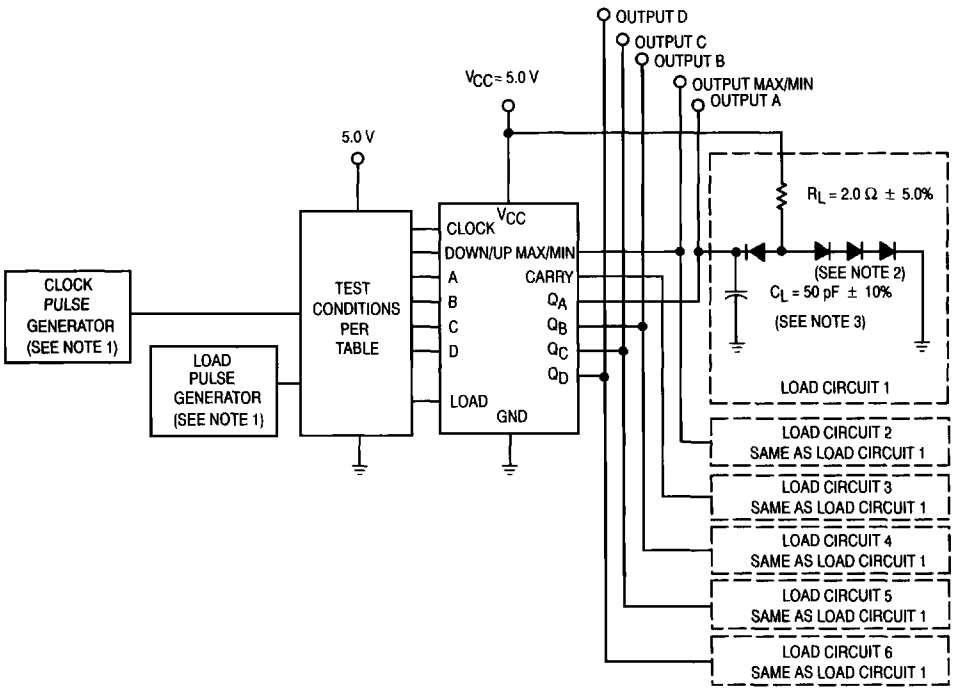
PARALLEL LOADED VOLTAGE WAVEFORMS



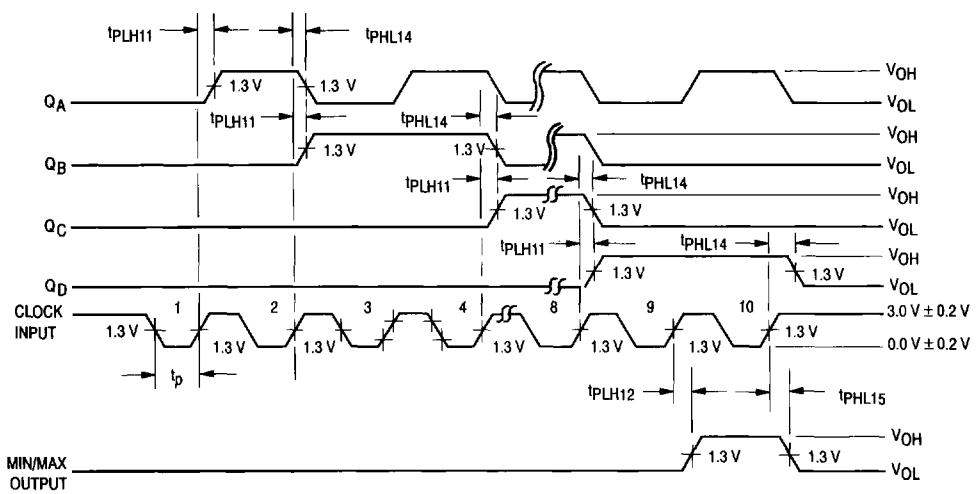
NOTES:

1. The pulse generator has the following characteristics: V_{gen} = 3.0 V, PRR ≤ 1.0 MHz, t_r ≤ 15 ns, t_f ≤ 6.0 ns, between 0.7 V and 2.7 V, t_p = 0.5 µs and Z_{OUT} ≈ 50 Ω.
2. All diodes are 1N3064 or equivalent.
3. C_L = 50 pF ± 10%, including scope probe, wiring, and stray capacitance without package in test fixture.
4. Voltage values are with respect to ground terminal.
5. R_L = 2.0 kΩ ± 5.0%.
6. f_{MAX}: $t_r = t_f \leq 6.0$ ns.
7. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

AC TEST CIRCUIT



SERIAL LOADED VOLTAGE WAVEFORMS (COUNT UP MODE)



REFERENCE NOTES ON PAGE 5-252

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IH} = 2.0 V, V_{IN} = 0.7 V, other inputs are open.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, V_{IN} = 2.0 V, other inputs are open.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
$I_{IH(\overline{CE})}$	Logical "1" Input Current		60		60		60	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
$I_{IHH(\overline{CE})}$	Logical "1" Input Current		300		300		300	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{PL}$ = 5.5 V or 2.7 V.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open, $\overline{PL}$ = 5.5 V.
$I_{IL(\overline{CE})}$	Logical "0" Input Current	− 0.36	− 1.08	− 0.36	− 1.08	− 0.36	− 1.08	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V ($\overline{CE}$), other input ($\overline{U}$/D) = 5.5 V.
I_{IL}	Logical "0" Input Current	− 120	− 360	− 120	− 360	− 120	− 360	µA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs are open, $\overline{PL}$ = GND or open.
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open, $\overline{PL}$ = GND, V_{OUT} = GND.
I_{CC}	Power Supply Current Off		35		35		35	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL10} t_{PHL10}	Propagation Delay /Data-Output PL to Q Outputs	3.0 —	55 50	3.0 —	77 72	3.0 —	77 72	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH8} t_{PLH8}	Propagation Delay /Data-Output PL to Q Outputs	3.0 —	38 33	3.0 —	53 48	3.0 —	53 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL14} t_{PHL14}	Propagation Delay /Data-Output Clock to Q Outputs	3.0 —	41 36	3.0 —	57 52	3.0 —	57 52	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH11} t_{PLH11}	Propagation Delay /Data-Output Clock to Q Outputs	3.0 —	29 24	3.0 —	41 36	3.0 —	41 36	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL15} t_{PHL15}	Propagation Delay /Data-Output Clock to TC	3.0 —	57 52	3.0 —	80 75	3.0 —	80 75	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL12} t_{PHL12}	Propagation Delay /Data-Output Clock to TC	3.0 —	47 42	3.0 —	66 61	3.0 —	66 61	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX} f_{MAX}	Maximum Clock Frequency	18 20		18 —		18 —		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

NOTE:

1. The limit specified for C_L = 15 pF are guaranteed but not tested.

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