54F/74F432

Multi-Mode Buffered Latch With 3-State Outputs

Description

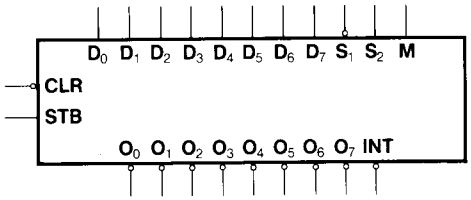
The 'F432 is an 8-bit latch with 3-state output buffers and control and device selection logic. Also included is a status flip-flop for providing device-busy or request-interrupt commands. Separate Mode and Select inputs allow data to be stored with the outputs enabled or disabled. The device can also operate in a fully transparent mode.

The 'F432 is the functional equivalent of the Intel 8212, but with inverting outputs.

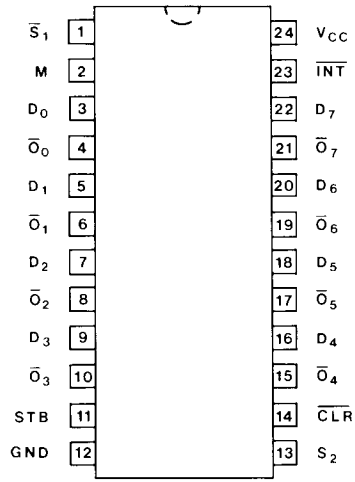
- 3-State Inverting Outputs
- Status Flip-Flop for Interrupt Commands
- Asynchronous or Latched Receiver Modes
- Data to Output Propagation Delay Typically 8.5 ns
- Supply Current 43 mA Typ
- 24-Pin Slim Package

Ordering Code: See Section 5

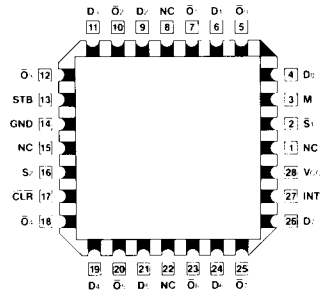
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
$\overline{O}_0$-$\overline{O}_7$	Latch Outputs	75/15 (12.5)
$\overline{S}_1$,S_2	Select Inputs	0.5/0.375
M	Mode Control Input	0.5/0.375
STB	Strobe	0.5/0.375
$\overline{INT}$	Interrupt	25/12.5
$\overline{CLR}$	Clear	0.5/0.375

Functional Description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The 3-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable, G, input is HIGH and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_1$ and S_2), and the strobe (STB) inputs and during transparency each data output ($\overline{O}_n$) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See Data Latches Function Table.

An input mode or an output mode is selectable from this single input line. In the input mode, M = L, the eight data latch inputs are enabled when the strobe is HIGH regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken LOW the latches will store the most recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_1$ and S_2) inputs. See Data Latches Function Table.

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Data Latches Function Table

Function	$\overline{CLR}$	M	$\overline{S}_1$	S_2	STB	Data In	Data Out
Clear	L	H	H	X	X	X	H
	L	L	L	H	L	X	H
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	$\overline{Q}_0$
	H	L	L	H	L	X	$\overline{Q}_0$
Data Bus	H	H	L	H	X	L	H
	H	H	L	H	X	H	L
Data Bus	H	L	L	H	H	L	H
	H	L	L	H	H	H	L

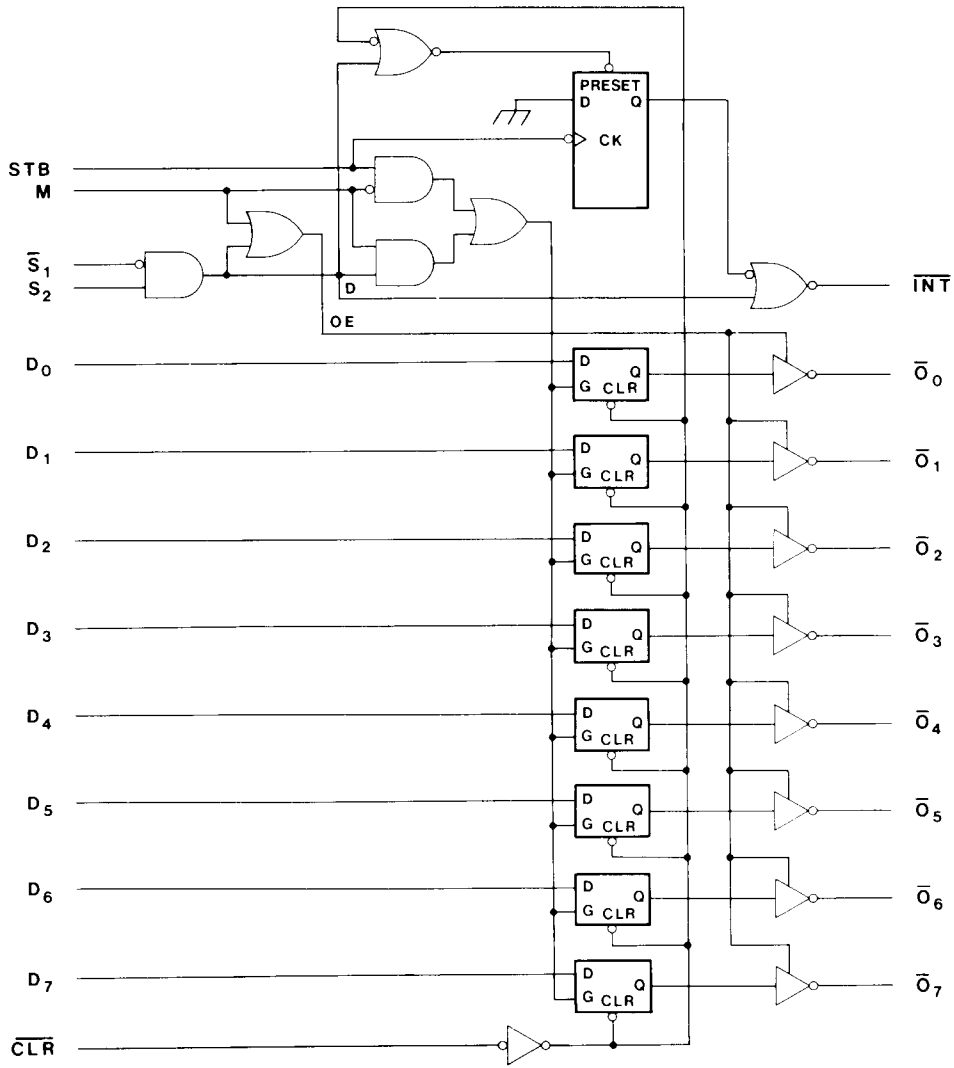
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Status Flip-Flop Function Table

$\overline{CLR}$	$\overline{S}_1$	S_2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↑	L
H	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		43	65	mA	V_{CC} = Max
I_{CCL}			29	43		
I_{CCZ}			29	43		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.5	8.5	10.5			3.0	12.0	ns	3-1
t_{PHL}	D_n to O_n	2.5	5.5	7.0			3.0	12.0		3-3
t_{PLH}	Propagation Delay	8.5	16.0	21.0			7.5	23.0	ns	3-1
t_{PHL}	$\overline{S}_1$, S_2 or STB to $\overline{O}_n$	6.5	12.5	16.0			5.5	18.0		3-7
t_{PHL}	Propagation Delay $\overline{CLR}$ to $\overline{O}_n$	7.0	15.0	18.5			6.0	20.5	ns	3-1, 3-9
t_{PHL}	Propagation Delay STB to INT	6.0	11.5	14.5			5.0	16.0	ns	3-1, 3-10
t_{PLH}	Propagation Delay $\overline{S}_1$ or S_2 to $\overline{INT}$	4.0	7.5	9.5			3.5	10.5	ns	3-1, 3-10
t_{PLH}	Propagation Delay	9.0	15.0	19.0			9.0	20.0	ns	3-1
t_{PHL}	M to $\overline{O}_n$	6.5	11.0	14.0			6.5	15.0		3-3
t_{PZH}	Enable Time	4.5	13.0	18.0			4.0	20.0	ns	3-1, 3-12, 3-13
t_{PZL}	$\overline{S}_1$, S_2 to $\overline{O}_n$	5.0	11.0	15.0			4.0	17.0		
t_{PHZ}	Disable Time	4.0	8.0	11.0			3.5	12.5		
t_{PLZ}	$\overline{S}_1$, S_2 to $\overline{O}_n$	5.0	11.0	15.5			4.0	17.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{S}_1$, S_2, STB	0 0		0 0	ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{S}_1$, S_2, STB	11.0 8.5		12.5 9.5		
$t_w(H)$ $t_w(L)$	STB, $\overline{S}_1$, S_2 Pulse Width HIGH or LOW	8.0 8.0		9.0 9.0	ns	3-9
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	8.0		9.0	ns	3-9