LMV7291 Single 1.8V Low Power Comparator with Rail-to-Rail Input

Check for Samples: LMV7291

FEATURES

- **(V_S = 1.8V, T_A = 25°C, Typical Values unless Specified)**
- **Single Supply**
- **Ultra Low Supply Current 9µA per Channel**
- **Low Input Bias Current 10nA**
- **Low Input Offset Current 200pA**
- **Low ensured V_{OS} 4mV**
- **Propagation Delay 880ns (20mV Overdrive)**
- **Input Common Mode Voltage Range 0.1V beyond Rails**

APPLICATIONS

- **Mobile Communications**
- **Laptops and PDA's**
- **Battery Powered Electronics**
- **General Purpose Low Voltage Applications**

DESCRIPTION

The LMV7291 is a rail-to-rail input low power comparator, characterized at supply voltage 1.8V, 2.7V and 5.0V. It consumes only 9uA supply current per channel while achieving a 800ns propagation delay.

The LMV7291 is available in SC70 package. With this tiny package, the PC board area can be significantly reduced. It is ideal for low voltage, low power and space critical designs.

The LMV7291 features a push-pull output stage which allows operation with minimum power consumption when driving a load.

The LMV7291 is built with Texas Instruments' advance submicron silicon-gate BiCMOS process. It has bipolar inputs for improved noise performance and CMOS outputs for rail-to-rail output swing.

Typical Circuit

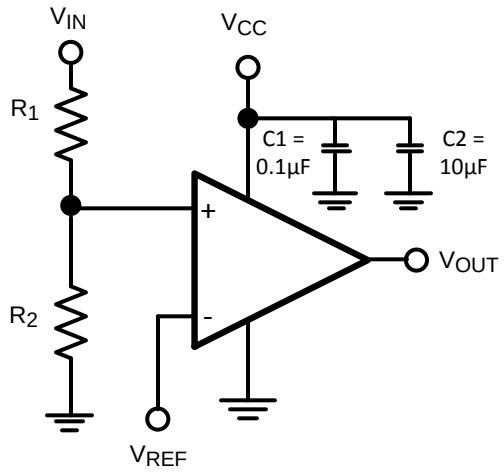


Figure 1. Threshold Detector

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance	
	2KV (3)
	200V (4)
V_{IN} Differential	±Supply Voltage
Supply Voltage (V^+ - V^-)	5.5V
Voltage at Input/Output pins	V^+ +0.1V, V^- −0.1V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (5)	+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω in series with 200pF.
(5) Typical values represent the most likely parametric norm.

Operating Ratings (1)

Operating Temperature Range (2)	−40°C to +85°C
Package Thermal Resistance (2)	
SC70	265°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

1.8V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 1.8V, V^- = 0V. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 0.9V (4)		10		uV/C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current	LMV7291		9	12 **14**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0.9V	3.5	6		mA
		Sinking, V_O = 0.9V	4	6		
V_{OH}	Output Voltage High	I_O = 0.5mA	1.7	1.74		V
		I_O = 1.5mA	1.58	1.63		
V_{OL}	Output Voltage Low	I_O = −0.5mA		52	70	mV
		I_O = −1.5mA		166	220	
V_{CM}	Input Common Mode Voltage Range	CMRR > 45 dB			1.9	V
			−0.1			V
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 1.8V	47	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 1.8V		2		pA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		880		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		570		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1100		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		800		ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.

2.7V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 1.35V (4)		10		µV/C
I_B	Input Bias Current			10		nA
I_{OS}	Input offset Current			200		pA
I_S	Supply Current	LMV7291		9	13 **15**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 1.35V	12	15		mA
		Sinking, V_O = 1.35V	12	15		
V_{OH}	Output Voltage High	I_O = 0.5mA	2.63	2.66		V
		I_O = 2.0mA	2.48	2.55		
V_{OL}	Output Voltage Low	I_O = −0.5mA		50	70	mV
		I_O = −2mA		155	220	
V_{CM}	Input Common Voltage Range	CMRR > 45dB			2.8	V
			−0.1			V
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 2.7V	47	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 2.7V		2		pA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Condition	Min(2)	Typ(3)	Max(2)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		1200		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		810		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1300		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		860		ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.

5V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 2.5V (4)		10		µV/C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current	LMV7291		10	14 **16**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 2.5V	28	34		mA
		Sinking, V_O = 2.5V	28	34		
V_{OH}	Output Voltage High	I_O = 0.5mA	4.93	4.96		V
		I_O = 4.0mA	4.70	4.77		
V_{OL}	Output Voltage Low	I_O = −0.5mA		27	70	mV
		I_O = −4.0mA		225	300	
V_{CM}	Input Common Voltage Range	CMRR > 45dB			5.1	V
			−0.1			
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 5.0V	47	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 5V		2		pA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

5.0V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes. (1)

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		2100		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		1380		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1800		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		1100		ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm.

Connection Diagram

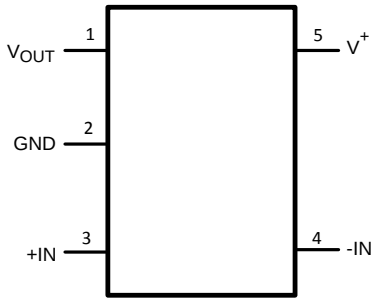


Figure 2. 5-Pin SC70 – Top View
See Package Number DCK

Typical Performance Characteristics

(T_A = 25°C, Unless otherwise specified).

V_{OS} vs. V_{CM}

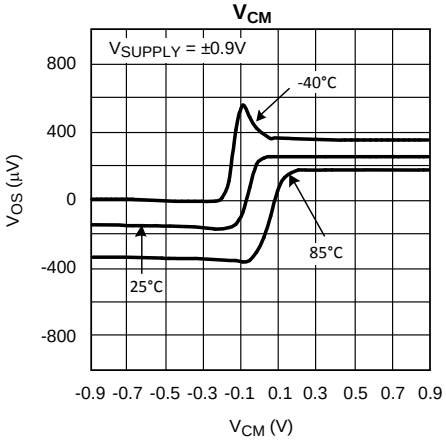


Figure 3.

V_{OS} vs. V_{CM}

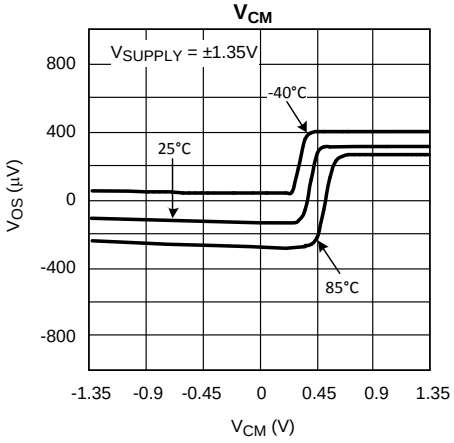


Figure 4.

V_{OS} vs. V_{CM}

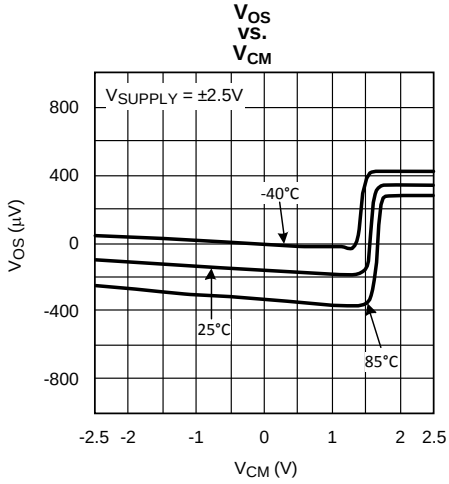


Figure 5.

Short Circuit vs. Supply Voltage

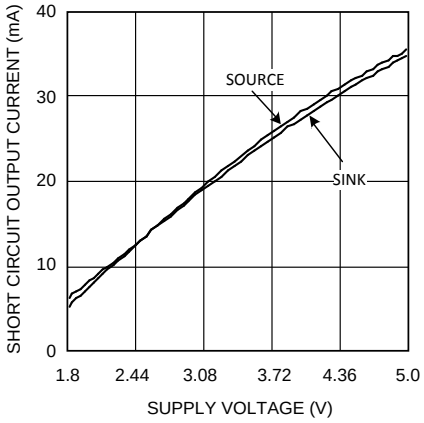


Figure 6.

Supply Current vs. Supply Voltage

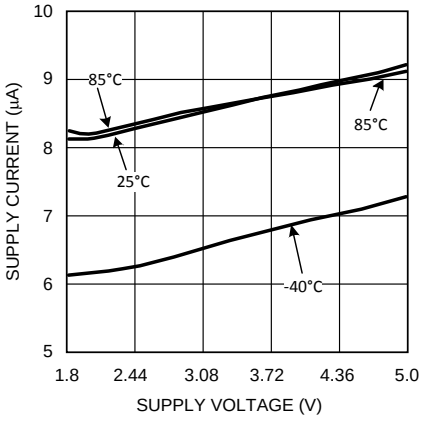


Figure 7.

Supply Current vs. Supply Voltage

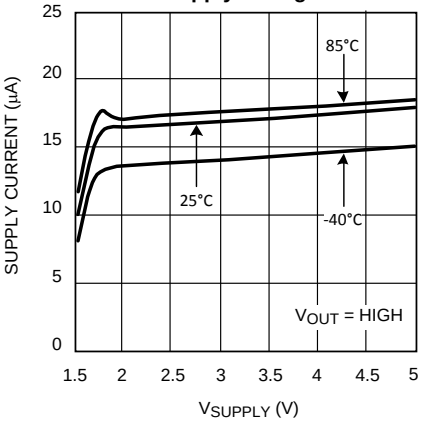


Figure 8.

Typical Performance Characteristics (continued)

(T_A = 25°C, Unless otherwise specified).

Supply Current vs. Supply Voltage

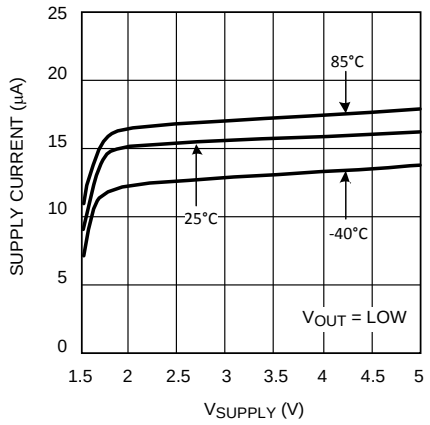


Figure 9.

Output Positive Swing vs. V_{SUPPLY}

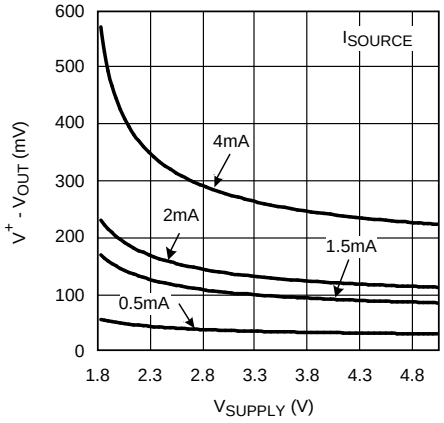


Figure 10.

Output Negative Swing vs. V_{SUPPLY}

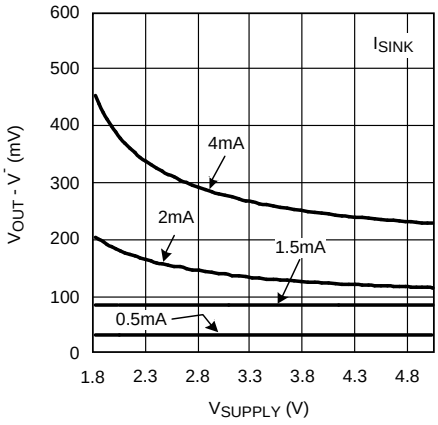


Figure 11.

Output Positive Swing vs. I_{SOURCE}

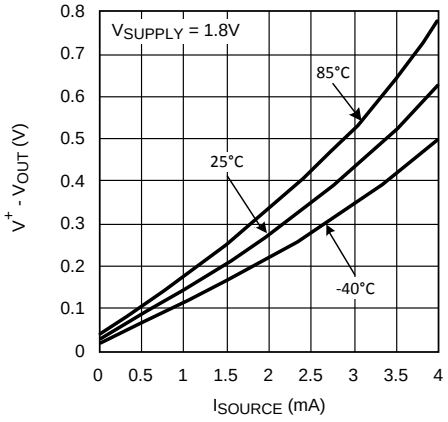


Figure 12.

Output Negative Swing vs. I_{SINK}

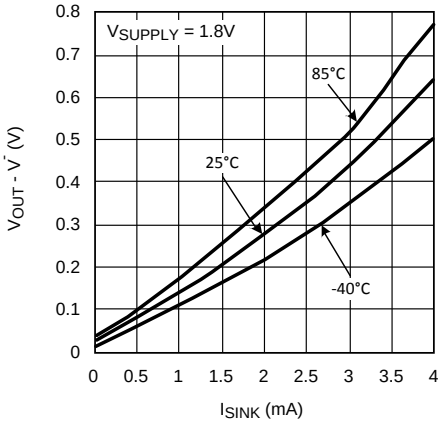


Figure 13.

Output Positive Swing vs. I_{SOURCE}

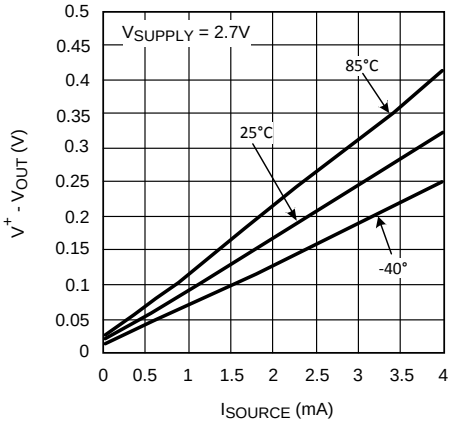


Figure 14.

Typical Performance Characteristics (continued)

(T_A = 25°C, Unless otherwise specified).

Output Negative Swing vs. I_{SINK}

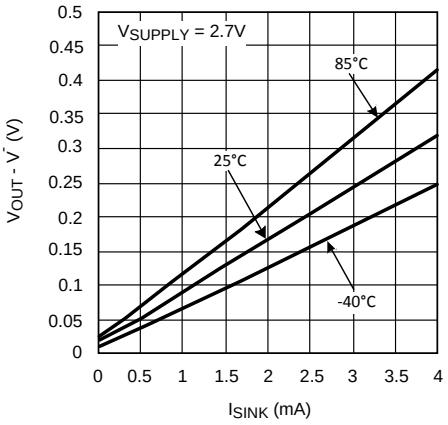


Figure 15.

Output Negative Swing vs. I_{SINK}

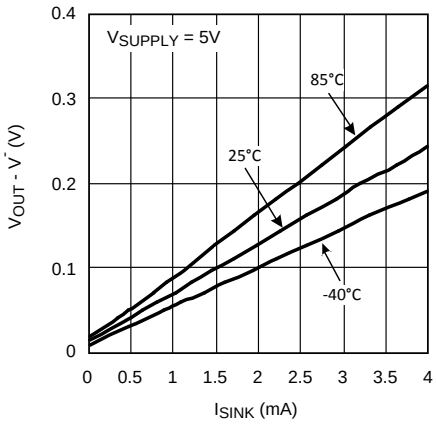


Figure 16.

Output Positive Swing vs. I_{SOURCE}

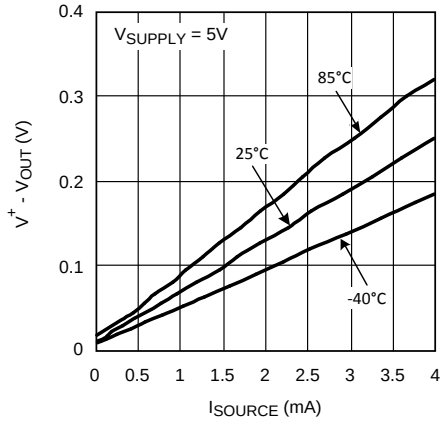


Figure 17.

Propagation Delay (t_{PLH})

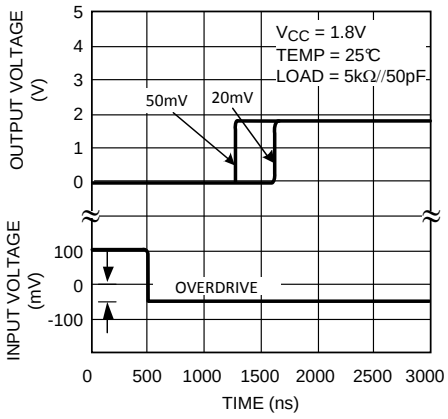


Figure 18.

Propagation Delay (t_{PHL})

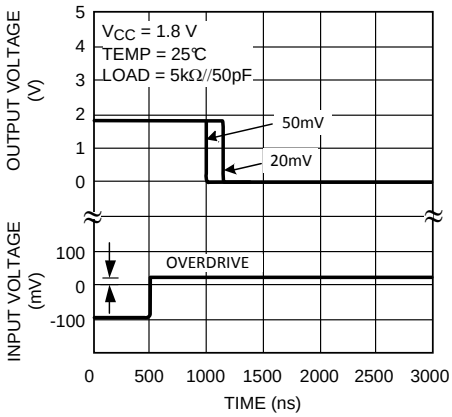


Figure 19.

Propagation Delay (t_{PLH})

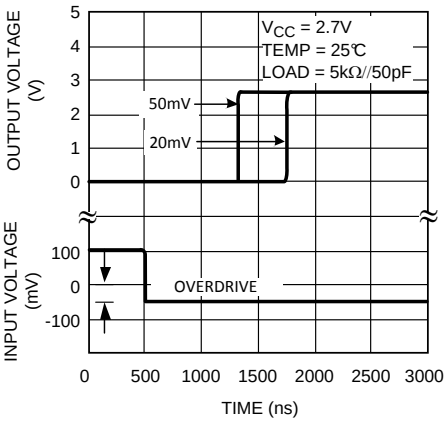


Figure 20.

Typical Performance Characteristics (continued)

(T_A = 25°C, Unless otherwise specified).

Propagation Delay (t_{PHL})

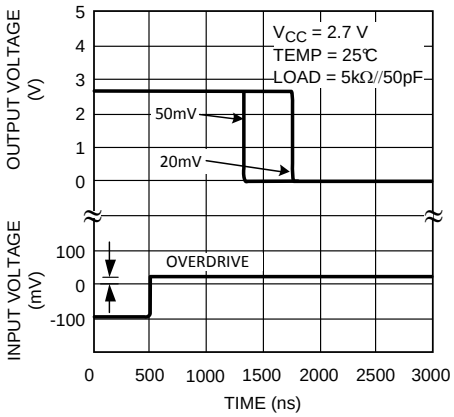


Figure 21.

Propagation Delay (t_{PLH})

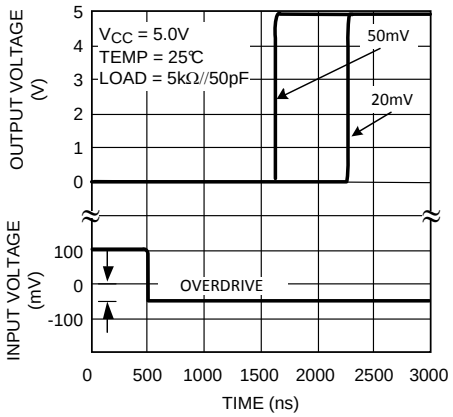


Figure 22.

Propagation Delay (t_{PHL})

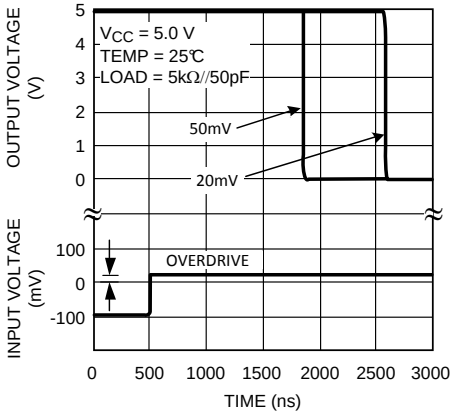


Figure 23.

t_{PHL} vs. Overdrive

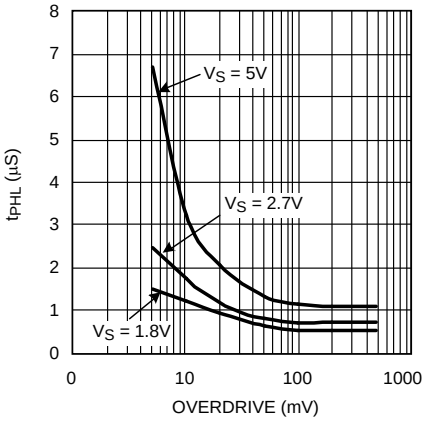


Figure 24.

t_{PLH} vs. Overdrive

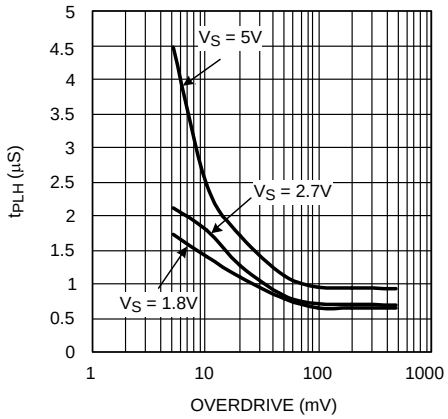


Figure 25.

APPLICATION NOTES

BASIC COMPARATOR

A comparator is often used to convert an analog signal to a digital signal. As shown in Figure 26, the comparator compares an input voltage (V_{IN}) to a reference voltage (V_{REF}). If V_{IN} is less than V_{REF}, the output (V_O) is low. However, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is high.

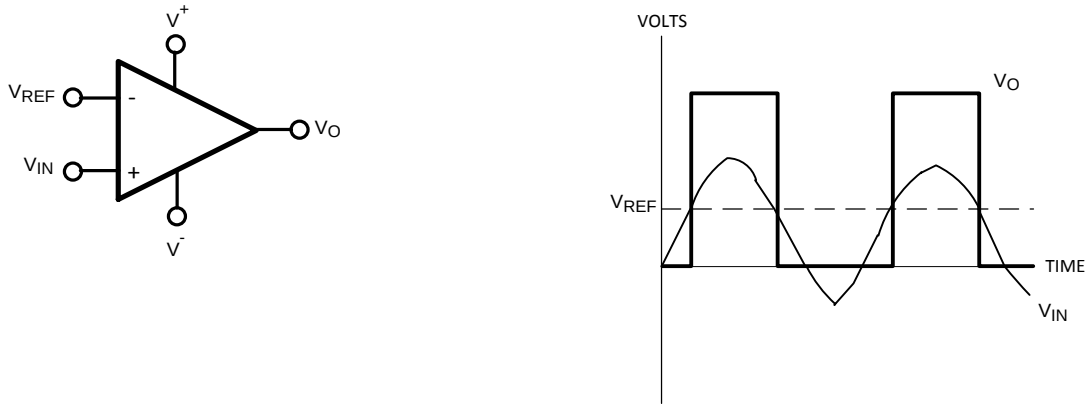


Figure 26. LMV7291 Basic Comparator

RAIL-TO-RAIL INPUT STAGE

The LMV7291 has an input common mode voltage range (V_{CM}) of −0.1V below the V^- to 0.1V above V^+. This is achieved by using paralleled PNP and NPN differential input pairs. When the V_{CM} is near V^+, the NPN pair is on and the PNP pair is off. When the V_{CM} is near V^-, the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around 950mV from V^+. Since each input stage has its own offset voltage (V_{OS}), the V_{OS} of the comparator becomes a function of the V_{CM}. See Figure 3, Figure 4, and Figure 5 in Typical Performance Characteristics. In application design, it is recommended to keep the V_{CM} away from the crossover point to avoid problems. The wide input voltage range makes LMV7291 ideal in power supply monitoring circuits, where the comparators are used to sense signals close to gnd and power supplies.

OUTPUT STAGE

The LMV7291 has a push-pull output stage. This output stage keeps the total system power consumption to the absolute minimum. The only current consumed is the low supply current and the current going directly into the load. When output switches, both PMOS and NMOS at the output stage are on at the same time for a very short time. This allows current to flow directly between V^+ and V^- through output transistors. The result is a short spike of current (shoot-through current) drawn from the supply and glitches in the supply voltages. The glitches can spread to other parts of the board as noise. To prevent the glitches in supply lines, power supply bypass capacitors must be installed. See CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS for details.

HYSTERESIS

It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier of its own noise.

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage V_{CC} of the comparator (Figure 27). When V_{IN} at the inverting input is less than V_A, the voltage at the non-inverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1||R_3$ in series with R_2. The lower input trip voltage V_{A1} is defined as

$$V_{A1} = \frac{V_{CC}\, R_2}{(R_1||R_3) + R_2} \quad (1)$$

When V_{IN} is greater than V_A ($V_{IN} > V_A$), the output voltage is low and very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{A2} is defined as

$$V_{A2} = \frac{V_{CC}\,(R_2||R_3)}{R_1 + (R_2||R_3)} \quad (2)$$

The total hysteresis provided by the network is defined as

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

A good typical value of ΔV_A would be in the range of 5 to 50 mV. This is easily obtained by choosing R_3 as 1000 to 100 times ($R_1||R_2$) for 5V operation, or as 300 to 30 times ($R_1||R_2$) for 1.8V operation.

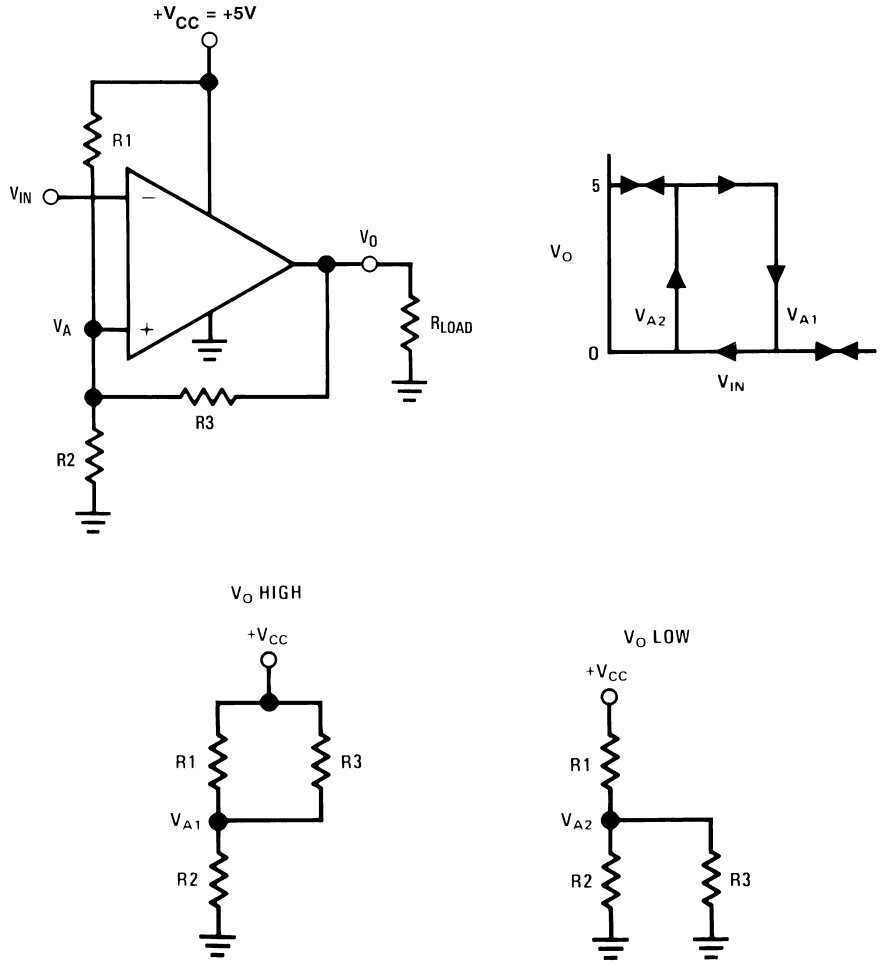


Figure 27. Inverting Comparator with Hysteresis

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input (Figure 28). When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}, where V_{IN1} is calculated by

$$V_{in1} = \frac{V_{ref}\,(R_1 + R_2)}{R_2} \quad (4)$$

When V_{IN} is high, the output is also high. To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN} can be calculated by:

$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC} R_1}{R_2} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{CC} R_1 / R_2 \quad (6)$$

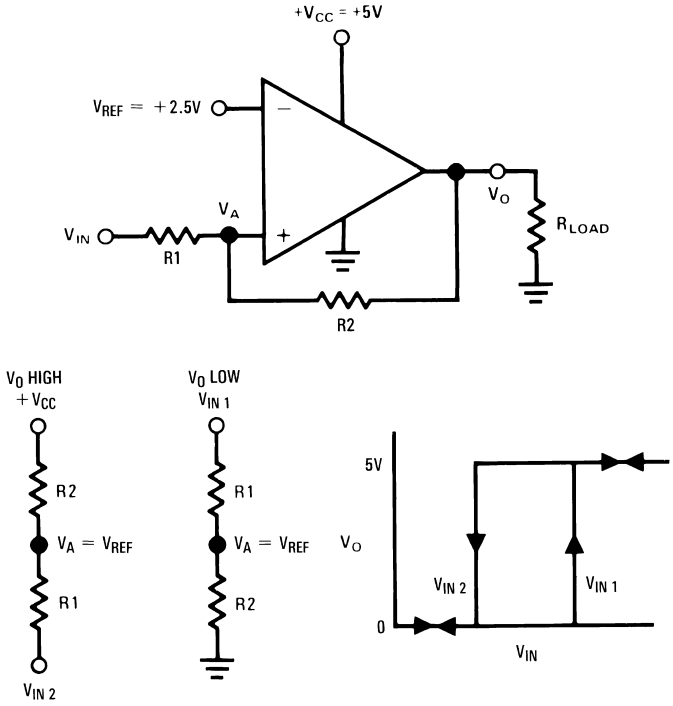


Figure 28. Non-Inverting Comparator with Hysteresis

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and transient response. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to mis-operate. To avoid problems, a small bypass capacitor, such as 0.1uF ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8µF or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In dual supply application, a 0.1µF capacitor is recommended to be placed across V^+ and V^- pins.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).
3. It is a good practice to use an unbroken ground plane on a printed circuit board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.
4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard.

5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.
6. All pins of any unused comparators should be tied to the negative supply.

Typical Applications

POSITIVE PEAK DETECTOR

A positive peak detect circuit is basically a comparator operated in a unity gain follower configuration, with a capacitor as a load to maintain the highest voltage. A diode is added at the output to prevent the capacitor from discharging through the output, and a 1MΩ resistor added in parallel to the capacitor to provide a high impedance discharge path. When the input V_{IN} increases, the inverting input of the comparator follows it, thus charging the capacitor. When it decreases, the cap discharges through the 1MΩ resistor. The decay time can be modified by changing the resistor. The output should be accessed through a follower circuit to prevent loading.

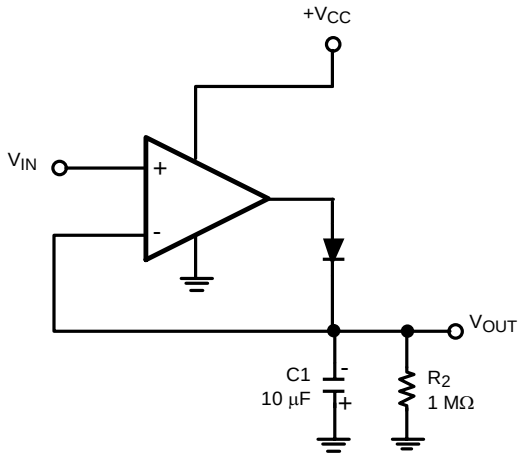


Figure 29. Positive Peak Detector

NEGATIVE PEAK DETECTOR

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. Since there is no pull-up resistor, the only discharge path will be the 1MΩ resistor and any load impedance used. Decay time is changed by varying the 1MΩ resistor.

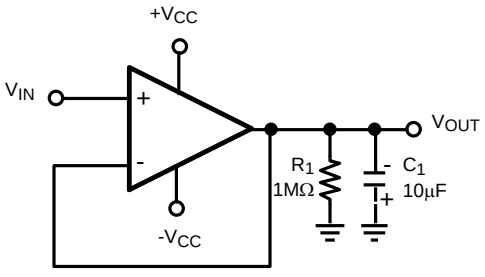


Figure 30. Negative Peak Detector

SQUARE WAVE GENERATOR

A typical application for a comparator is as a square wave oscillator. The circuit below generates a square wave whose period is set by the RC time constant of the capacitor $C_1$and resistor R_4. The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.

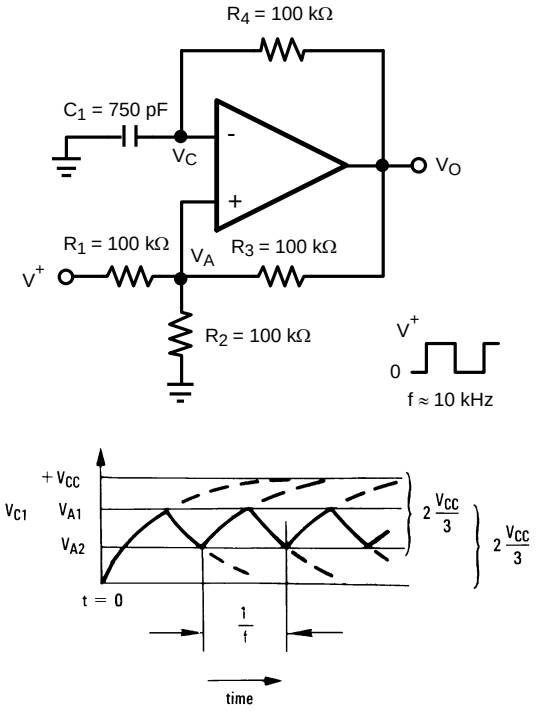


Figure 31. Squarewave Oscillator

To analyze the circuit, consider it when the output is high. That implies that the inverted input (V_C) is lower than the non-inverting input (V_A). This causes the C_1 to get charged through R_4, and the voltage V_C increases till it is equal to the non-inverting input. The value of V_A at this point is

$$V_{A1} = \frac{V_{CC}.R_2}{R_2 + R_1||R_3} \tag{7}$$

If $R_1 = R_2 = R_3$ then $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{CC}\,(R_2||R_3)}{R_1 + (R_2||R_3)} \tag{8}$$

If $R_1 = R_2 = R_3$ then $V_{A2} = V_{CC}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1.\ln 2$. Hence the formula for the frequency is:

$F = 1/(2.R_4.C_1.\ln 2)$

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7291MG	LIFEBUY	SC70	DCK	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	C36	
LMV7291MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C36	Samples
LMV7291MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C36	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

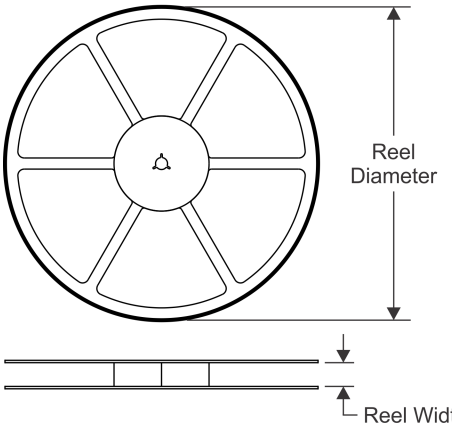
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

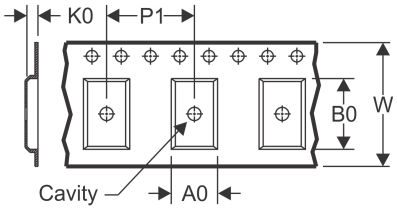
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

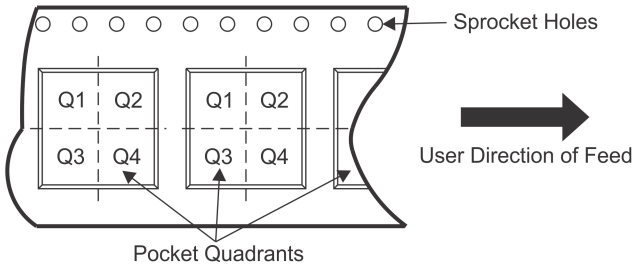


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

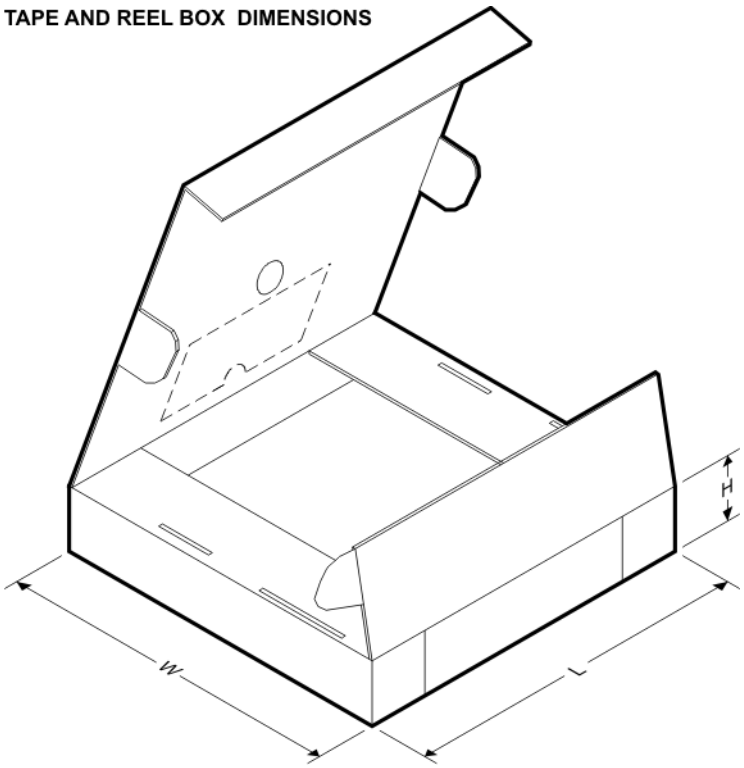
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7291MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7291MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7291MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

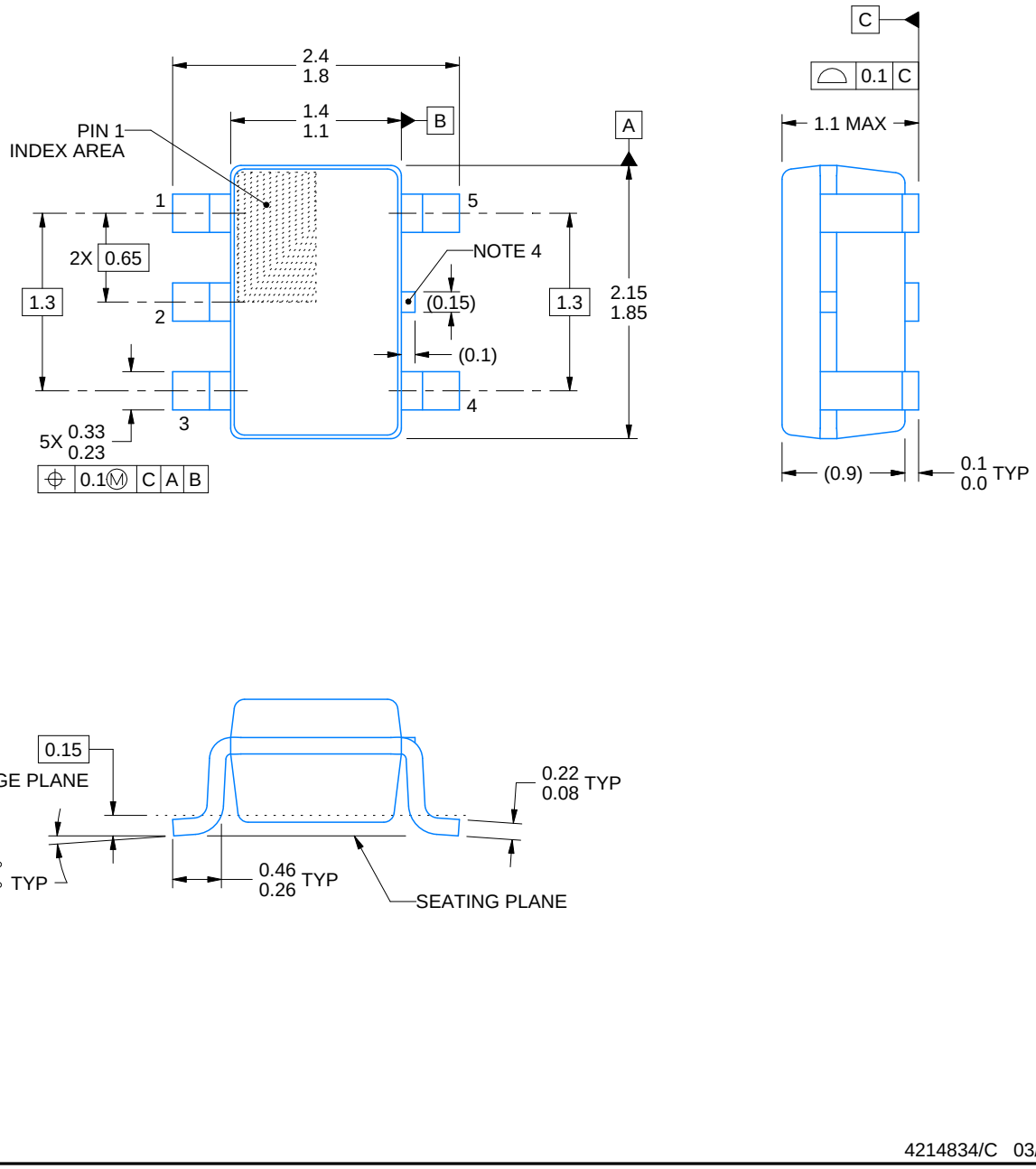
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7291MG	SC70	DCK	5	1000	208.0	191.0	35.0
LMV7291MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV7291MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

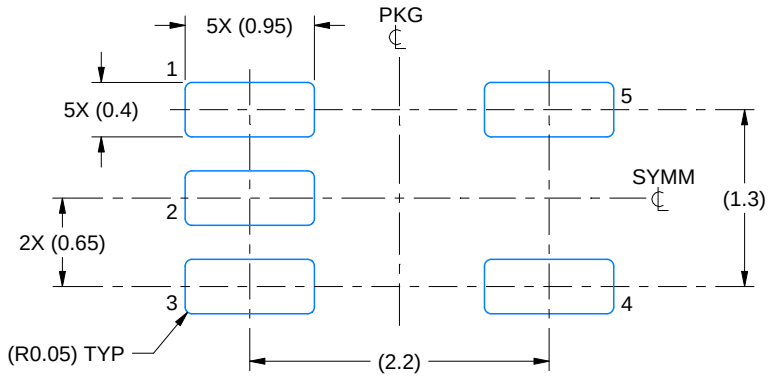
SMALL OUTLINE TRANSISTOR



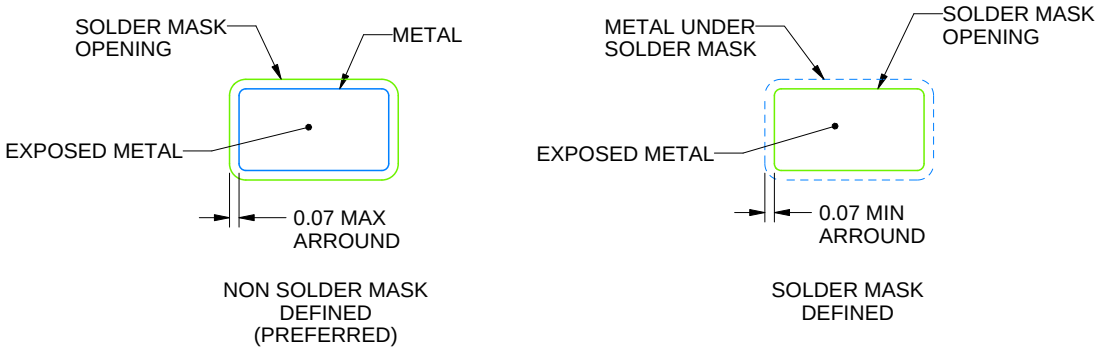
4214834/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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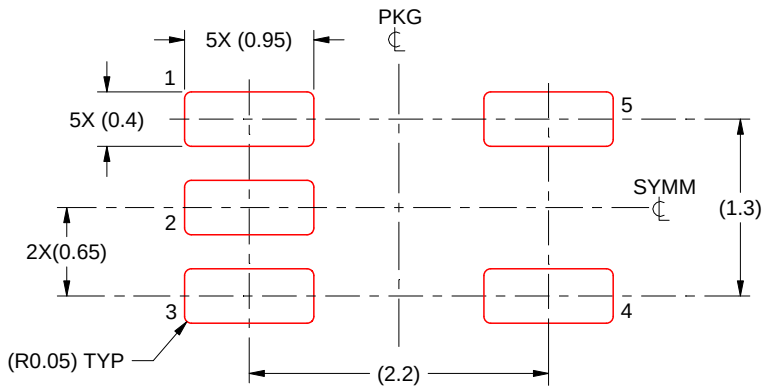
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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