Features

- **Single Voltage Operation Read/Write: 2.65V - 3.6V**
- **2.7V - 3.6V Read/Write**
- **Access Time – 70 ns**
- **Sector Erase Architecture**
  - **One Hundred Twenty-seven 32K Word Main Sectors with Individual Write Lockout**
  - **Eight 4K Word Sectors with Individual Write Lockout**
- **Fast Word Program Time – 10 µs**
- **Typical Sector Erase Time: 32K Word Sectors – 500 ms; 4K Word Sectors – 100 ms**
- **Suspend/Resume Feature for Erase and Program**
  - **Supports Reading and Programming Data from Any Sector by Suspending Erase of a Different Sector**
  - **Supports Reading Any Word by Suspending Programming of Any Other Word**
- **Low-power Operation**
  - **10 mA Active**
  - **15 µA Standby**
- **Data Polling and Toggle Bit for End of Program Detection**
- **VPP Pin for Write Protection and Accelerated Program Operations**
- **RESET Input for Device Initialization**
- **Sector Lockdown Support**
- **TSOP Package**
- **Top or Bottom Boot Block Configuration Available**
- **128-bit Protection Register**
- **Common Flash Interface (CFI)**
- **Green (Pb/Halide-free) Packaging**

1. Description

The AT49BV642D(T) is a 2.7-volt 64-megabit Flash memory organized as 4,194,304 words of 16 bits each. The memory is divided into 135 sectors for erase operations. The device can be read or reprogrammed off a single 2.7V power supply, making it ideally suited for in-system programming.

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors. The end of program or erase is detected by $\overline{\text{Data}}$ Polling or toggle bit.

The VPP pin provides data protection and faster programming times. When the V_{PP} input is below 0.4V, the program and erase functions are inhibited. When V_{PP} is at 1.65V or above, normal program and erase operations can be performed. With V_{PP} at 10.0V, the program (dual-word program command) operation is accelerated.

A six-word command (Enter Single Pulse Program Mode) to remove the requirement of entering the three-word program sequence is offered to further improve programming time. After entering the six-word code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Word Program) is exited by powering down the device, by taking the $\overline{\text{RESET}}$ pin to GND or by a high-to-low transition on the V_{PP} input. Erase, Erase Suspend/Resume, Program Suspend/Resume and Read Reset commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-word code reside in the software of the final product but only exist in external programming code.

64-megabit
(4M x 16)
3-volt Only
Flash Memory

AT49BV642D
AT49BV642DT

Not Recommended for New Design
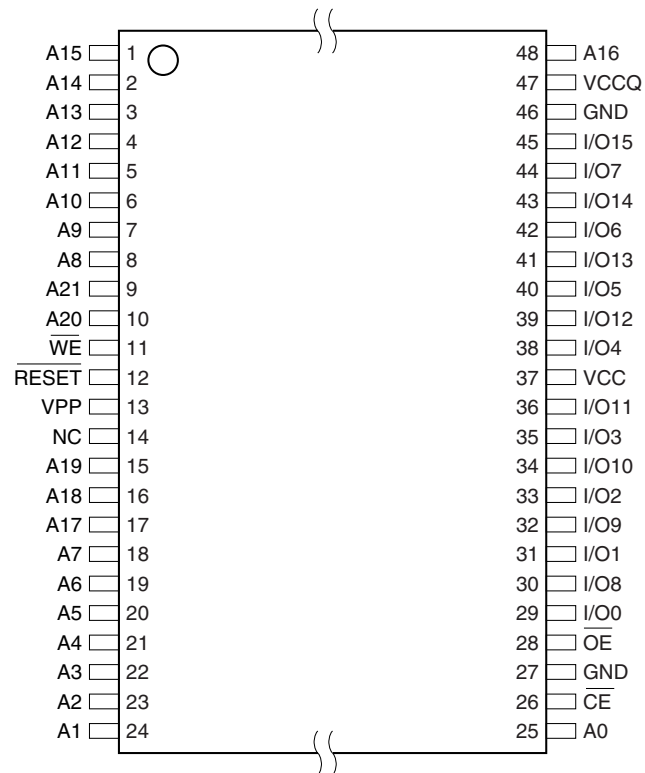Contact Atmel to discuss the latest design in trends and options

2. Pin Configurations

Pin Name	Pin Function
I/O0 - I/O15	Data Inputs/Outputs
A0 - A21	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	Reset
VPP	Write Protection and Power Supply for Accelerated Program Operations
VCCQ	Output Power Supply

2.1 TSOP Top View (Type 1)

Left Pin	#		#	Right Pin
A15	1		48	A16
A14	2		47	VCCQ
A13	3		46	GND
A12	4		45	I/O15
A11	5		44	I/O7
A10	6		43	I/O14
A9	7		42	I/O6
A8	8		41	I/O13
A21	9		40	I/O5
A20	10		39	I/O12
$\overline{WE}$	11		38	I/O4
$\overline{RESET}$	12		37	VCC
VPP	13		36	I/O11
NC	14		35	I/O3
A19	15		34	I/O10
A18	16		33	I/O2
A17	17		32	I/O9
A7	18		31	I/O1
A6	19		30	I/O8
A5	20		29	I/O0
A4	21		28	$\overline{OE}$
A3	22		27	GND
A2	23		26	$\overline{CE}$
A1	24		25	A0

3. Device Operation

3.1 Command Sequences

The device powers on in the read mode. Command sequences are used to place the device in other operating modes such as program and erase. After the completion of a program or an erase cycle, the device enters the read mode. The command sequences are written by applying a low pulse on the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high or by applying a low-going pulse on the $\overline{CE}$ input with $\overline{WE}$ low and $\overline{OE}$ high. The address is latched on the falling edge of the $\overline{WE}$ or $\overline{CE}$ pulse whichever occurs first. Valid data is latched on the rising edge of the $\overline{WE}$ or the $\overline{CE}$ pulse, whichever occurs first. The addresses used in the command sequences are not affected by entering the command sequences.

3.2 Read

The AT49BV642D(T) is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

3.3 Reset

A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ pin halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to read or standby mode, depending upon the state of the control pins.

3.4 Erase

Before a word can be reprogrammed it must be erased. The erased state of the memory bits is a logical "1". The entire memory can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

3.4.1 Chip Erase

Chip Erase is a six-bus cycle operation. The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse. Chip Erase does not alter the data of the protected sectors. After the full chip erase the device will return back to the read mode. The hardware reset during Chip Erase will stop the erase but the data will be of unknown state. Any command during Chip Erase except Erase Suspend will be ignored.

3.4.2 Sector Erase

As an alternative to a full chip erase, the device is organized into multiple sectors that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector whose address is valid at the sixth falling edge of $\overline{WE}$ will be erased provided the given sector has not been protected.

3.5 Word Programming

The device is programmed on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The programming address and data are latched in the fourth cycle. The device will automatically generate the required internal programming pulses. Please note that a "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s.

3.6 Sector Lockdown

Each sector has a programming lockdown feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockdown feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector's usage as a write-protected region is optional to the user.

At power-up or reset, all sectors are unlocked. To activate the lockdown for a specific sector, the six-bus cycle Sector Lockdown command must be issued. Once a sector has been locked down, the contents of the sector is read-only and cannot be erased or programmed.

3.6.1 Sector Lockdown Detection

A software method is available to determine if programming of a sector is locked down. When the device is in the software product identification mode (see "Software Product Identification Entry/Exit" sections on page 23), a read from address location 00002H within a sector will show if programming the sector is locked down. If the data on I/O0 is low, the sector can be programmed; if the data on I/O0 is high, the program lockdown feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

3.6.2 Sector Lockdown Override

The only way to unlock a sector that is locked down is through reset or power-up cycles. After power-up or reset, the content of a sector that is locked down can be erased and reprogrammed.

3.7 Program/Erase Status

The device provides several bits to determine the status of a program or erase operation: I/O2, I/O3, I/O5, I/O6, and I/O7. All other status bits are don't care. The "Status Bit Table" on page 10 and the following four sections describe the function of these bits. To provide greater flexibility for system designers, the AT49BV642D(T) contains a programmable configuration register. The configuration register allows the user to specify the status bit operation. The configuration register can be set to one of two different values, "00" or "01". If the configuration register is set to "00", the part will automatically return to the read mode after a successful program or erase operation. If the configuration register is set to a "01", a Product ID Exit command must be given after a successful program or erase operation before the part will return to the read mode. It is important to note that whether the configuration register is set to a "00" or to a "01", any unsuccessful program or erase operation requires using the Product ID Exit command to return the device to read mode. The default value (after power-up) for the configuration register is "00". Using the four-bus cycle set configuration register command as shown in the "Command Definition Table" on page 11, the value of the configuration register can be changed. Voltages applied to the reset pin will not alter the value of the configuration register. The value of the configuration register will affect the operation of the I/O7 status bit as described below.

3.7.1 Data Polling

The AT49BV642D(T) features Data Polling to indicate the end of a program cycle. If the status configuration register is set to a "00", during a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. Data Polling may begin at any time during the program cycle. Please see "Status Bit Table" on page 10 for more details.

If the status bit configuration register is set to a "01", the I/O7 status bit will be low while the device is actively programming or erasing data. I/O7 will go high when the device has completed a program or erase operation. Once I/O7 has gone high, status information on the other pins can be checked.

The Data Polling status bit must be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 3-1 and 3-2 on page 8.

3.7.2 Toggle Bit

In addition to Data Polling, the AT49BV642D(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the memory will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. Please see "Status Bit Table" on page 10 for more details.

The toggle bit status bit should be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 3-3 and 3-4 on page 9.

3.7.3 Erase/Program Status Bit

The device offers a status bit on I/O5 that indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a "1", the device is unable to verify that an erase or a word program operation has been successfully performed. The device may also output a "1" on I/O5 if the system tries to program a "1" to a location that was previously programmed to a "0". Only an erase operation can change a "0" back to a "1". If a program (Sector Erase) command is issued to a protected sector, the protected sector will not be programmed (erased). The device will go to a status read mode and the I/O5 status bit will be set high, indicating the program (erase) operation did not complete as requested. Once the erase/program status bit has been set to a "1", the system must write the Product ID Exit command to return to the read mode. The erase/program status bit is a "0" while the erase or program operation is still in progress. Please see "Status Bit Table" on page 10 for more details.

3.7.4 VPP Status Bit

The AT49BV642D(T) provides a status bit on I/O3 that provides information regarding the voltage level of the VPP pin. During a program or erase operation, if the voltage on the VPP pin is not high enough to perform the desired operation successfully, the I/O3 status bit will be a "1". Once the V_{PP} status bit has been set to a "1", the system must write the Product ID Exit command to return to the read mode. On the other hand, if the voltage level is high enough to perform a program or erase operation successfully, the V_{PP} status bit will output a "0". Please see "Status Bit Table" on page 10 for more details.

3.8   Erase Suspend/Erase Resume

The Erase Suspend command allows the system to interrupt a sector erase operation and then program or read data from a different sector within the memory. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command. The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

3.9   Program Suspend/Program Resume

The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 10 µs to suspend the programming operation. After the programming operation has been suspended, the system can then read from any other word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same.

3.10   128-Bit Protection Register

The AT49BV642D(T) contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. To program block B in the protection register, the four-bus cycle Program Protection Register command must be used as shown in the "Command Definition Table" on page 11. To lock out block B, the four-bus cycle lock protection register command must be used as shown in the Command Definition table. Data bit D1 must be zero during the fourth bus cycle. All other data bits during the fourth bus cycle are don't cares. To determine whether block B is locked out, the status of Block B Protection command is given. If data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. Please see the "Protection Register Addressing Table" on page 12 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether block B is protected or not or reading the protection register, the Product ID Exit command must be given prior to performing any other operation.

3.11 Common Flash Interface (CFI)

Common Flash Interface (CFI) is a published, standardized data structure that may be read from a Flash device. CFI allows system software to query the installed device to determine the configurations, various electrical and timing parameters, and functions supported by the device. CFI is used to allow the system to learn how to interface to the Flash device most optimally. The two primary benefits of using CFI are ease of upgrading and second source availability. The command to enter the CFI Query mode is a one-bus cycle command which requires writing data 98h to address 55h. The CFI Query command can be written when the device is ready to read data or can also be written when the part is in the product ID mode. Once in the CFI Query mode, the system can read CFI data at the addresses given in the "Common Flash Interface Definition Table" on page 24. To exit the CFI Query mode, the product ID exit command must be given.

3.12 Hardware Data Protection

Hardware features protect against inadvertent programs to the AT49BV642D(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time-out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) V_{PP} is less than V_{ILPP}.

3.13 Input Levels

While operating with a 2.65V to 3.6V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can be driven from 0 to V_{CCQ} + 0.6V.

3.14 Output Levels

For the AT49BV642D(T), output high levels are equal to V_{CCQ} - 0.1V (not V_{CC}). For 2.65V to 3.6V output levels, V_{CCQ} must be tied to V_{CC}.

Figure 3-1. $\overline{\text{Data}}$ Polling Algorithm
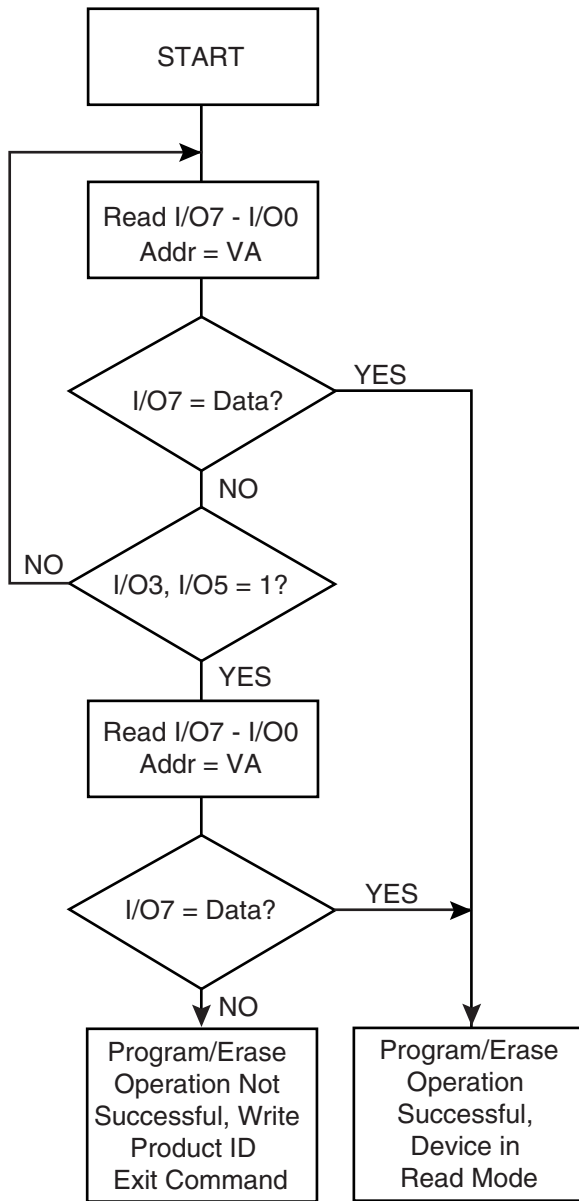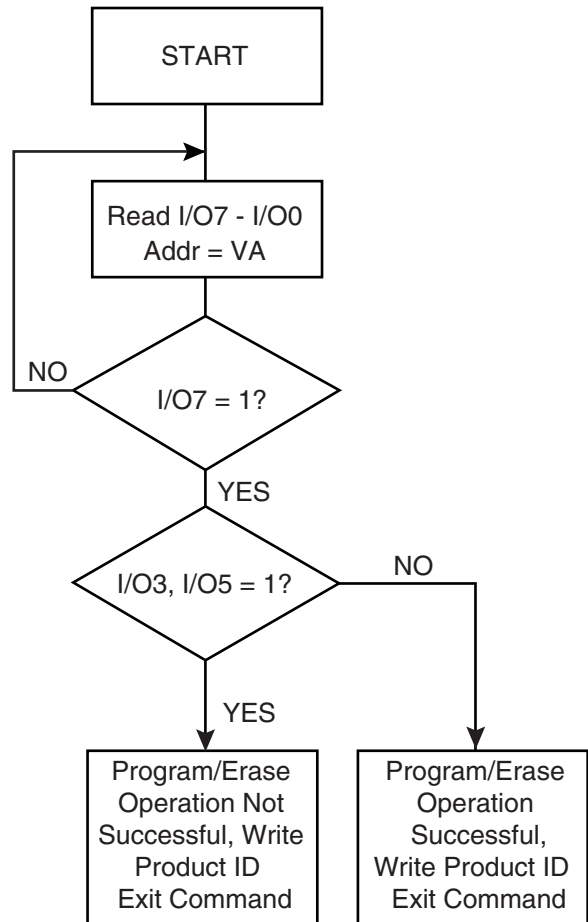(Configuration Register = 00)

Figure 3-2. $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 01)

START

Read I/O7 - I/O0
Addr = VA

I/O7 = Data?   YES

NO

I/O3, I/O5 = 1?   NO

YES

Read I/O7 - I/O0
Addr = VA

I/O7 = Data?   YES

NO

Program/Erase
Operation Not
Successful, Write
Product ID
Exit Command

Program/Erase
Operation
Successful,
Device in
Read Mode

START

Read I/O7 - I/O0
Addr = VA

NO

I/O7 = 1?

YES

I/O3, I/O5 = 1?   NO

YES

Program/Erase
Operation Not
Successful, Write
Product ID
Exit Command

Program/Erase
Operation
Successful,
Write Product ID
Exit Command

Note: 1. VA = Valid address for programming. During a sector
             erase operation, a valid address is any sector
             address within the sector being erased. During chip
             erase, a valid address is any non-protected sector
             address.

Notes: 1. VA = Valid address for programming. During a sector
             erase operation, a valid address is any sector
             address within the sector being erased. During chip
             erase, a valid address is any non-protected sector
             address.
         2. I/O7 should be rechecked even if I/O5 = "1" because
             I/O7 may change simultaneously with I/O5.

8   **AT49BV642D(T)**

Figure 3-3. Toggle Bit Algorithm
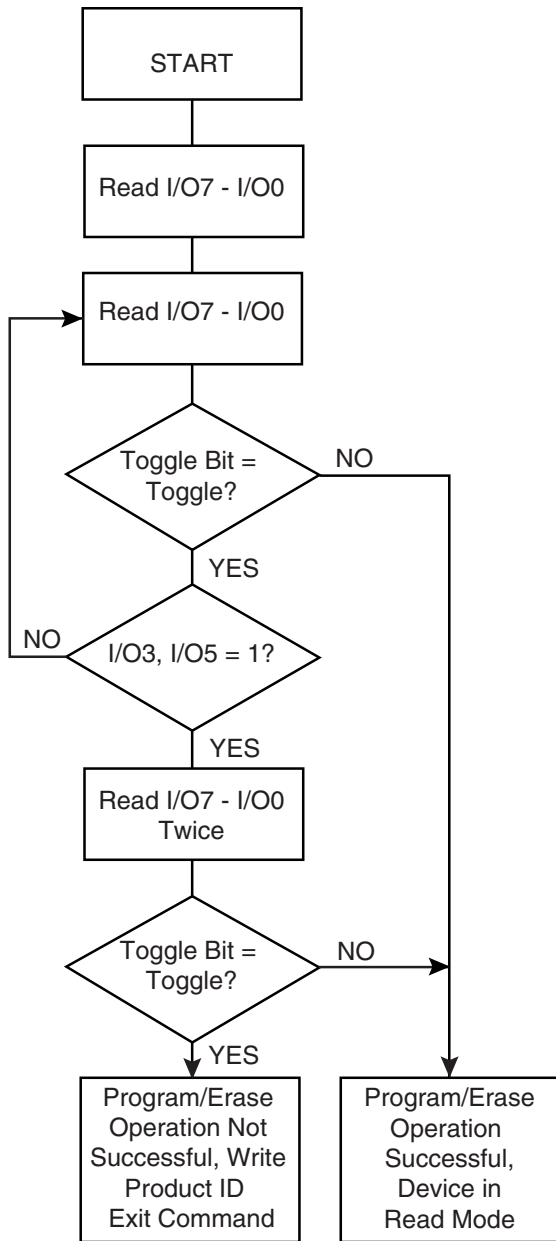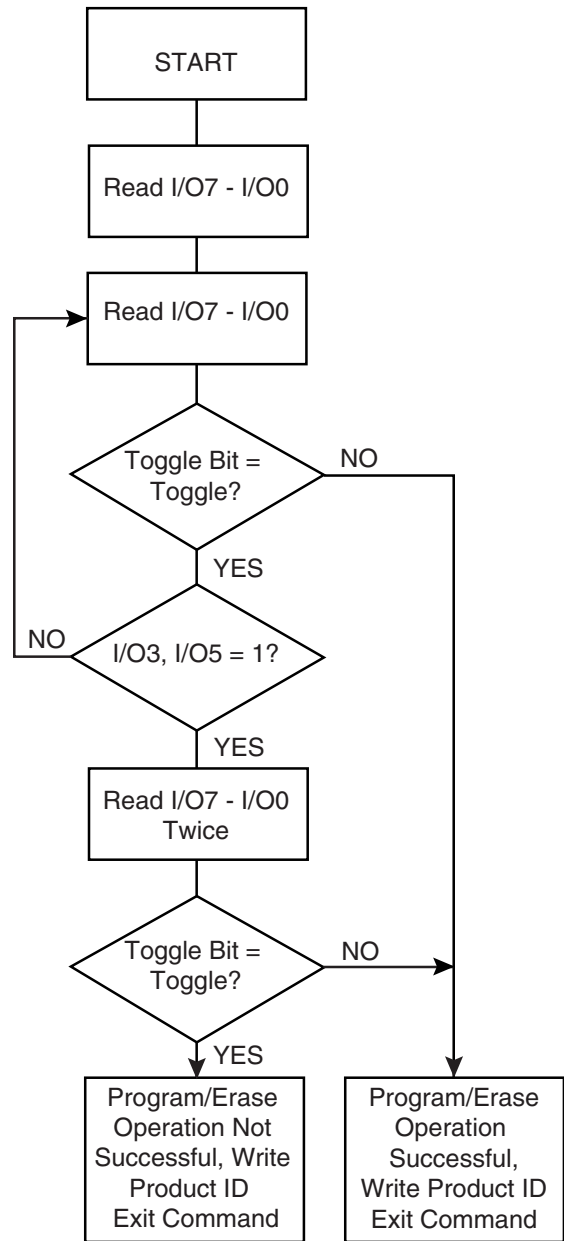(Configuration Register = 00)

Figure 3-4. Toggle Bit Algorithm
(Configuration Register = 01)

Note: 1. The system should recheck the toggle bit even if
I/O5 = "1" because the toggle bit may stop toggling
as I/O5 changes to "1".

Note: 1. The system should recheck the toggle bit even if
I/O5 = "1" because the toggle bit may stop toggling
as I/O5 changes to "1".

4. Status Bit Table

	Status Bit					
	I/O7	**I/O7**	**I/O6**	**I/O5**[1]	**I/O3**[2]	**I/O2**
Configuration Register	**00**	**01**	**00/01**	**00/01**	**00/01**	**00/01**
Programming	$\overline{I/O7}$	0	TOGGLE	0	0	1
Erasing	0	0	TOGGLE	0	0	TOGGLE
Erase Suspended & Read Erasing Sector	1	1	1	0	0	TOGGLE
Erase Suspended & Read Non-erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA
Erase Suspended & Program Non-erasing Sector	$\overline{I/O7}$	0	TOGGLE	0	0	TOGGLE
Erase Suspended & Program Suspended and Reading from Non-suspended Sectors	DATA	DATA	DATA	DATA	DATA	DATA
Program Suspended & Read Programming Sector	I/O7	1	1	0	0	TOGGLE
Program Suspended & Read Non-programming Sector	DATA	DATA	DATA	DATA	DATA	DATA

Notes: 1. I/O5 switches to a "1" when a program or an erase operation has exceeded the maximum time limits or when a program or sector erase operation is performed on a protected sector.

2. I/O3 switches to a "1" when the V_{PP} level is not high enough to successfully perform program and erase operations.

5. Command Definition Table

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[3]	30
Word Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Dual-Word Program[4]	5	555	AA	AAA	55	555	E0	Addr0	D_{IN0}	Addr1	D_{IN1}		
Enter Single-pulse Program Mode	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	A0
Single-pulse Word Program Mode	1	Addr	D_{IN}										
Sector Lockdown[5]	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[3][5]	60
Erase/Program Suspend	1	xxx	B0										
Erase/Program Resume	1	xxx	30										
Product ID Entry[6]	3	555	AA	AAA	55	555	90						
Product ID Exit[7]	3	555	AA	AAA	55	555	F0[8]						
Product ID Exit[7]	1	xxx	F0[8]										
Program Protection Register – Block B	4	555	AA	AAA	55	555	C0	Addr[9]	D_{IN}				
Lock Protection Register – Block B	4	555	AA	AAA	55	555	C0	80	X0				
Status of Block B Protection	4	555	AA	AAA	55	555	90	80	D_{OUT}[10]				
Set Configuration Register	4	555	AA	AAA	55	555	D0	xxx	00/01[11]				
CFI Query	1	X55	98										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex). The ADDRESS FORMAT in each bus cycle is as follows: A11 - A0 (Hex), A11 - A21 (Don't Care).
2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
3. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 13 - 16 for details).
4. The fast programming option enables the user to program two words in parallel only when V_{PP} = 10V. The addresses, Addr0 and Addr1, of the two words, D_{IN0} and D_{IN1}, must only differ in address A0. This command should be used for manufacturing purpose only.
5. Once a sector is in the lockdown mode, the data in the protected sector cannot be changed, unless the chip is reset or power cycled.
6. During the fourth bus cycle, the manufacturer code is read from address 00000H, the device code is read from address 00001H, and the data in the protection register is read from addresses 000081H - 000088H.
7. Either one of the Product ID Exit commands can be used.
8. Bytes of data other than F0 may be used to exit the product ID mode. However, it is recommended that F0 be used.
9. Any address within the user programmable register region. Please see "Protection Register Addressing Table" on page 12.
10. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
11. The default state (after power-up) of the configuration register is "00".

6.   Absolute Maximum Ratings*

Temperature under Bias .... -55°C to +125°C

Storage Temperature..................................... -65°C to +150°C

All Input Voltages Except V_{PP}
(including NC Pins)
with Respect to Ground ....-0.6V to +6.25V

V_{PP} Input Voltage
with Respect to Ground ....0V to 10.0V

All Output Voltages
with Respect to Ground ....-0.6V to V_{CCQ} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.   Protection Register Addressing Table

Word	Use	Block	A7	A6	A5	A4	A3	A2	A1	A0
0	Factory	A	1	0	0	0	0	0	0	1
1	Factory	A	1	0	0	0	0	0	1	0
2	Factory	A	1	0	0	0	0	0	1	1
3	Factory	A	1	0	0	0	0	1	0	0
4	User	B	1	0	0	0	0	1	0	1
5	User	B	1	0	0	0	0	1	1	0
6	User	B	1	0	0	0	0	1	1	1
7	User	B	1	0	0	0	1	0	0	0

Note: All address lines not specified in the above table must be "0" when accessing the protection register, i.e. A21 -A8 = 0.

8. Memory Organization – AT49BV642D

Sector	Size (Words)	x16 Address Range (A21 - A0)
SA0	4K	00000 - 00FFF
SA1	4K	01000 - 01FFF
SA2	4K	02000 - 02FFF
SA3	4K	03000 - 03FFF
SA4	4K	04000 - 04FFF
SA5	4K	05000 - 05FFF
SA6	4K	06000 - 06FFF
SA7	4K	07000 - 07FFF
SA8	32K	08000 - 0FFFF
SA9	32K	10000 - 17FFF
SA10	32K	18000 - 1FFFF
SA11	32K	20000 - 27FFF
SA12	32K	28000 - 2FFFF
SA13	32K	30000 - 37FFF
SA14	32K	38000 - 3FFFF
SA15	32K	40000 - 47FFF
SA16	32K	48000 - 4FFFF
SA17	32K	50000 - 57FFF
SA18	32K	58000 - 5FFFF
SA19	32K	60000 - 67FFF
SA20	32K	68000 - 6FFFF
SA21	32K	70000 - 77FFF
SA22	32K	78000 - 7FFFF
SA23	32K	80000 - 87FFF
SA24	32K	88000 - 8FFFF
SA25	32K	90000 - 97FFF
SA26	32K	98000 - 9FFFF
SA27	32K	A0000 - A7FFF
SA28	32K	A8000 - AFFFF
SA29	32K	B0000 - B7FFF
SA30	32K	B8000 - BFFFF
SA31	32K	C0000 - C7FFF
SA32	32K	C8000 - CFFFF

8. Memory Organization – AT49BV642D (Continued)

Sector	Size (Words)	x16 Address Range (A21 - A0)
SA33	32K	D0000 - D7FFF
SA34	32K	D8000 - DFFFF
SA35	32K	E0000 - E7FFF
SA36	32K	E8000 - EFFFF
SA37	32K	F0000 - F7FFF
SA38	32K	F8000 - FFFFF
SA39	32K	100000 - 107FFF
SA40	32K	108000 - 10FFFF
SA41	32K	110000 - 117FFF
SA42	32K	118000 - 11FFFF
SA43	32K	120000 - 127FFF
SA44	32K	128000 - 12FFFF
SA45	32K	130000 - 137FFF
SA46	32K	138000 - 13FFFF
SA47	32K	140000 - 147FFF
SA48	32K	148000 - 14FFFF
SA49	32K	150000 - 157FFF
SA50	32K	158000 - 15FFFF
SA51	32K	160000 - 167FFF
SA52	32K	168000 - 16FFFF
SA53	32K	170000 - 177FFF
SA54	32K	178000 - 17FFFF
SA55	32K	180000 - 187FFF
SA56	32K	188000 - 18FFFF
SA57	32K	190000 - 197FFF
SA58	32K	198000 - 19FFFF
SA59	32K	1A0000 - 1A7FFF
SA60	32K	1A8000 - 1AFFFF
SA61	32K	1B0000 - 1B7FFF
SA62	32K	1B8000 - 1BFFFF
SA63	32K	1C0000 - 1C7FFF
SA64	32K	1C8000 - 1CFFFF
SA65	32K	1D0000 - 1D7FFF

Sector	Size (Words)	x16 Address Range (A21 - A0)
SA66	32K	1D8000 - 1DFFFF
SA67	32K	1E0000 - 1E7FFF
SA68	32K	1E8000 - 1EFFFF
SA69	32K	1F0000 - 1F7FFF
SA70	32K	1F8000 - 1FFFFF
SA71	32K	200000 - 207FFF
SA72	32K	208000 - 20FFFF
SA73	32K	210000 - 217FFF
SA74	32K	218000 - 21FFFF
SA75	32K	220000 - 227FFF
SA76	32K	228000 - 22FFFF
SA77	32K	230000 - 237FFF
SA78	32K	238000 - 23FFFF
SA79	32K	240000 - 247FFF
SA80	32K	248000 - 24FFFF
SA81	32K	250000 - 257FFF
SA82	32K	258000 - 25FFFF
SA83	32K	260000 - 267FFF
SA84	32K	268000 - 26FFFF
SA85	32K	270000 - 277FFF
SA86	32K	278000 - 27FFFF
SA87	32K	280000 - 287FFF
SA88	32K	288000 - 28FFFF
SA89	32K	290000 - 297FFF
SA90	32K	298000 - 29FFFF
SA91	32K	2A0000 - 2A7FFF
SA92	32K	2A8000 - 2AFFFF
SA93	32K	2B0000 - 2B7FFF
SA94	32K	2B8000 - 2BFFFF
SA95	32K	2C0000 - 2C7FFF
SA96	32K	2C8000 - 2CFFFF
SA97	32K	2D0000 - 2D7FFF
SA98	32K	2D8000 - 2DFFFF
SA99	32K	2E0000 - 2E7FFF

Sector	Size (Words)	x16 Address Range (A21 - A0)
SA100	32K	2E8000 - 2EFFFF
SA101	32K	2F0000 - 2F7FFF
SA102	32K	2F8000 - 2FFFFF
SA103	32K	300000 - 307FFF
SA104	32K	308000 - 30FFFF
SA105	32K	310000 - 317FFF
SA106	32K	318000 - 31FFFF
SA107	32K	320000 - 327FFF
SA108	32K	328000 - 32FFFF
SA109	32K	330000 - 337FFF
SA110	32K	338000 - 33FFFF
SA111	32K	340000 - 347FFF
SA112	32K	348000 - 34FFFF
SA113	32K	350000 - 357FFF
SA114	32K	358000 - 35FFFF
SA115	32K	360000 - 367FFF
SA116	32K	368000 - 36FFFF
SA117	32K	370000 - 377FFF
SA118	32K	378000 - 37FFFF
SA119	32K	380000 - 387FFF
SA120	32K	388000 - 38FFFF
SA121	32K	390000 - 397FFF
SA122	32K	398000 - 39FFFF
SA123	32K	3A0000 - 3A7FFF
SA124	32K	3A8000 - 3AFFFF
SA125	32K	3B0000 - 3B7FFF
SA126	32K	3B8000 - 3BFFFF
SA127	32K	3C0000 - 3C7FFF
SA128	32K	3C8000 - 3CFFFF
SA129	32K	3D0000 - 3D7FFF
SA130	32K	3D8000 - 3DFFFF
SA131	32K	3E0000 - 3E7FFF
SA132	32K	3E8000 - 3EFFFF
SA133	32K	3F0000 - 3F7FFF
SA134	32K	3F8000 - 3FFFFF

9. Memory Organization – AT49BV642DT

Sector	Size (Words)	x16 Address Range (A21 - A0)
SA0	32K	00000 - 07FFF
SA1	32K	08000 - 0FFFF
SA2	32K	10000 - 17FFF
SA3	32K	18000 - 1FFFF
SA4	32K	20000 - 27FFF
SA5	32K	28000 - 2FFFF
SA6	32K	30000 - 37FFF
SA7	32K	38000 - 3FFFF
SA8	32K	40000 - 47FFF
SA9	32K	48000 - 4FFFF
SA10	32K	50000 - 57FFF
SA11	32K	58000 - 5FFFF
SA12	32K	60000 - 67FFF
SA13	32K	68000 - 6FFFF
SA14	32K	70000 - 77FFF
SA15	32K	78000 - 7FFFF
SA16	32K	80000 - 87FFF
SA17	32K	88000 - 8FFFF
SA18	32K	90000 - 97FFF
SA19	32K	98000 - 9FFFF
SA20	32K	A0000 - A7FFF
SA21	32K	A8000 - AFFFF
SA22	32K	B0000 - B7FFF
SA23	32K	B8000 - BFFFF
SA24	32K	C0000 - C7FFF
SA25	32K	C8000 - CFFFF
SA26	32K	D0000 - D7FFF
SA27	32K	D8000 - DFFFF
SA28	32K	E0000 - E7FFF
SA29	32K	E8000 - EFFFF
SA30	32K	F0000 - F7FFF
SA31	32K	F8000 - FFFFF
SA32	32K	100000 - 107FFF
SA33	32K	108000 - 10FFFF
SA34	32K	110000 - 117FFF
SA35	32K	118000 - 11FFFF

9. Memory Organization – AT49BV642DT (Continued)

Sector	Size (Words)	x16 Address Range (A21 - A0)
SA36	32K	120000 - 127FFF
SA37	32K	128000 - 12FFFF
SA38	32K	130000 - 137FFF
SA39	32K	138000 - 13FFFF
SA40	32K	140000 - 147FFF
SA41	32K	148000 - 14FFFF
SA42	32K	150000 - 157FFF
SA43	32K	158000 - 15FFFF
SA44	32K	160000 - 167FFF
SA45	32K	168000 - 16FFFF
SA46	32K	170000 - 177FFF
SA47	32K	178000 - 17FFFF
SA48	32K	180000 - 187FFF
SA49	32K	188000 - 18FFFF
SA50	32K	190000 - 197FFF
SA51	32K	198000 - 19FFFF
SA52	32K	1A0000 - 1A7FFF
SA53	32K	1A8000 - 1AFFFF
SA54	32K	1B0000 - 1B7FFF
SA55	32K	1B8000 - 1BFFFF
SA56	32K	1C0000 - 1C7FFF
SA57	32K	1C8000 - 1CFFFF
SA58	32K	1D0000 - 1D7FFF
SA59	32K	1D8000 - 1DFFFF
SA60	32K	1E0000 - 1E7FFF
SA61	32K	1E8000 - 1EFFFF
SA62	32K	1F0000 - 1F7FFF
SA63	32K	1F8000 - 1FFFFF
SA64	32K	200000 - 207FFF
SA65	32K	208000 - 20FFFF
SA66	32K	210000 - 217FFF
SA67	32K	218000 - 21FFFF
SA68	32K	220000 - 227FFF
SA69	32K	228000 - 22FFFF
SA70	32K	230000 - 237FFF
SA71	32K	238000 - 23FFFF

Sector	Size (Words)	x16 Address Range (A21 - A0)
SA72	32K	240000 - 247FFF
SA73	32K	248000 - 24FFFF
SA74	32K	250000 - 257FFF
SA75	32K	258000 - 25FFFF
SA76	32K	260000 - 267FFF
SA77	32K	268000 - 26FFFF
SA78	32K	270000 - 277FFF
SA79	32K	278000 - 27FFFF
SA80	32K	280000 - 287FFF
SA81	32K	288000 - 28FFFF
SA82	32K	290000 - 297FFF
SA83	32K	298000 -29FFFF
SA84	32K	2A0000 - 2A7FFF
SA85	32K	2A8000 - 2AFFFF
SA86	32K	2B0000 - 2B7FFF
SA87	32K	2B8000 - 2BFFFF
SA88	32K	2C0000 - 2C7FFF
SA89	32K	2C8000 - 2CFFFF
SA90	32K	2D0000 - 2D7FFF
SA91	32K	2D8000 - 2DFFFF
SA92	32K	2E0000 - 2E7FFF
SA93	32K	2E8000 - 2EFFFF
SA94	32K	2F0000 - 2F7FFF
SA95	32K	2F8000 - 2FFFFF
SA96	32K	300000 - 307FFF
SA97	32K	308000 - 30FFFF
SA98	32K	310000 - 317FFF
SA99	32K	318000 - 31FFFF
SA100	32K	320000 - 327FFF
SA101	32K	328000 - 32FFFF
SA102	32K	330000 - 337FFF
SA103	32K	338000 - 33FFFF

Sector	Size (Words)	x16 Address Range (A21 - A0)
SA104	32K	340000 - 347FFF
SA105	32K	348000 - 34FFFF
SA106	32K	350000 - 357FFF
SA107	32K	358000 - 35FFFF
SA108	32K	360000 - 367FFF
SA109	32K	368000 - 36FFFF
SA110	32K	370000 - 377FFF
SA111	32K	378000 - 37FFFF
SA112	32K	380000 - 387FFF
SA113	32K	388000 - 38FFFF
SA114	32K	390000 - 397FFF
SA115	32K	398000 - 39FFFF
SA116	32K	3A0000 - 3A7FFF
SA117	32K	3A8000 - 3AFFFF
SA118	32K	3B0000 - 3B7FFF
SA119	32K	3B8000 - 3BFFFF
SA120	32K	3C0000 - 3C7FFF
SA121	32K	3C8000 - 3CFFFF
SA122	32K	3D0000 - 3D7FFF
SA123	32K	3D8000 - 3DFFFF
SA124	32K	3E0000 - 3E7FFF
SA125	32K	3E8000 - 3EFFFF
SA126	32K	3F0000 - 3F7FFF
SA127	4K	3F8000 - 3F8FFF
SA128	4K	3F9000 - 3F9FFF
SA129	4K	3FA000 - 3FAFFF
SA130	4K	3FB000 - 3FBFFF
SA131	4K	3FC000 - 3FCFFF
SA132	4K	3FD000 - 3FDFFF
SA133	4K	3FE000 - 3FEFFF
SA134	4K	3FF000 - 3FFFFF

10. DC and AC Operating Range

		AT49BV642D(T) - 70
Operating Temperature (Case)	Industrial	-40°C - 85°C
V_{CC} Power Supply		2.7V - 3.6V

11. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}[1]	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X[2]	Ai	D_{OUT}
Program/Erase[3]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IHPP}[4]	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[2]	X	V_{IH}	X	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}	X		
	X	V_{IL}	X	V_{IH}	X		
	X	X	X	X	V_{ILPP}[5]		
Output Disable	X	V_{IH}	X	V_{IH}	X		High Z
Reset	X	X	X	V_{IL}	X	X	High Z
Software Product Identification				V_{IH}		A0 = V_{IL}, A1 - A21 = V_{IL}	Manufacturer Code[6]
						A0 = V_{IH}, A1 - A21 = V_{IL}	Device Code[6]

Notes: 1. The VPP pin can be tied to V_{CC}. For faster program operations, V_{PP} can be set to 9.5V ± 0.5V.
2. X can be V_{IL} or V_{IH}.
3. Refer to program cycle waveforms on page 21.
4. V_{IHPP} (min) = 1.65V.
5. V_{ILPP} (max) = 0.4V.
6. Manufacturer Code: 001FH; Device Code: 01D6H - AT49BV642D; 01D2H - AT49BV642DT.

12. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}			2	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			2	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CCQ} - 0.3V to V_{CC}		15	25	µA
I_{CC}[1]	V_{CC} Active Read Current	f = 5 MHz; I_{OUT} = 0 mA		10	15	mA
I_{CC1}	V_{CC} Programming Current				25	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		V_{CCQ} - 0.6			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CCQ} - 0.1			V

Note: 1.   In the erase mode, I_{CC} is 25 mA.

13. Input Test Waveforms and Measurement Level

t_R, t_F < 5 ns
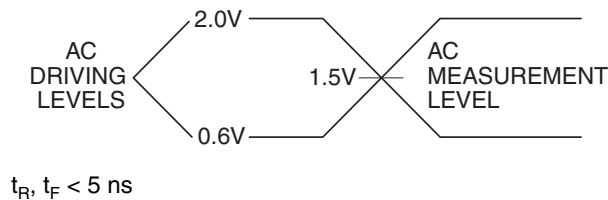
14. Output Test Load
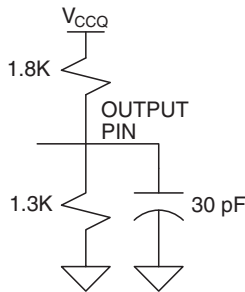
15. Pin Capacitance

f = 1 MHz, T = 25°C[1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1.   This parameter is characterized and is not 100% tested.

16. AC Read Characteristics

Symbol	Parameter	Min	Max	Units
t_{RC}	Read Cycle Time	70		ns
t_{ACC}	Access, Address to Data Valid		70	ns
t_{CE}	Access, $\overline{CE}$ to Data Valid		70	ns
t_{OE}	$\overline{OE}$ to Data Valid		20	ns
t_{DF}	$\overline{CE}$, $\overline{OE}$ High to Data Float		25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever Occurs First	0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		100	ns

17. Asynchronous Read Cycle Waveform[(1)(2)(3)]
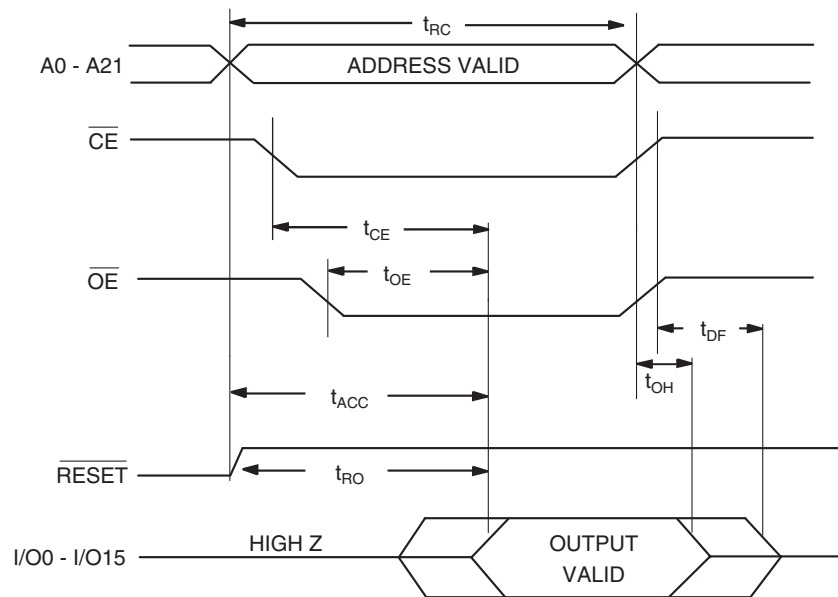
Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).

18. AC Word Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	25		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	25		ns
t_{WPH}	Write Pulse Width High	15		ns
t_{DS}	Data Setup Time	25		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

19. AC Word Load Waveforms

19.1 $\overline{WE}$ Controlled
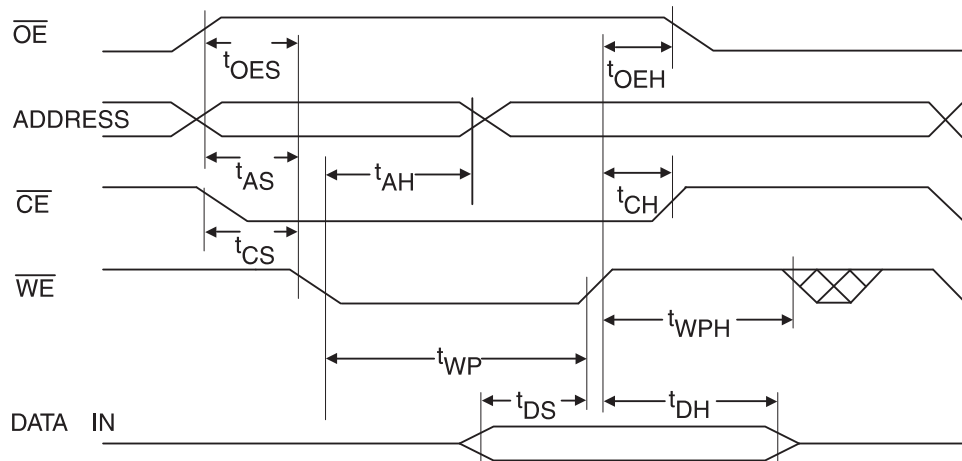
19.2 $\overline{CE}$ Controlled
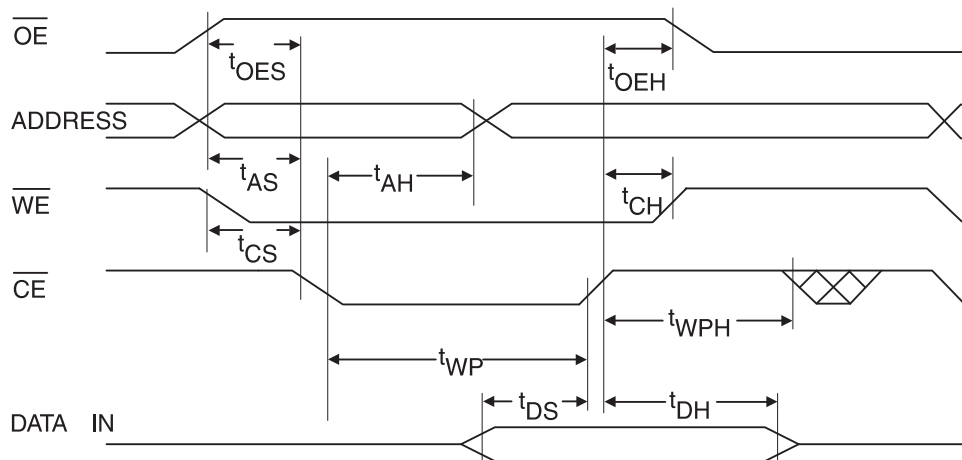
20. Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time		10	120	µs
t_{BPD}	Word Programming Time in Dual Programming Mode		5	60	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	25			ns
t_{DS}	Data Setup Time	25			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	25			ns
t_{WPH}	Write Pulse Width High	15			ns
t_{WC}	Write Cycle Time	70			ns
t_{RP}	$\overline{Reset}$ Pulse Width	500			ns
t_{EC}	Chip Erase Cycle Time		64		seconds
t_{SEC1}	Sector Erase Cycle Time (4K Word Sectors)		0.1	2.0	seconds
t_{SEC2}	Sector Erase Cycle Time (32K Word Sectors)		0.5	6.0	seconds
t_{ES}	Erase Suspend Time			15	µs
t_{PS}	Program Suspend Time			10	µs

21. Program Cycle Waveforms
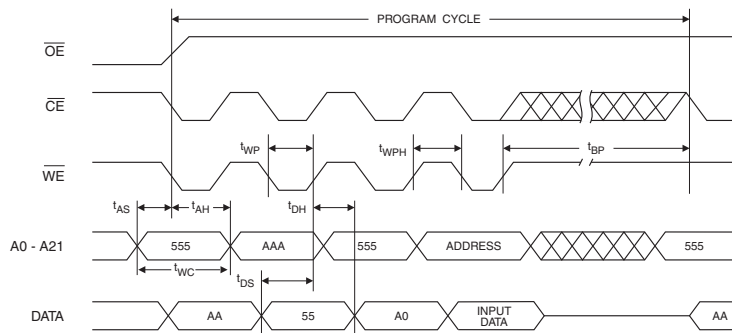
22. Sector or Chip Erase Cycle Waveforms
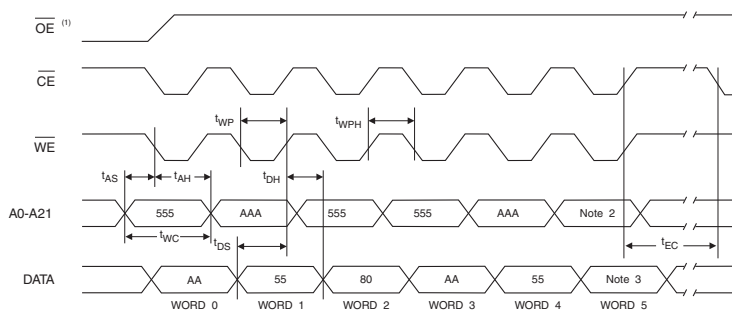
Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 3 under "Command Definition Table" on page 11.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

23. $\overline{\text{Data}}$ Polling Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
       2. See t_{OE} spec on page 19.

24. $\overline{\text{Data}}$ Polling Waveforms
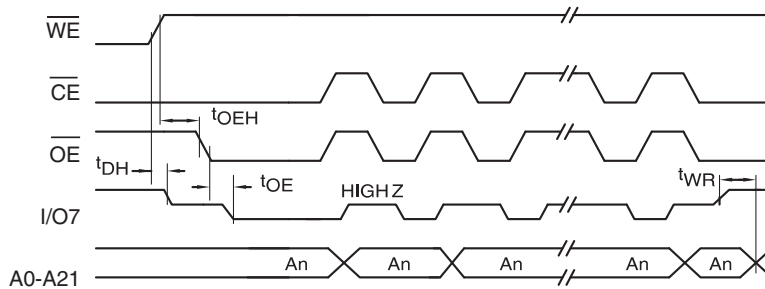
25. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{\text{OE}}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
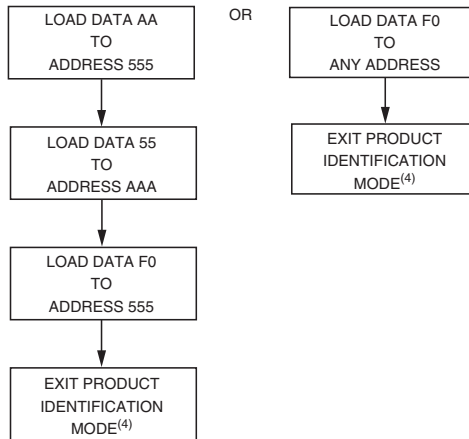   2. See t_{OE} spec on page 19.

26. Toggle Bit Waveforms[1][2][3]
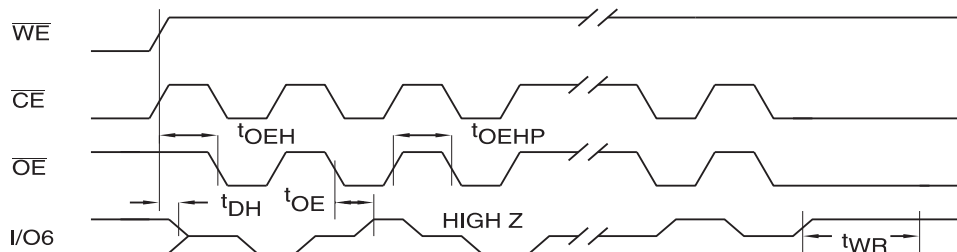
Notes: 1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit.
         The t_{OEHP} specification must be met by the toggling input(s).
       2. Beginning and ending state of I/O6 will vary.
       3. Any address location may be used but the address should not vary.

27. Software Product Identification Entry[1]

```
LOAD DATA AA
TO
ADDRESS 555
        │
        ▼
LOAD DATA 55
TO
ADDRESS AAA
        │
        ▼
LOAD DATA 90
TO
ADDRESS 555
        │
        ▼
ENTER PRODUCT
IDENTIFICATION
MODE[2][3][5]
```

28. Software Product Identification Exit[1][6]

```
LOAD DATA AA          OR        LOAD DATA F0
TO                               TO
ADDRESS 555                      ANY ADDRESS
     │                              │
     ▼                              ▼
LOAD DATA 55                     EXIT PRODUCT
TO                               IDENTIFICATION
ADDRESS AAA                      MODE[4]
     │
     ▼
LOAD DATA F0
TO
ADDRESS 555
     │
     ▼
EXIT PRODUCT
IDENTIFICATION
MODE[4]
```
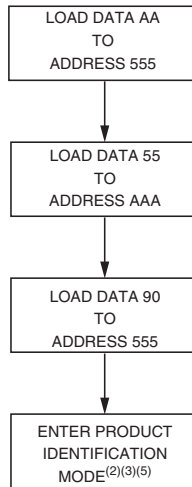
Notes: 1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A11 - A0 (Hex), and A11 - A21 (Don't Care).
2. A1 - A21 = V_{IL}. Manufacturer Code is read for A0 = V_{IL}; Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 001FH(x16)
Device Code: 01D6H – AT49BV642D;
01D2H – AT49BV642DT.
6. Either one of the Product ID Exit commands can be used.

29. Common Flash Interface Definition Table

Address	Data	Comments
10h	0051h	"Q"
11h	0052h	"R"
12h	0059h	"Y"
13h	0002h	
14h	0000h	
15h	0041h	
16h	0000h	
17h	0000h	
18h	0000h	
19h	0000h	
1Ah	0000h	
1Bh	0027h	VCC min write/erase
1Ch	0036h	VCC max write/erase
1Dh	0090h	VPP min voltage
1Eh	00A0h	VPP max voltage
1Fh	0004h	Typ word write – 10 µs
20h	0002h	Typ dual-word program time – 5 µs
21h	0009h	Typ sector erase – 500 ms
22h	0010h	Typ chip erase – 64,300 ms
23h	0004h	Max word write/typ time
24h	0004h	Max dual-word program time/typ time
25h	0004h	Max sector erase/typ sector erase
26h	0004h	Max chip erase/ typ chip erase
27h	0017h	Device size
28h	0001h	x16 device
29h	0000h	x16 device
2Ah	0002h	Max number of bytes in multiple byte write = 4
2Bh	0000h	Max number of bytes in multiple byte write = 4
2Ch	0002h	2 regions, x = 2
2Dh	0007h	8K bytes, Y = 7
2Eh	0000h	8K bytes, Y = 7
2Fh	0020h	8K bytes, Z = 32
30h	0000h	8K bytes, Z = 32
31h	007Eh	64K bytes, Y = 126
32h	0000h	64K bytes, Y = 126
33h	0000h	64K bytes, Z = 256
34h	0001h	64K bytes, Z = 256

29. Common Flash Interface Definition Table (Continued)

Address	Data	Comments
VENDOR SPECIFIC EXTENDED QUERY		
41h	0050h	"P"
42h	0052h	"R"
43h	0049h	"I"
44h	0031h	Major version number, ASCII
45h	0030h	Minor version number, ASCII
46h	0087h	Bit 0 – chip erase supported, 0 – no, 1 – yes Bit 1 – erase suspend supported, 0 – no, 1 – yes Bit 2 – program suspend supported, 0 – no, 1 – yes Bit 3 – simultaneous operations supported, 0 – no, 1 – yes Bit 4 – burst mode read supported, 0 – no, 1 – yes Bit 5 – page mode read supported, 0 – no, 1 – yes Bit 6 – queued erase supported, 0 – no, 1 – yes Bit 7 – protection bits supported, 0 – no, 1 – yes
47h	0000h AT49BV642DT or 0001h AT49BV642D	Bit 0 – top ("0") or bottom ("1") boot block device Undefined bits are "0"
48h	0000h	Bit 0 – 4 word linear burst with wrap around, 0 – no, 1 – yes Bit 1 – 8 word linear burst with wrap around, 0 – no, 1 – yes Bit 2 – continuos burst, 0 – no, 1 – yes Undefined bits are "0"
49h	0000h	Bit 0 – 4 word page, 0 – no, 1 – yes Bit 1 – 8 word page, 0 – no, 1 – yes Undefined bits are "0"
4Ah	0080h	Location of protection register lock byte, the section's first byte
4Bh	0003h	# of bytes in the factory prog section of prot register – 2*n
4Ch	0003h	# of bytes in the user prog section of prot register – 2*n

30. Ordering Information

30.1 Green Package (Pb/Halide-free/RoHS Compliant)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	15	0.025	AT49BV642D-70TU	48T	Industrial (-40° to 85°C)
			AT49BV642DT-70TU		

Package Type	
48T	48-lead, Plastic Thin Small Outline Package (TSOP)

31. Packaging Information

31.1 48T – TSOP

PIN 1

Pin 1 Identifier

D1 D

e

b

E

A2 A

A1

0° ~ 8°

c

L

L1

SEATING PLANE ———— GAGE PLANE

Notes: 1. This package conforms to JEDEC reference MO-142, Variation DD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.
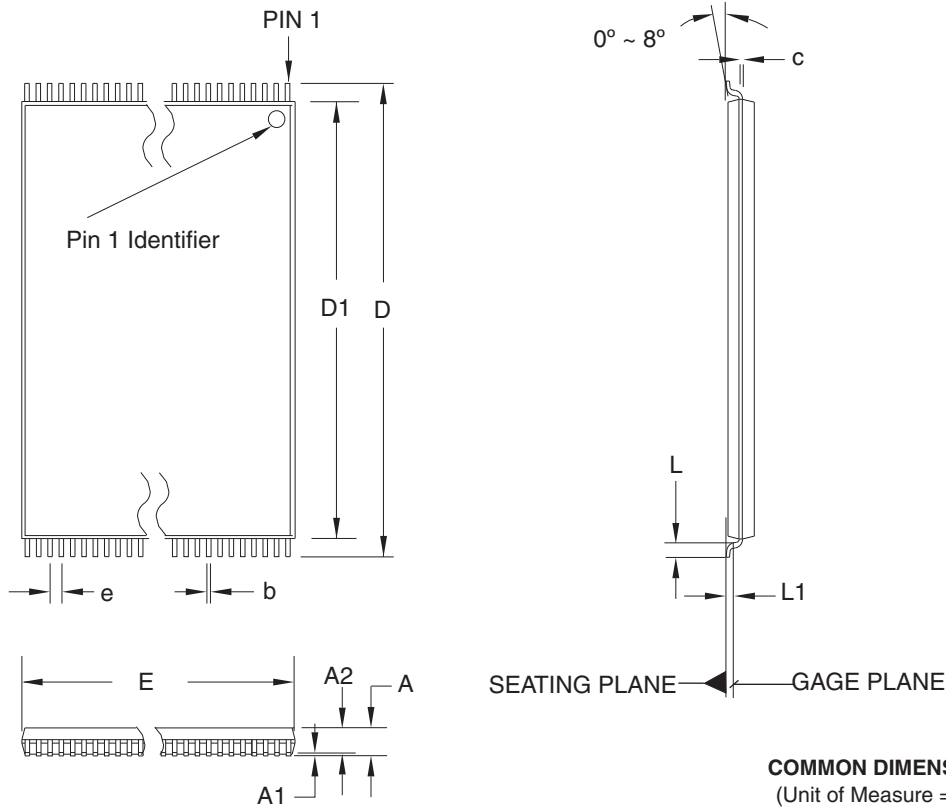
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	11.90	12.00	12.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

10/18/01

	TITLE	DRAWING NO.	REV.
AMEL 2325 Orchard Parkway San Jose, CA 95131	**48T**, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	48T	B

32. Revision History

Revision No.	History
Revision A – April 2006	• Initial Release

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

 Printed on recycled paper.

3631A–FLASH–04/06   xM