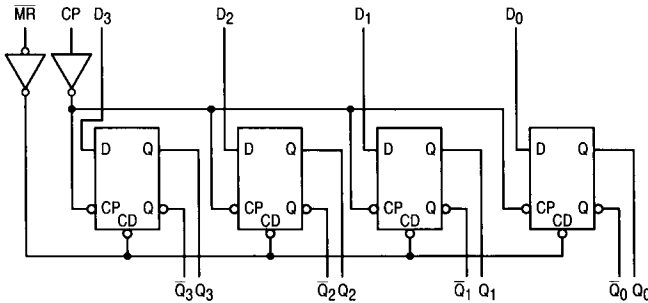# MOTOROLA

Quad D-Type Positive Edge-Triggered Flip-Flop

ELECTRICALLY TESTED PER:
MIL-M-38510/34104

The 54F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset
- True and Complement Output

MPO

AVAILABLE AS:

1) JAN: JM38510/34104BXA
2) SMD: N/A
3) 883: 54F175/BXAJC

X = CASE OUTLINE AS FOLLOWS:
     PACKAGE: CERDIP: E
                    CERFLAT: F
                    LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

LOGIC DIAGRAM

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

AC TEST CIRCUIT
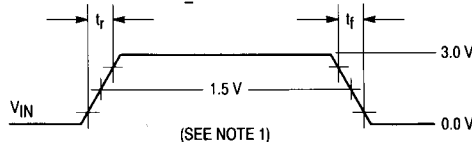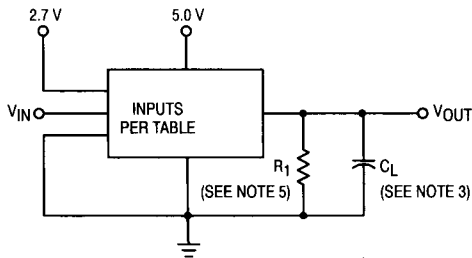
REFERENCE TO NOTES ON PAGE 4-92

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{MR}$	1	1	2	GND
Q_0	2	2	3	OPEN
$\overline{Q}_0$	3	3	4	OPEN
D_0	4	4	5	V_{CC}
D_1	5	5	7	V_{CC}
$\overline{Q}_1$	6	6	8	OPEN
Q_1	7	7	9	OPEN
GND	8	8	10	GND
CP	9	9	12	V_{CC}
Q_2	10	10	13	OPEN
$\overline{Q}_2$	11	11	14	OPEN
D_2	12	12	15	V_{CC}
D_3	13	13	17	V_{CC}
$\overline{Q}_3$	14	14	18	OPEN
Q_3	15	15	19	OPEN
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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FUNCTIONAL DESCRIPTION

The F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.
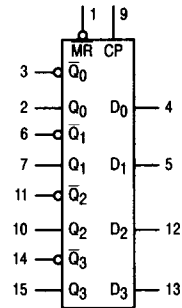
TRUTH TABLE

Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ $t_n + 1$	
D_n	Q_n	$\overline{Q_n}$
L	L	H
H	H	L

t_n = Bit time before clock pulse
$t_n + 1$ = Bit time after clock pulse
H = High Voltage Level
L = LOW Voltage Level

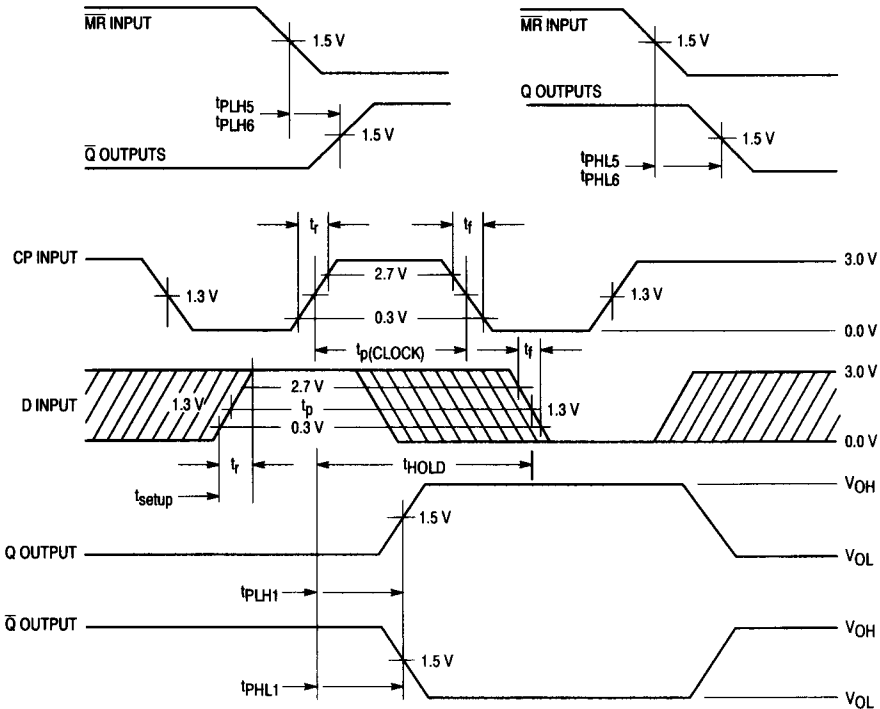### CONNECTION DIAGRAM
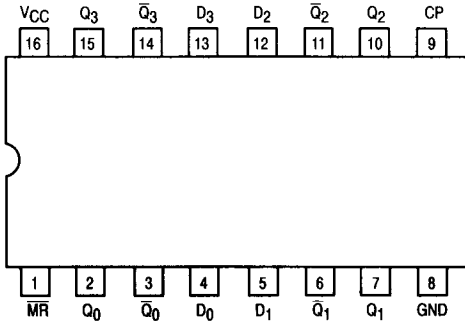
LOGIC SYMBOL

WAVEFORMS

The shaded areas indicate when the input is permitted to change for pedictable output performance.

54F175

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C Subgroup 1		+125°C Subgroup 2		−55°C Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	$V_{CC} = 4.5$ V, $I_{OH} = -1.0$ mA, $V_{IN} = 2.0$ V or 0.8 V per truth table.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA, $V_{IN} = 2.0$ V or 0.8 V per truth table.
V_{IC}	Input Clamping Voltage		−1.2					V	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	$V_{CC} = 5.5$ V, $V_{IH} = 2.7$ V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	$V_{CC} = 5.5$ V, $V_{IHH} = 7.0$ V, other inputs are open.
I_{IL}	Logical "0" Input Current ($\overline{MR}$, CP, D)	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	$V_{CC} = 5.5$ V, $V_{IL} = 0.5$ V, other inputs are open.
I_{OD}	Diode Current	60		60		60		mA	$V_{CC} = 4.5$ V, $\overline{MR} = 0$ V, $V_{IN} = 5.5$ V, other inputs are open, $V_{OUT} = 2.5$ V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	$V_{CC} = 5.5$ V, $V_{IN}(D) = 0$ V, other data inputs are open, $\overline{MR}$ & CR = (See Note 9), $V_{OUT} = 0$ V.
I_{CC}	Power Supply Current		34		34		34	mA	$V_{CC} = 5.5$ V, $V_{IN} = 4.5$ V, CP = (See Note 10), other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	$V_{CC} = 4.5$ V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	$V_{CC} = 4.5$ V.
t_s (H) t_s (L)	Set Up Time, D High or Low to CP	3.0		3.0		3.0		ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF. (Information only, No Testing Required).
t_h (H) t_h (L)	Hold Time, D High or Low to CP	1.0		1.0		1.0		ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF. (Information only, No Testing Required).
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0		5.0		5.0		ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF. (Information only, No Testing Required).
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with $V_{CC} = 4.5$ V, (**Repeat at**) $V_{CC} = 5.5$ V, $V_{INL} = 0.5$ V, and $V_{INH} = 2.5$ V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output Clock to Q_n	4.0	8.5	3.5	10.5	3.5	10.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.
t_{PLH1}	Propagation Delay /Data-Output Clock to Q_n	4.0	6.5	3.5	8.5	3.5	8.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.
t_{PHL2}	Propagation Delay /Data-Output Clock to $\overline{Q}_n$	4.0	8.5	3.5	10.5	3.5	10.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.
t_{PLH2}	Propagation Delay /Data-Output Clock to $\overline{Q}_n$	4.0	6.5	3.5	8.5	3.5	8.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.
t_{PHL5}	Propagation Delay /Data-Output $\overline{MR}$ to Q_n	4.5	11.5	4.5	15	4.5	15	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.
t_{PLH5}	Propagation Delay /Data-Output $\overline{MR}$ to Q_n	4.0	8.0	4.0	10	4.0	10	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.
t_{PHL6}	Propagation Delay /Data-Output $\overline{MR}$ to $\overline{Q}_n$	4.5	11.5	4.5	15	4.5	15	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.
t_{PLH6}	Propagation Delay /Data-Output $\overline{MR}$ to $\overline{Q}_n$	4.0	8.0	4.0	10	4.0	10	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.
f_{MAX}	Maximum Clock Frequency	100		80		80		MHz	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = 499$ Ω ± 5.0%.

NOTES:

1. Input pulse has the following characteristics:
   $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, or as specified in table 1, PRR (Subgroups 10 and 11) have a duty cycle 50 ± 15%, $t_p = 5.0$ ns (Min).
2. Inputs not under test are at GND, (see Note 8).
3. $C_L = 50$ pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = 499$ Ω ± 5.0%.
6. f_{MAX} minimum limit specified is the input pulse. The output frequency shall be 1/2 the input frequency.
7. Clock, Clear and Set inputs need to be in the proper configuration for specified output conditions.
8. Terminal conditions (pins not designated may be High ≥ 2.0 V, Low ≤ 0.8 V, or open).
9. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to $\overline{MR}$, then apply 3.0 V, 0 V, 3.0 V to CP, then make measurement.
10. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to CP, then make measurement.