REVISED DECEMBER 1983

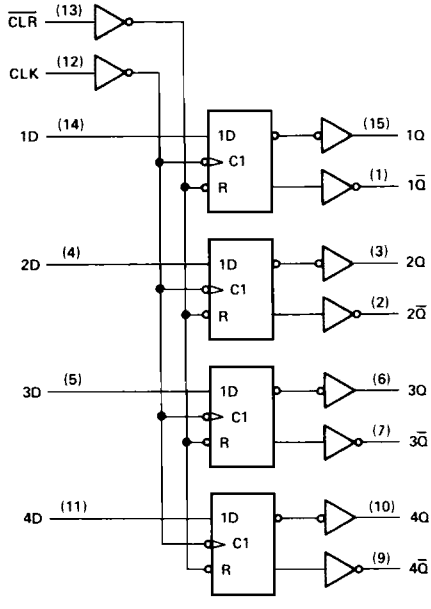
- **Contains Four Flip-Flops with Double Rail Outputs**
- **Buffered Clock and Clear Inputs**
- **Individual Data Inputs to Each Flip-Flop**

description

These monolithic, positive-edge triggered flip-flops utilize the latest low-power Schottky circuitry to implement D-type flip-flop logic. They have a direct clear input and complementary outputs from each flip-flop.

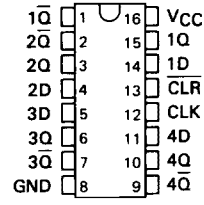
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

logic diagram

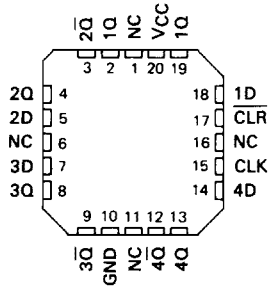


Pin numbers shown on logic notation are for D, J or N packages.

SN54LS171 . . . J OR W PACKAGE
SN74LS171 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS171 . . . FK PACKAGE
SN74LS171 . . . FN PACKAGE
(TOP VIEW)



NC-No internal connection

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLR	CLK	D	Q	Q̄
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

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TTL DEVICES

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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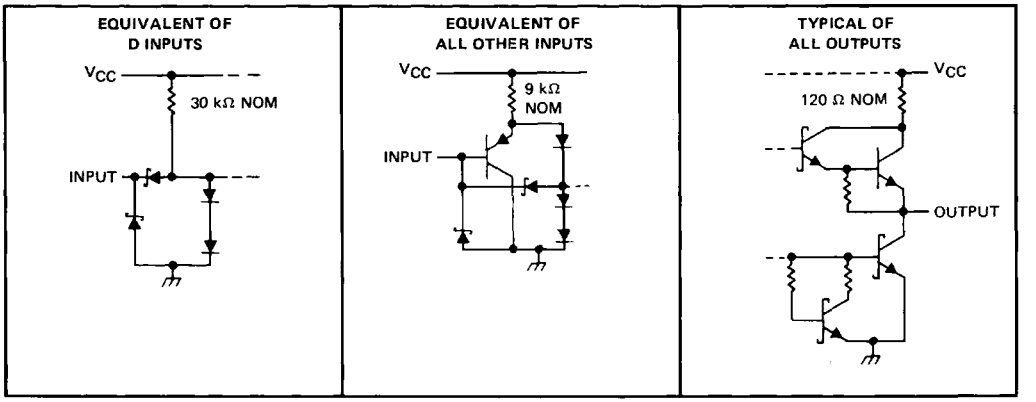
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS171 Circuits . . . . . −55°C to 125°C
SN74LS171 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS171			SN74LS171			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		20	0		20	MHz
t_w	Width of clock or clear pulse		20			20			ns
t_{su}	Setup time	Data input	20			20			ns
		Clear inactive-state	25			25			
t_h	Data hold time		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS171			SN74LS171			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA					0.35	0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	D inputs	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
		All others						−0.2			−0.2	mA
I_{OS}§	Short-circuit output current		V_{CC} = MAX,	V_O = 0 V		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 1			14	25		14	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS171			UNIT
				MIN	TYP	MAX	
f_{max}			R_L = 2 kΩ, C_L = 15 pF	20	30		MHz
t_{PLH}	CLK	Q, $\overline{Q}$			15	25	ns
t_{PHL}					18	30	ns
t_{PLH}	$\overline{CLR}$	Q			18	30	ns
t_{PHL}					24	40	ns

NOTE 2: See General Information Section for load circuits and voltage waveforms.