Synertek

SY2114A

1024 x 4 Static Random Access Memory

Features

- 100ns Maximum Access
- Low Operating Power Dissipation 0.05 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible: All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

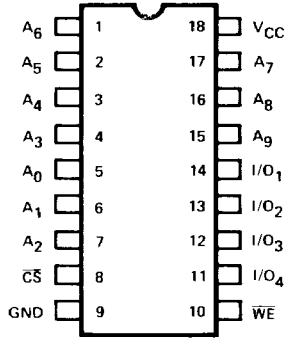
Description

The SY2114A is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 1 TTL load.

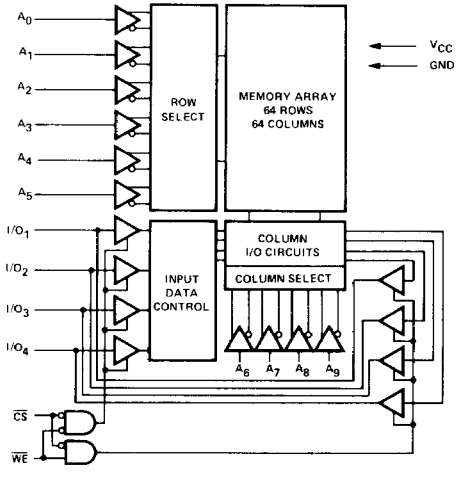
The SY2114A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The SY2114A is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology – a technology providing excellent performance characteristics as well as improved protection against contamination.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−3.5V to +7V
Power Dissipation	1.0W
Electrostatic Discharge Rating (ESD)** Inputs to Ground	±2000V

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**Test Condition: MIL-STD-883B Method 3015.1

D.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise Specified)

Symbol	Parameter	2114AL-1/ L-2/L-3/L-4 Min	2114AL-1/ L-2/L-3/L-4 Max	2114A-4 2114A-5 Min	2114A-4 2114A-5 Max	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10	μA	V_{IN} = 0 to 5.5V
I_{LO}	I/O Leakage Current		10		10	μA	$\overline{CS}$ = 2.0V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		35		65	mA	V_{CC} = 5.5V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current		40		70	mA	V_{CC} = 5.5V, $I_{I/O}$ = 0 mA T_A = 0°C
V_{IL}	Input Low Voltage	-3.0	0.8	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH} = -1.0 mA

Capacitance

T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
$C_{I/O}$	Input/Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

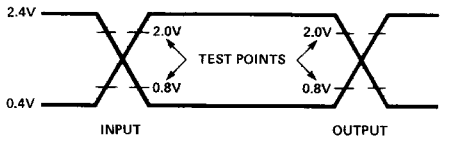
NOTE: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±10% (Unless otherwise Specified)

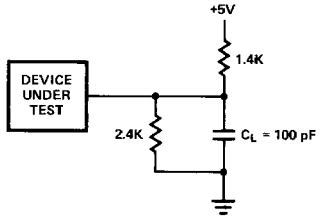
Symbol	Parameter	2114AL-1 Min	2114AL-1 Max	2114AL-2 Min	2114AL-2 Max	2114AL-3 Min	2114AL-3 Max	2114A-4/L-4 Min	2114A-4/L-4 Max	2114A-5 Min	2114A-5 Max	Unit
Read Cycle												
t_{RC}	Read Cycle Time	100		120		150		200		250		nsec
t_A	Access Time		100		120		150		200		250	nsec
t_{CO}	Chip Select to Output Valid		50		70		70		70		85	nsec
t_{CX}	Chip Select to Output Enabled	10		10		10		10		10		nsec
t_{OTD}	Chip Deselect to Output Off		30		35		40		50		60	nsec
t_{OHA}	Output Hold From Address Change	15		15		15		15		15		nsec
Write Cycle												
t_{WC}	Write Cycle Time	100		120		150		200		250		nsec
t_{AW}	Address to Write Setup Time	0		0		0		0		0		nsec
t_W	Write Pulse Width	50		75		90		120		135		nsec
t_{WR}	Write Release Time	0		0		0		0		0		nsec
t_{OTW}	Write to Output Off		30		35		40		50		60	nsec
t_{DW}	Data to Write Overlap	50		70		90		120		135		nsec
t_{DH}	Data Hold	0		0		0		0		0		nsec

A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

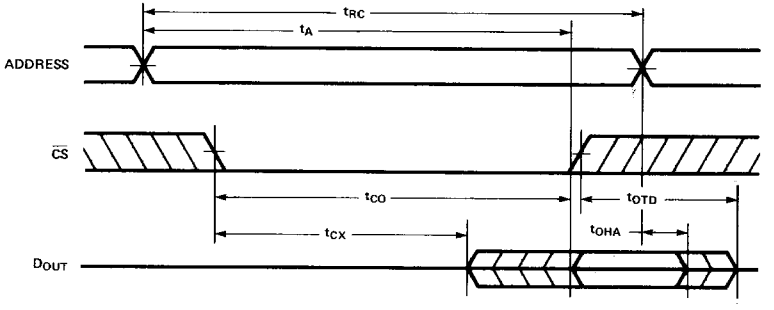
A.C. Testing Load Circuit



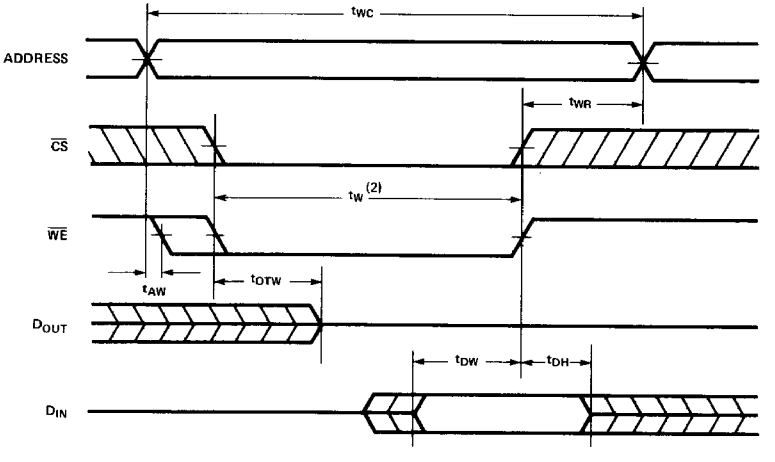
C_L INCLUDES JIG CAPACITANCE

Timing Diagrams

READ CYCLE (note 1)



WRITE CYCLE



NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
3. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Data Storage

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

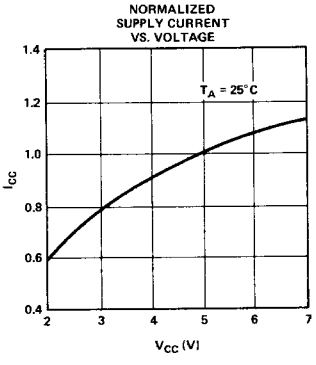
Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ or both can prevent extraneous writing due to

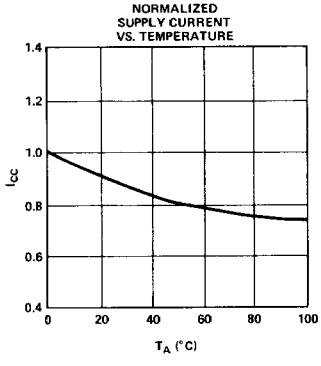
signal transitions.

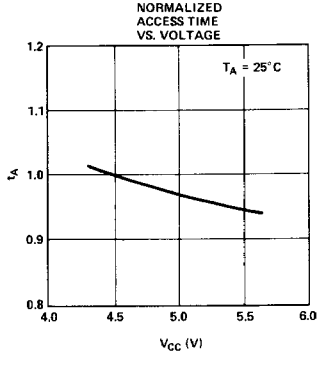
Data within the array can only be changed during Write time – defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus t_{WR}.

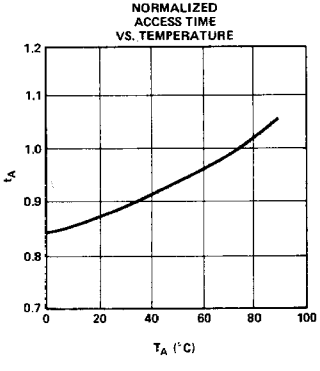
Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

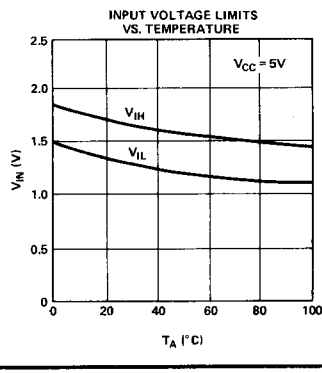
Typical Characteristics

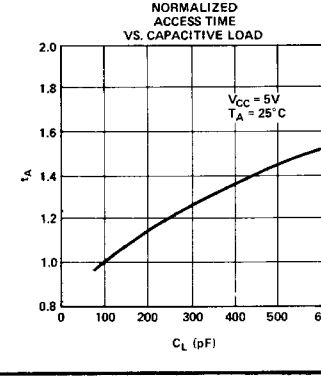












Package Availability

18 Pin Cerdip
18 Pin Plastic

Ordering Information

Order Number	Access Time (Max)	Supply Current (Max)	Package Type
SYD2114AL-1	100nsec	40mA	Cerdip
SYP2114AL-1	100nsec	40mA	Plastic
SYD2114AL-2	120nsec	40mA	Cerdip
SYP2114AL-2	120nsec	40mA	Plastic
SYD2114AL-3	150nsec	40mA	Cerdip
SYP2114AL-3	150nsec	40mA	Plastic
SYD2114AL-4	200nsec	40mA	Cerdip
SYP2114AL-4	200nsec	40mA	Plastic
SYD2114A-4	200nsec	70mA	Cerdip
SYP2114A-4	200nsec	70mA	Plastic
SYD2114A-5	250nsec	70mA	Cerdip
SYP2114A-5	250nsec	70mA	Plastic