

7.6A, 12ns, SOT23/TDFN, MOSFET Driver
General Description

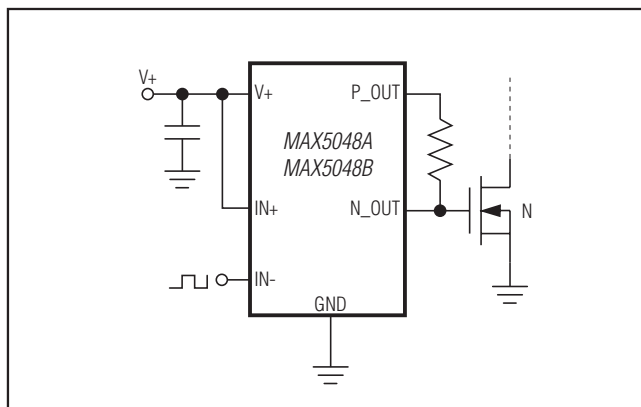
The MAX5048A/MAX5048B are high-speed MOSFET drivers capable of sinking/sourcing 7.6A/1.3A peak currents. These devices take logic input signals and drive a large external MOSFET. The MAX5048A/MAX5048B have inverting and noninverting inputs that give the user greater flexibility in controlling the MOSFET. They feature two separate outputs working in complementary mode, offering flexibility in controlling both turn-on and turn-off switching speeds.

The MAX5048A/MAX5048B have internal logic circuitry, which prevents shoot-through during output state changes. The logic inputs are protected against voltage spikes up to +14V, regardless of V+ voltage. Propagation delay time is minimized and matched between the inverting and noninverting inputs. The MAX5048A/MAX5048B have very fast switching times combined with very short propagation delays (12ns typ), making them ideal for high-frequency circuits.

The MAX5048A/MAX5048B operate from a +4V to +12.6V single power supply and typically consume 0.95mA of supply current. The MAX5048A has CMOS input logic levels, while the MAX5048B has standard TTL input logic levels. These devices are available in space-saving 6-pin SOT23 and TDFN packages.

Applications

Power MOSFET Switching
 Switch-Mode Power Supplies
 DC-DC Converters
 Motor Control
 Power-Supply Modules

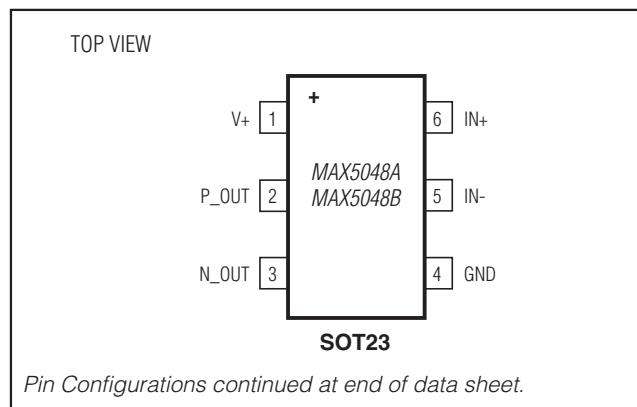
Typical Operating Circuit

Features

- ◆ Independent Source-and-Sink Outputs for Controllable Rise and Fall Times
- ◆ +4V to +12.6V Single Power Supply
- ◆ 7.6A/1.3A Peak Sink/Source Drive Current
- ◆ 0.23Ω Open-Drain n-Channel Sink Output
- ◆ 2Ω Open-Drain p-Channel Source Output
- ◆ 12ns (typ) Propagation Delay
- ◆ Matching Delay Time Between Inverting and Noninverting Inputs
- ◆ V_{CC}/2 CMOS (MAX5048A)/TTL (MAX5048B) Logic Inputs
- ◆ 1.6V Input Hysteresis
- ◆ Up to +14V Logic Inputs (Regardless of V+ Voltage)
- ◆ Low Input Capacitance: 2.5pF (typ)
- ◆ -40°C to +125°C Operating Temperature Range
- ◆ 6-Pin SOT23 and TDFN Packages

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	LOGIC INPUT	TOP MARK
MAX5048AAUT-T	-40°C to +125°C	6 SOT23	V _{CC} /2 CMOS	ABEC
MAX5048BAUT-T	-40°C to +125°C	6 SOT23	TTL	ABED
MAX5048AATT-T	-40°C to +125°C	6 TDFN-EP*	V _{CC} /2 CMOS	AKV
MAX5048BATT-T	-40°C to +125°C	6 TDFN-EP*	TTL	AKW

Ordering Information continued at end of data sheet.

Pin Configurations


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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND

V+	-0.3V to +13V	6-Pin TDFN (derate 18.2mW/°C above +70°C)	1454mW
IN+, IN-	-0.3V to +14V	Operating Temperature Range	-40°C to +125°C
N_OUT, P_OUT	-0.3V to (V+ + 0.3V)	Storage Temperature Range	-65°C to +150°C
N_OUT Continuous Output Current (Note 1)	390mA	Junction Temperature	+150°C
P_OUT Continuous Output Current (Note 1)	100mA	Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation* (T _A = +70°C)		Soldering Temperature (reflow)	+260°C
6-Pin SOT23 (derate 9.1mW/°C above +70°C)	727mW		

Note 1: Continuous output current is limited by the power dissipation of the package.

*As per JEDEC51 standard.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

SOT23

Junction-to-Case Thermal Resistance (θ_{JC}).....75°C/W

TDFN

Junction-to-Case Thermal Resistance (θ_{JC}).....8.5°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

(V₊ = +12V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
V+ Operating Range	V+			4.0		12.6	V
V+ Undervoltage Lockout	UVLO	V+ rising		3.25	3.6	4.00	V
V+ Undervoltage Lockout Hysteresis					400		mV
V+ Undervoltage Lockout to Output Delay Time		V+ rising			300		ns
V+ Supply Current	I+	IN+ = IN- = V+			0.95	1.5	mA
n-CHANNEL OUTPUT							
Driver Output Resistance— Pulling Down (MAX5048AAUT/ MAX5048BAUT)	R _{ON-N}	V _{V+} = +10V, I _{N-OUT} = -100mA	T _A = +25°C		0.23	0.26	Ω
			T _A = +125°C		0.38	0.43	
		V _{V+} = +4.5V, I _{N-OUT} = -100mA	T _A = +25°C		0.24	0.28	
			T _A = +125°C		0.40	0.47	
Driver Output Resistance— Pulling Down (MAX5048AATT/ MAX5048BATT)	R _{ON-N}	V _{V+} = +10V, I _{N-OUT} = -100mA	T _A = +25°C		0.31	0.34	Ω
			T _A = +125°C		0.46	0.51	
		V _{V+} = +4.5V, I _{N-OUT} = -100mA	T _A = +25°C		0.32	0.36	
			T _A = +125°C		0.48	0.55	

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ELECTRICAL CHARACTERISTICS (continued)

(V+ = +12V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Off Pulldown Resistance		V+ = 0 or unconnected, I _{N-OUT} = -10mA, T _A = +25°C		3.3	10	Ω
Power-Off Pulldown Clamp Voltage		V+ = 0 or unconnected, I _{N-OUT} = -10mA, T _A = +25°C		0.85	1.0	V
Output Leakage Current	I _{LK-N}	N_OUT = V+		6.85	20	μA
Peak Output Current (Sinking)	I _{PK-N}	C _L = 10,000pF		7.6		A
p-CHANNEL OUTPUT						
Driver Output Resistance— Pulling Up (MAX5048AAUT/ MAX5048BAUT)	R _{ON-P}	V _{V+} = +10V, I _{P-OUT} = 50mA	T _A = +25°C	2.00	3.00	Ω
			T _A = +125°C	2.85	4.30	
		V _{V+} = +4.5V, I _{P-OUT} = 50mA	T _A = +25°C	2.20	3.30	
			T _A = +125°C	3.10	4.70	
Driver Output Resistance— Pulling Up (MAX5048AATT/ MAX5048BATT)	R _{ON-P}	V _{V+} = +10V, I _{P-OUT} = 50mA	T _A = +25°C	2.08	3.08	Ω
			T _A = +125°C	2.93	4.38	
		V _{V+} = +4.5V, I _{P-OUT} = 50mA	T _A = +25°C	2.28	3.38	
			T _A = +125°C	3.18	4.78	
Output Leakage Current	I _{LK-P}	P_OUT = 0		0.001	10	μA
Peak Output Current (Sourcing)	I _{PK-P}	C _L = 10,000pF		1.3		A
LOGIC INPUT						
Logic 1 Input Voltage	V _{IH}	MAX5048A	0.67 x V+			V
		MAX5048B	2.4			
Logic 0 Input Voltage	V _{IL}	MAX5048A	0.33 x V+			V
		MAX5048B	0.8			
Logic-Input Hysteresis	V _{HYS}	MAX5048A	1.6			V
		MAX5048B	0.68			
Logic-Input Current		V _{IN_} = V+ or 0		0.001	10	μA
Input Capacitance	C _{IN}			2.5		pF
SWITCHING CHARACTERISTICS FOR V+ = +10V						
Rise Time	t _R	C _L = 1000pF	8			ns
		C _L = 5000pF	45			
		C _L = 10,000pF	82			
Fall Time	t _F	C _L = 1000pF	3.2			ns
		C _L = 5000pF	7.5			
		C _L = 10,000pF	12.5			
Turn-On Propagation Delay Time	t _{D-ON}	Figure 1, C _L = 1000pF (Note 4)	7	12	25	ns
Turn-Off Propagation Delay Time	t _{D-OFF}	Figure 1, C _L = 1000pF (Note 4)	7	12	25	ns
Break-Before-Make Time				2.5		ns

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ELECTRICAL CHARACTERISTICS (continued)

(V+ = +12V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

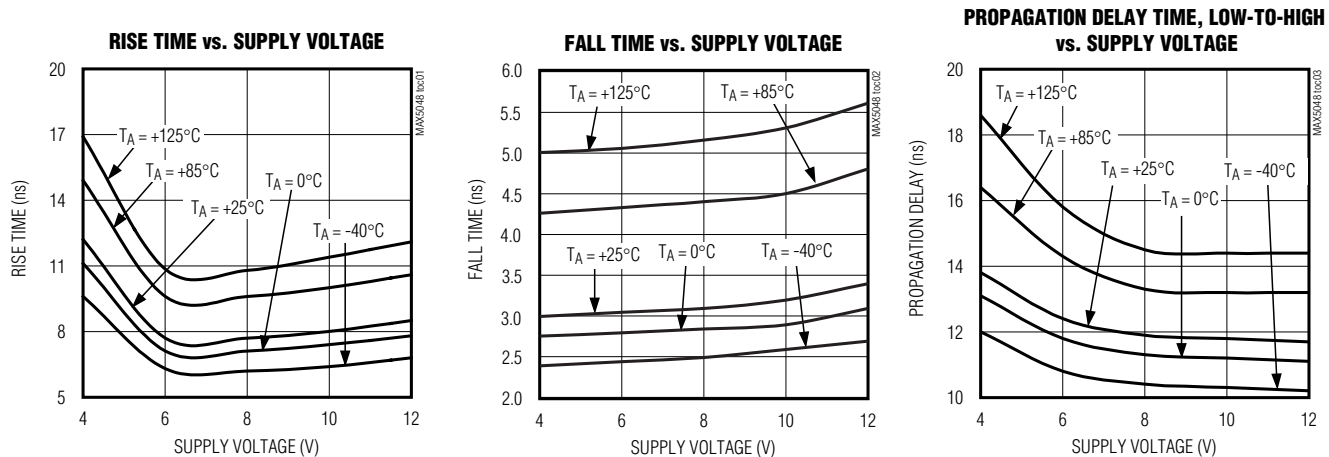
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS FOR V+ = +4.5V						
Rise Time	t _R	C _L = 1000pF		12		ns
		C _L = 5000pF		41		
		C _L = 10,000pF		74		
Fall Time	t _F	C _L = 1000pF		3.0		ns
		C _L = 5000pF		7.0		
		C _L = 10,000pF		11.3		
Turn-On Propagation Delay Time	t _{D-ON}	Figure 1, C _L = 1000pF (Note 4)	8	14	27	ns
Turn-Off Propagation Delay Time	t _{D-OFF}	Figure 1, C _L = 1000pF (Note 4)	8	14	27	ns
Break-Before-Make Time				4.2		ns

Note 3: All DC specifications are 100% tested at T_A = +25°C. Specifications over -40°C to +125°C are guaranteed by design.

Note 4: Guaranteed by design, not production tested.

Typical Operating Characteristics

(C_L = 1000pF, T_A = +25°C, unless otherwise noted.)



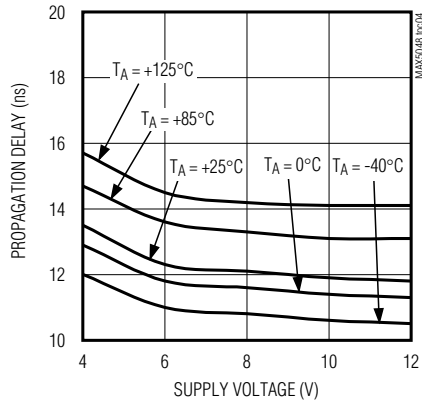
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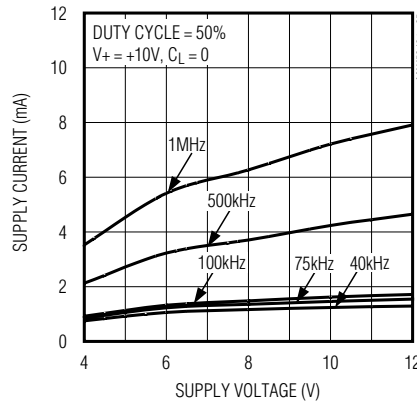
Typical Operating Characteristics (continued)

($C_L = 1000\text{pF}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

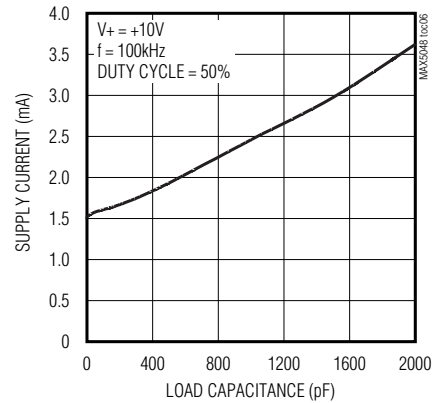
PROPAGATION DELAY TIME, HIGH-TO-LOW vs. SUPPLY VOLTAGE



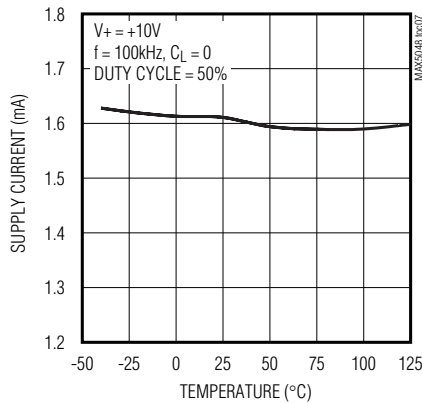
SUPPLY CURRENT vs. SUPPLY VOLTAGE



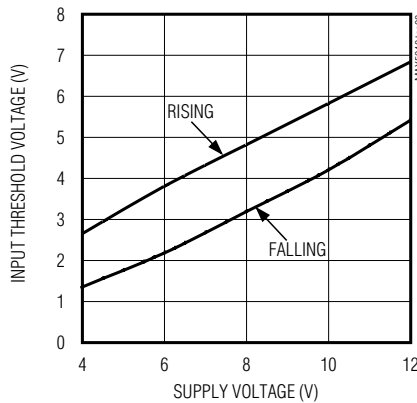
SUPPLY CURRENT vs. LOAD CAPACITANCE



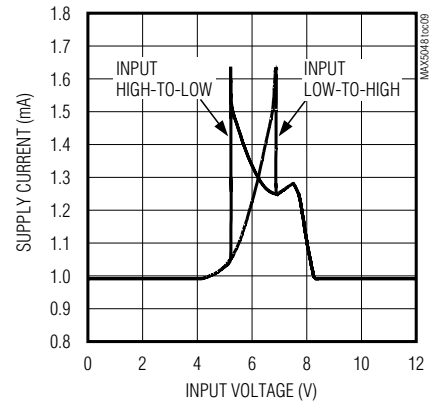
SUPPLY CURRENT vs. TEMPERATURE



MAX5048A INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



MAX5048A SUPPLY CURRENT vs. INPUT VOLTAGE



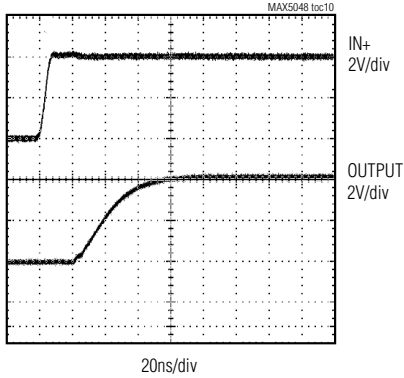
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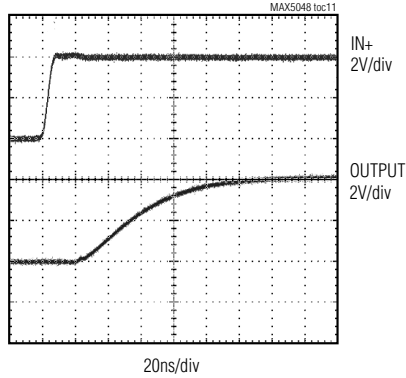
Typical Operating Characteristics (continued)

($C_L = 1000\text{pF}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

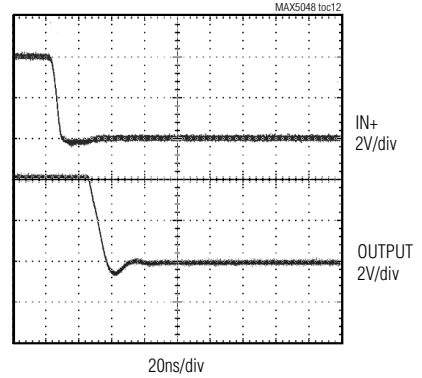
INPUT VOLTAGE vs. OUTPUT VOLTAGE
($V_+ = +4\text{V}$, $C_L = 5000\text{pF}$)



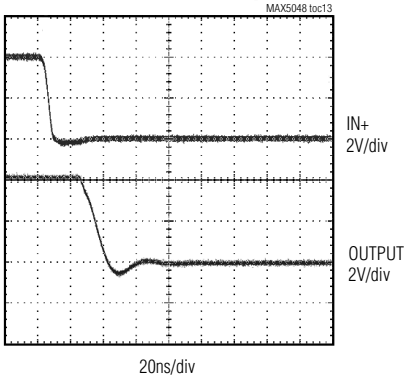
INPUT VOLTAGE vs. OUTPUT VOLTAGE
($V_+ = +4\text{V}$, $C_L = 10,000\text{pF}$)



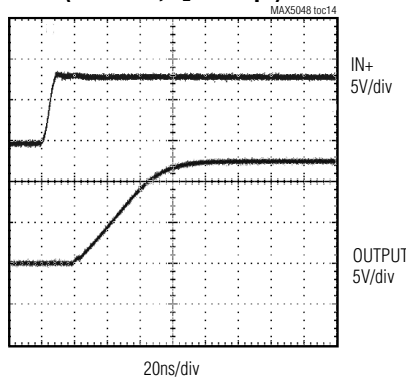
INPUT VOLTAGE vs. OUTPUT VOLTAGE
($V_+ = +4\text{V}$, $C_L = 5000\text{pF}$)



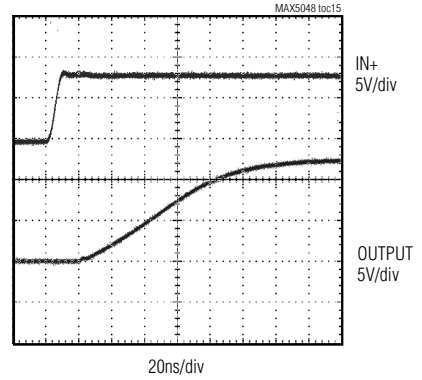
INPUT VOLTAGE vs. OUTPUT VOLTAGE
($V_+ = +4\text{V}$, $C_L = 10,000\text{pF}$)



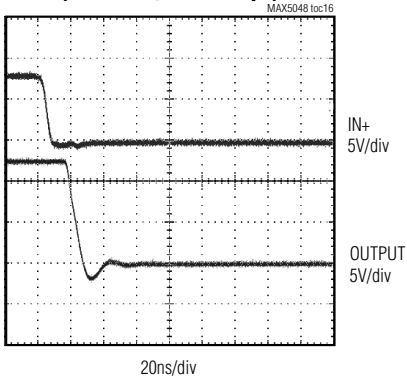
INPUT VOLTAGE vs. OUTPUT VOLTAGE
($V_+ = +12\text{V}$, $C_L = 5000\text{pF}$)



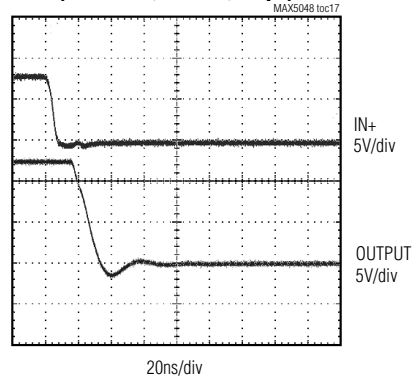
INPUT VOLTAGE vs. OUTPUT VOLTAGE
($V_+ = +12\text{V}$, $C_L = 10,000\text{pF}$)



INPUT VOLTAGE vs. OUTPUT VOLTAGE
($V_+ = +12\text{V}$, $C_L = 5000\text{pF}$)



INPUT VOLTAGE vs. OUTPUT VOLTAGE
($V_+ = +12\text{V}$, $C_L = 10,000\text{pF}$)



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Pin Description

PIN	NAME	FUNCTION
1	V+	Power Supply. Bypass to GND with a 0.1µF ceramic capacitor.
2	P_OUT	p-Channel Open-Drain Output. Sources current for MOSFET turn-on.
3	N_OUT	n-Channel Open-Drain Output. Sinks current for MOSFET turn-off.
4	GND	Ground
5	IN-	Inverting Logic Input Terminal. Connect to GND when not used.
6	IN+	Noninverting Logic Input Terminal. Connect to V+ when not used.
—	EP	Exposed paddle. Connect to GND. Solder EP to the GND plane for improved thermal performance.

Detailed Description

Logic Inputs

The MAX5048A/MAX5048Bs' logic inputs are protected against voltage spikes up to +14V, regardless of the V+ voltage. The low 2.5pF input capacitance of the inputs reduces loading and increases switching speed. These devices have two inputs that give the user greater flexibility in controlling the MOSFET. Table 1 shows all possible input combinations.

The difference between the MAX5048A and the MAX5048B is the input threshold voltage. The MAX5048A has $V_{CC}/2$ CMOS logic-level thresholds, while the MAX5048B has TTL logic-level thresholds (see the *Electrical Characteristics*). For V+ above 5.5V, V_{IH} (typ) = $0.5x(V+) + 0.8V$ and V_{IL} (typ) = $0.5x(V+) - 0.8V$. As V+ is reduced from 5.5V to 4V, V_{IH} and V_{IL} gradually approach V_{IH} (typ) = $0.5x(V+) + 0.65V$ and V_{IL} (typ) = $0.5x(V+) - 0.65V$. Connect IN+ to V+ or IN- to GND when not used. Alternatively, the unused input can be used as an ON/OFF pin (see Table 1).

Table 1. Truth Table

IN+	IN-	p-CHANNEL	n-CHANNEL
L	L	OFF	ON
L	H	OFF	ON
H	L	ON	OFF
H	H	OFF	ON

L = Logic low

H = Logic high

Undervoltage Lockout (UVLO)

When V+ is below the UVLO threshold, the N-channel is ON and the P-channel is OFF, independent of the state of the inputs. The UVLO is typically 3.6V with 400mV typical hysteresis to avoid chattering.

Driver Outputs

The MAX5048A/MAX5048B provide two separate outputs. One is an open-drain P-channel, the other an open-drain N-channel. They have distinct current sourcing/sinking capabilities to independently control the rise and fall times of the MOSFET gate. Add a resistor in series with P_OUT/N_OUT to slow the corresponding rise/fall time of the MOSFET gate.

Applications Information

Supply Bypassing, Device Grounding, and Placement

Ample supply bypassing and device grounding are extremely important because when large external capacitive loads are driven, the peak current at the V+ pin can approach 1.3A, while at the GND pin the peak current can approach 7.6A. V_{CC} drops and ground shifts are forms of negative feedback for inverters and, if excessive, can cause multiple switching when the IN-input is used and the input slew rate is low. The device driving the input should be referenced to the MAX5048A/MAX5048B GND pin especially when the IN-input is used. Ground shifts due to insufficient device grounding may disturb other circuits sharing the same AC ground return path. Any series inductance in the V+, P_OUT, N_OUT and/or GND paths can cause oscillations due to the very high di/dt that results when the MAX5048A/MAX5048B are switched with any capacitive load. A 0.1µF or larger value ceramic capacitor is recommended bypassing V+ to GND and placed as close to the pins as possible. When driving very large loads (e.g., 10nF) at minimum rise time, 10µF or more of parallel storage capacitance is recommended. A ground plane is highly recommended to minimize ground return resistance and series inductance. Care should be taken to place the MAX5048A/MAX5048B as close as possible to the external MOSFET being driven to further minimize board inductance and AC path resistance.

Power Dissipation

Power dissipation of the MAX5048A/MAX5048B consists of three components, caused by the quiescent current, capacitive charge and discharge of internal nodes, and the output current (either capacitive or resistive load). The sum of these components must be kept below the maximum power-dissipation limit.

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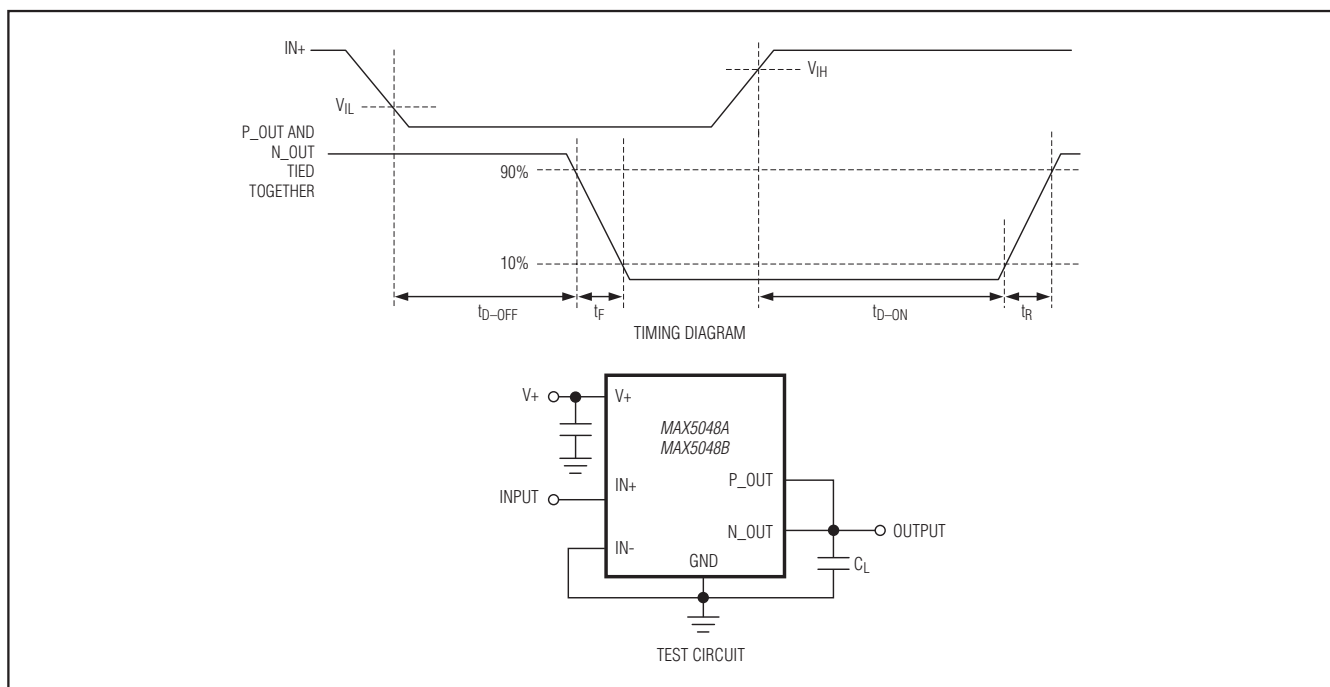


Figure 1. Timing Diagram and Test Circuit

The quiescent current is 0.95mA typical. The current required to charge and discharge the internal nodes is frequency dependent (see the *Typical Operating Characteristics*). The MAX5048A/MAX5048B power dissipation when driving a ground referenced resistive load is:

$$P = D \times R_{ON(MAX)} \times I_{LOAD}^2$$

where D is the fraction of the period the MAX5048A/MAX5048Bs' output pulls high, $R_{ON(MAX)}$ is the maximum on-resistance of the device with the output high (P-channel), and I_{LOAD} is the output load current of the MAX5048A/MAX5048B.

For capacitive loads, the power dissipation is:

$$P = C_{LOAD} \times (V_+)^2 \times FREQ$$

where C_{LOAD} is the capacitive load, V_+ is the supply voltage, and FREQ is the switching frequency.

Layout Information

The MOSFET drivers MAX5048A/MAX5048B source-and-sink large currents to create very fast rise and fall edges at the gate of the switching MOSFET. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PCB layout guidelines are recommended when designing with the MAX5048A/MAX5048B:

- Place one or more 0.1 μ F decoupling ceramic capacitor(s) from V_+ to GND as close to the device as possible. At least one storage capacitor of 10 μ F (min) should be located on the PC board with a low resistance path to the V_+ pin of the MAX5048A/MAX5048B.
- There are two AC current loops formed between the device and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from N_OUT of the MAX5048A/MAX5048B to the MOSFET gate to the MOSFET source and to GND of the MAX5048A/MAX5048B. When the gate of the MOSFET is being pulled high, the active current loop is from P_OUT of the MAX5048A/MAX5048B to the MOSFET gate to the MOSFET source to the GND terminal of the decoupling capacitor to the V_+ terminal of the MAX5048A/MAX5048B. While the charging current loop is important, the discharging current loop is critical. It is important to minimize the physical distance and the impedance in these AC current paths.
- In a multilayer PCB, the component surface layer surrounding the MAX5048A/MAX5048B should consist of a GND plane containing the discharging and charging current loops.

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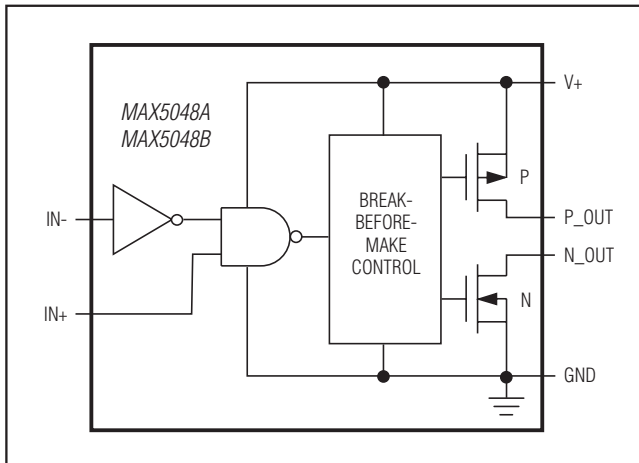


Figure 2. MAX5048A/MAX5048B Functional Diagram

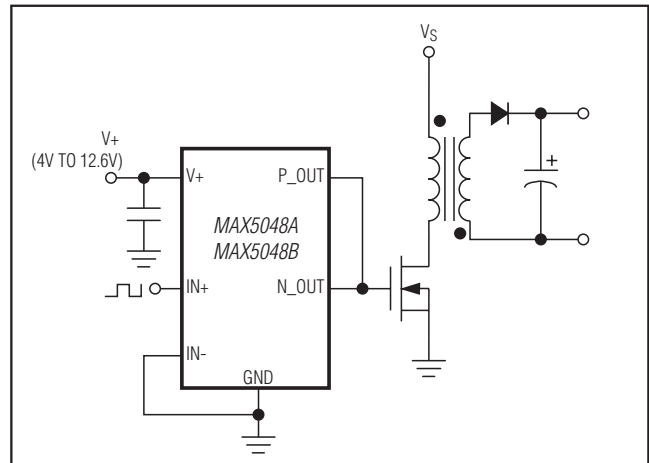


Figure 3. Noninverting Application

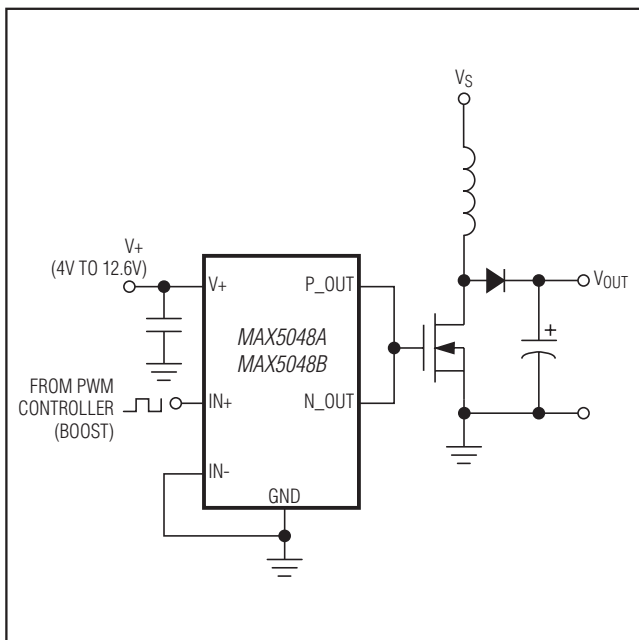


Figure 4. Boost Converter

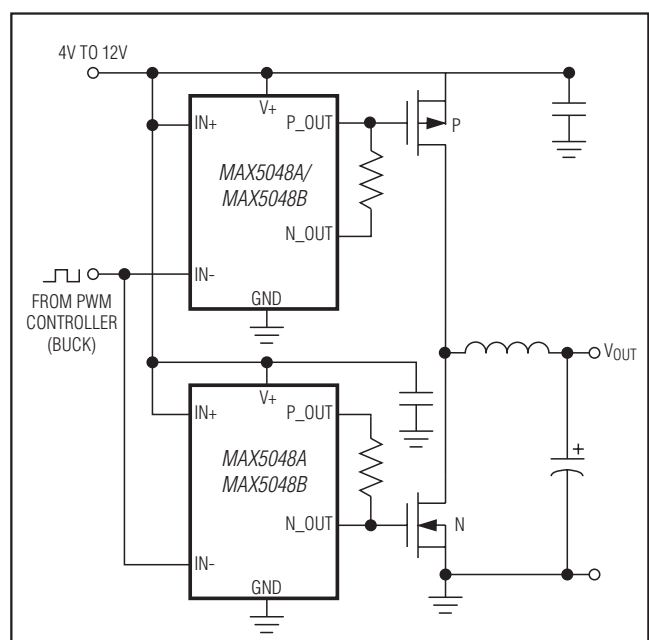
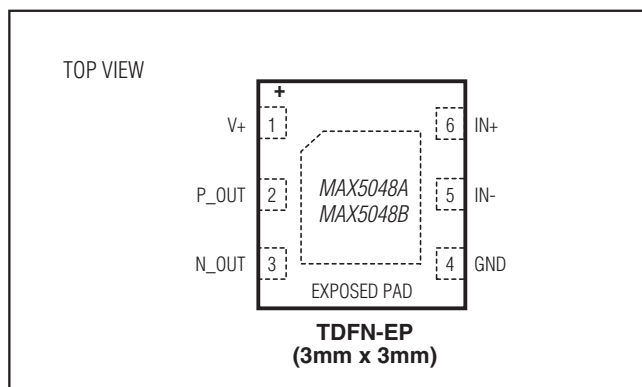


Figure 5. MAX5048A/MAX5048B in High-Power Synchronous Buck Converter

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Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	LOGIC INPUT	TOP MARK
MAX5048AAUT+T	-40°C to +125°C	6 SOT23	V _{CC} /2 CMOS	ABEC
MAX5048BAUT+T	-40°C to +125°C	6 SOT23	TTL	ABED
MAX5048AATT+T	-40°C to +125°C	6 TDFN-EP*	V _{CC} /2 CMOS	AKV
MAX5048BATT+T	-40°C to +125°C	6 TDFN-EP*	TTL	AKW

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

*EP = Exposed pad.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 SOT23	U6F+6	21-0058	90-0175
6 TDFN	—	21-0137	90-0058

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	11/12	Added "+" lead(Pb)-free/RoHS-compliant designations to <i>Ordering Information</i>	1, 9



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