National Semiconductor

74LVX3L384A
10-Bit Low Power Extended Input Voltage Bus Switch

General Description

The LVX3L384A provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ($\overline{BE}$) signals. When $\overline{BE}$ is low, the switch is on and port A is connected to port B. When $\overline{BE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The 74LVX3L384A 10-bit bus switch is pin-for-pin and function compatible with the 74LVX3L384 device. It has the added feature of allowing extended negative input voltages on the I/O pins. The 74LVX3L384A bus switch, unlike most bus switches on the market, will not falsely turn on when $\overline{BE}$ is high and negative undershoot voltages are encountered on the I/O pins. Thus it is "undershoot hardened" (see related application note) tolerating undershoots up to −1.5V.

Typical applications include IDE bus connector interfaces, PCI card interfaces, backplane card interfaces, and other noisy environments where switches are needed.

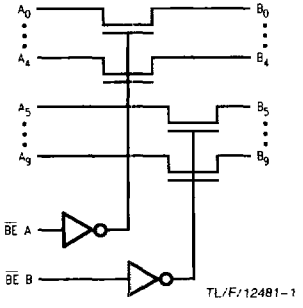
Features

- Extended input voltage design tolerates input undershoots up to −1.5V
- 10Ω switch connection between two ports
- Ultra low power with 2 μA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC, QSOP and TSSOP

Truth Table

$\overline{BE}$ A	$\overline{BE}$ B	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

Logic Diagram



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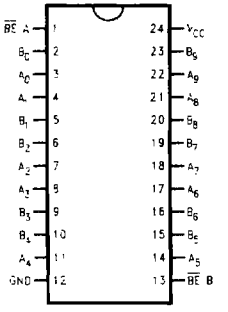
Pin Names	Description
$\overline{BE}$ A, $\overline{BE}$ B	Bus Switch Enable
A_0–A_9	Bus A
B_0–B_9	Bus B

Connection Diagram

Pin Assignment for SOIC, QSOP and TSSOP



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	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVX3L384AWM 74LVX3L384AWMX	74LVX3L384AQSC 74LVX3L384AQSCX	74LVX3L384AMTC 74LVX3L384AMTCX
See NS Package Number	M24B	MQA24	MTC24

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5 to +7.0V
DC Input Input Voltage (V_I) (Note 2)	−0.5 to +7.0V
DC Input Diode Current with (V_I < 0)	−20 mA
DC Output (I_O) Sink Current	120 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation	0.5W

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.0V to 5.5V
Free Air Operating Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVX3L384A T_A = −40°C to +85°C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Maximum Clamp Diode Voltage	4.75			−1.2	V	I_{IN} = −18 mA
V_{IH}	Minimum High Level Input Voltage	4.75–5.25	2.0			V	
V_{IL}	Maximum Low Level Input Voltage	4.75–5.25			0.8	V	
I_{IN}	Maximum Input Leakage Current	0			10	μA	0 ≤ V_{IN} ≤ 5.25V
		5.25			±1	μA	
I_{OZ}	Maximum TRI-STATE® I/O Leakage	5.25			±10	μA	0 ≤ A, B ≤ V_{CC}
I_{OS}	Short Circuit Current	4.75	100			mA	V_I(A), V_I(B) = 0V, V_I(B), V_I(A) = 4.75V
R_{ON}	Switch On Resistance (Note 3)	4.75		6	12	Ω	V_I = 0V, I_{ON} = 30 mA
				15	25	Ω	V_I = 2.4V, I_{ON} = 15 mA
I_{CC}	Maximum Quiescent Supply Current	5.25		0.2	10	μA	V_I = V_{CC}, GND I_O = 0
ΔI_{CC}	Increase in I_{CC} per Input (Note 4)	5.25			2.5	mA	V_{IN} = 3.15V, I_O = 0 Per Control Input

Note 3: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 4: Per TTL driven Input (V_{IN} = 3.15V, control inputs only). A and B pins do not contribute to I_{CC}.

Note 5: All typical values are at V_{CC} = 5.0V, T_A = 25°C.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX3L384A $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
			Min	Typ (Note 5)	Max	
T_{PLH} T_{PHL}	Data Propagation Delay An to Bn or Bn to An (Note 6)	4.75			0.50	ns
T_{PZL} T_{PZH}	Switch Enable Time $\overline{BE}_A$, $\overline{BE}_B$ to An, Bn	4.75	1.5		6.8	ns
T_{PLZ} T_{PHZ}	Switch Disable Time $\overline{BE}_A$, $\overline{BE}_B$ to An, Bn	4.75	1.5		6.0	ns

Note 5: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

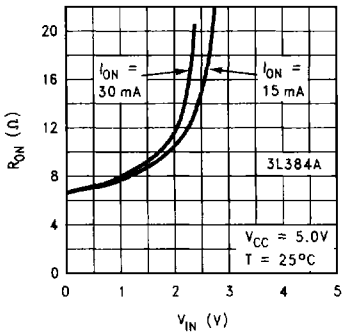
Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.5 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Capacitance (Note)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	4	6	pF	$V_{CC} = 5.0V$
$C_{I/O}$ (OFF)	Input/Output Capacitance	9	13	pF	$V_{CC} = 5.0V$

Note: Capacitance is characterized but not tested.

74LVX3L384A V_{IN} vs R_{ON} (Typ)



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