



Series 54H/74H

Series DM54H/DM74H

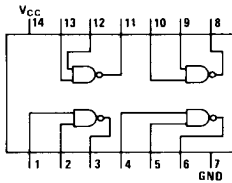
Series DM54H/DM74H

general description

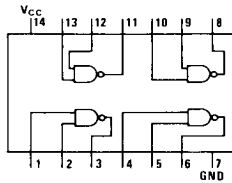
The Series 54H/74H extends the breadth of the Series 54/74 Family by adding a product line which is approximately twice as fast as the basic series. The products are completely miscible

within a system; and it is generally considered good engineering to optimize a design by utilizing the Series 54H/74H only where needed for higher speed.

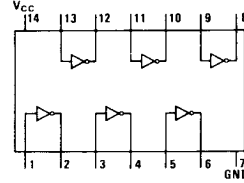
connection diagrams Dual-In-Line Package Only (Con't on Page 2-6)



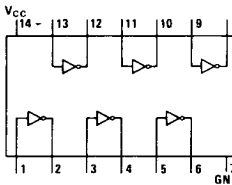
DM54H00/DM74H00
quad 2-input NAND gate



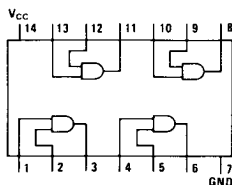
DM54H01/DM74H01
quad 2-input NAND gate
(open collector)



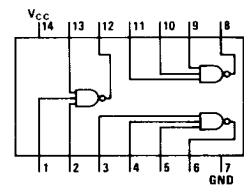
DM54H04/DM74H04
hex inverter



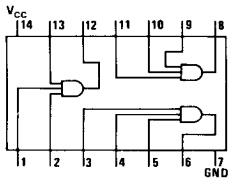
DM54H05/DM74H05
hex inverter
(open collector)



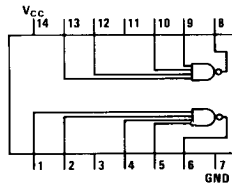
DM54H08/DM74H08
quad 2-input AND gate



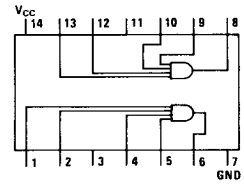
DM54H10/DM74H10
triple 3-input NAND gate



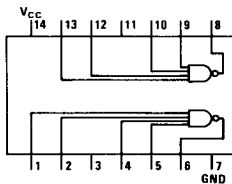
DM54H11/DM74H11
triple 3-input AND gate



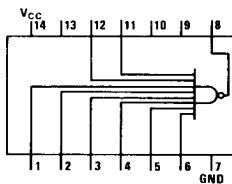
DM54H20/DM74H20
dual 4-input NAND gate



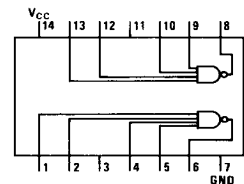
DM54H21/DM74H21
dual 4-input AND gate



DM54H22/DM74H22
dual 4-input NAND gate
(open collector)



DM54H30/DM74H30
8-input NAND gate



DM54H40/DM74H40
dual 4-input NAND buffer

2

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
Series 54H	-55°C to +125°C
Series 74H	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM54HXX	4.5	5.5	V
DM74HXX	4.75	5.25	V
Temperature			
DM54HXX	-55	125	°C
DM74HXX	0	70	°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	$V_{CC} = 5.0V, T_A = 25^\circ C, I_{IN} = -12 mA$			-1.5	V
Logical "1" Input Voltage	$V_{CC} = \text{Min}$	2.0			V
Logical "0" Input Voltage	$V_{CC} = \text{Min}$			0.8	V
Logical "1" Output Voltage					
All Devices, Except DM54H40/DM74H40 and Open Collector Circuits	$V_{CC} = \text{Min}, I_O = -500 \mu A, V_{IN} = 2.0V \text{ or } 0.8V$	2.4			V
DM54H40/DM74H40	$V_{CC} = \text{Min}, I_O = -1.5 mA, V_{IN} = 2.0V \text{ or } 0.8V$	2.4			V
Logical "0" Output Voltage					
All Devices, Except DM54H40/DM74H40	$V_{CC} = \text{Min}, I_O = 20 mA, V_{IN} = 2.0V \text{ or } 0.8V$			0.4	V
DM54H40/DM74H40	$V_{CC} = \text{Min}, I_O = 60 mA, V_{IN} = 2.0V \text{ or } 0.8V$			0.4	V
Logical "1" Output Current					
All Open Collector Circuits	$V_{CC} = \text{Min}, V_{OUT} = 5.5V, V_{IN} = 2.0V \text{ or } 0.8V$			250	μA
Except DM54H60, DM54H62	@ -55°C			320	μA
DM74H60, DM74H62	@ 0°C			570	μA
DM54H61, DM74H61	$V_{OUT} = 2.2V$			50	μA
Logical "0" Input Current	$V_{CC} = \text{Max}, V_{IN} = 0.4V$			-2.0	mA
Logical "1" Input Current	$V_{CC} = \text{Max}, V_{IN} = 2.4V$			50	μA
	$V_{CC} = \text{Max}$			1.0	mA
Output Short Circuit Current (Note 1)					
All Circuits Except DM54H40/DM74H40	$V_{CC} = \text{Max}, V_{OUT} = 0V$	-40		-100	mA
and Open Collector Circuits					
DM54H40/DM74H40	$V_{OUT} = 0V$	-40		-125	mA
Supply Current	$V_{CC} = \text{Max}$				
DM54H00/DM74H00			26	40	mA
Logical "0"			10	16.8	mA
Logical "1"					
DM54H01/DM74H01			26	40	mA
Logical "0"			6.8	10	mA
Logical "1"					
DM54H04/DM74H04			40	58	mA
Logical "0"			16	26	mA
Logical "1"					
DM54H05/DM74H05			40	58	mA
Logical "0"			16	26	mA
Logical "1"					
DM54H08/DM74H08			42	64	mA
Logical "0"			28	40	mA
Logical "1"					
DM54H10/DM74H10			19.5	30	mA
Logical "0"			7.5	12.6	mA
Logical "1"					
DM54H20/DM74H20			13	20	mA
Logical "0"			5.0	8.4	mA
Logical "1"					
DM54H21/DM74H21			20	32	mA
Logical "0"			12	20	mA
Logical "1"					
DM54H22/DM74H22			13	20	mA
Logical "0"			3.4	5.0	mA
Logical "1"					

Note 1: Not more than one output shorted at a time, duration of short-circuit test not to exceed 1 second, and all typical values are at $V_{CC} = 5V, T_A = 25^\circ C$.

electrical characteristics (con't)						
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
DM54H30/DM74H30 Logical "0" Logical "1"			6.5	10	mA	
			2.5	4.2	mA	
DM54H40/DM74H40 Logical "0" Logical "1"			25	40	mA	
			10.4	16	mA	
DM54H50/DM74H50 DM54H51/DM74H51 Logical "0" Logical "1"			15.2	24	mA	
			8.2	12.8	mA	
DM54H52/DM74H52 Logical "0" Logical "1"			15.2	24	mA	
			20	31	mA	
DM54H53/DM74H53 DM54H54/DM74H54 Logical "0" Logical "1"			9.4	14	mA	
			7.1	11	mA	
DM54H55/DM74H55 Logical "0" Logical "1"			7.5	12	mA	
			4.5	6.4	mA	
DM54H60/DM74H60 On Level Current Off Level Current			1.9	3.5	mA	
			3.0	4.5	mA	
DM54H61/DM74H61 On Level Current Off Level Current			11	16	mA	
			5.0	7.0	mA	
DM54H62/DM74H62 On Level Current Off Level Current			3.8	7.0	mA	
			6.0	9.0	mA	
DM54H71/DM74H71			19	30	mA	
DM54H72/DM74H72			16	25	mA	
DM54H73/DM74H73			32	50	mA	
DM54H74/DM74H74			30	50	mA	
DM54H76/DM74H76			32	50	mA	
DM54H78/DM74H78			32	50	mA	
switching characteristics $T_A = 25^\circ\text{C}$; $V_{CC} = 5\text{V}$; $N = 10$; $C = 25\text{ pF}$; $R_L = 280\Omega$						
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
DM54H00/DM74H00 t_{pd0} t_{pd1}			6.2	10	ns	
			5.9	10	ns	
DM54H01/DM74H01 t_{pd0} t_{pd1}			7.5	12	ns	
			10	15	ns	
DM54H04/DM74H04 t_{pd0} t_{pd1}			6.5	10	ns	
			6.0	10	ns	
DM54H05/DM74H05 t_{pd0} t_{pd1}			7.5	12	ns	
			10	15	ns	
DM54H08/DM74H08 t_{pd0} t_{pd1}			8.8	12	ns	
			7.6	12	ns	

switching characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DM54H10/DM74H10			6.3	10	ns
t_{pd0}			5.9	10	ns
t_{pd1}					
DM54H11/DM74H11			8.8	12	ns
t_{pd0}			7.6	12	ns
t_{pd1}					
DM54H20/DM74H20			7.0	10	ns
t_{pd0}			6.0	10	ns
t_{pd1}					
DM54H21/DM74H21			8.8	12	ns
t_{pd0}			7.6	12	ns
t_{pd1}					
DM54H22/DM74H22			7.5	12	ns
t_{pd0}			10	15	ns
t_{pd1}					
DM54H30/DM74H30			8.9	12	ns
t_{pd0}			6.8	10	ns
t_{pd1}					
DM54H40/DM74H40			6.5	12	ns
t_{pd0}			8.5	12	ns
t_{pd1}					
DM54H50/DM74H50			6.2	11	ns
t_{pd0}			6.8	11	ns
t_{pd1}					
DM54H51/DM74H51			6.2	11	ns
t_{pd0}			6.8	11	ns
t_{pd1}					
DM54H52/DM74H52			9.2	15	ns
t_{pd0}			10.6	15	ns
t_{pd1}					
DM54H53/DM74H53			6.2	11	ns
t_{pd0}			7.0	11	ns
t_{pd1}					
DM54H54/DM74H54			6.2	11	ns
t_{pd0}			7.0	11	ns
t_{pd1}					
DM54H55/DM74H55			6.5	11	ns
t_{pd0}			7.0	11	ns
t_{pd1}					
DM54H60/DM74H60 (Thru Expandable Gates)			7.4		ns
t_{pd0}			11.4		ns
t_{pd1}					
DM54H61/DM74H61 (Thru Expandable Gates)			9.8		ns
t_{pd0}			14.8		ns
t_{pd1}					
DM54H62/DM74H62 (Thru Expandable Gates)			7.4		ns
t_{pd0}			11.4		ns
t_{pd1}					
DM54H71/DM74H71			22	27	ns
$t_{pd0}(CLOCK)$			14	21	ns
$t_{pd1}(CLOCK)$			12	24	ns
$t_{pd0}(PRESET)$			6.0	13	ns
$t_{pd1}(PRESET)$					

switching characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Clock Frequency		25	30		ns
DM54H72/DM74H72					
DM54H73/DM74H73					
DM54H76/DM74H76					
DM54H78/DM74H78					
t _{pd0} (CLOCK)			22	27	ns
t _{pd1} (CLOCK)			14	21	ns
t _{pd0} (CLEAR,PRESET)			12	24	ns
t _{pd1} (CLEAR,PRESET)			6.0	13	ns
Maximum Clock Frequency		25	30		ns
DM54H74/DM74H74					
t _{pd0} (CLOCK)			13	20	ns
t _{pd1} (CLOCK)			8.5	15	ns
t _{pd0} (CLEAR,PRESET)				30	ns
t _{pd1} (CLEAR,PRESET)				20	ns
Maximum Clock Frequency		35	43		ns

loading table

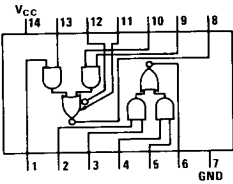
DEVICES	WEIGHTED LOADS
DM54H00/DM74H00	1
DM54H01/DM74H01	1
DM54H04/DM74H04	1
DM54H05/DM74H05	1
DM54H08/DM74H08	1
DM54H10/DM74H10	1
DM54H11/DM74H11	1
DM54H20/DM74H20	1
DM54H21/DM74H21	1
DM54H22/DM74H22	1
DM54H30/DM74H30	1
DM54H40/DM74H40	2
DM54H50/DM74H50	1
DM54H51/DM74H51	1
DM54H52/DM74H52	1
DM54H53/DM74H53	1
DM54H54/DM74H54	1
DM54H55/DM74H55	1
DM54H60/DM74H60	1
DM54H61/DM74H61	1
DM54H62/DM74H62	1
DM54H71/DM74H71	1
All Inputs Except	
Preset and Clock	1
Preset	3
Clock	2
DM54H72/DM74H72	
All Inputs Except	
Preset and Clear	1
Preset, Clear	2
DM54H73/DM74H73	
J, K, and Clock	1
Clear	2
DM54H74/DM74H74	
D	1
Preset and Clock	2
Clear	3
DM54H76/DM74H76	
J, K, and Clock	1
Preset and Clear	2
DM54H78/DM74H78	
J and K	1
Preset and Clock	2
Clear	4

1 Load = 50 μA @ 2.4V Logical "1" Input Current
 = 2 mA @ 0.4V Logical "0" Input Current

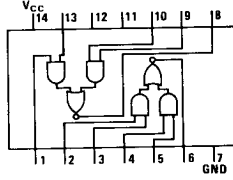
(All inputs are guaranteed 1 mA @ 5.5V for Logical "1" breakdown test)

2

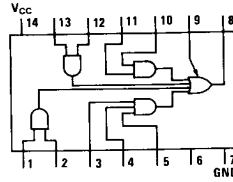
connection diagrams (con't)



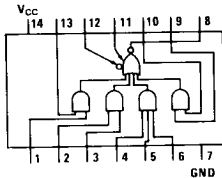
DM54H50/DM74H50
expandable dual 2-wide
2-input AND-OR-INVERT gate



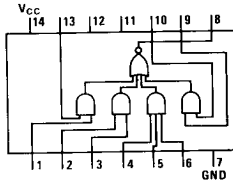
DM54H51/DM74H51
dual 2-wide 2-input
AND-OR-INVERT gate



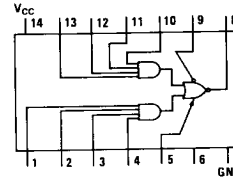
DM54H52/DM74H52
expandable 2-2-2-3-input
AND-OR gate



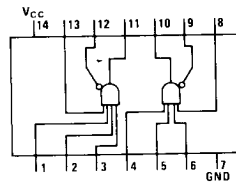
DM54H53/DM74H53
expandable 2-2-2-3-input
AND-OR-INVERT gate



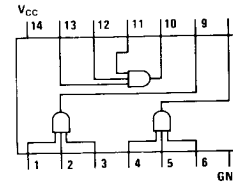
DM54H54/DM74H54
4-wide 2-input
AND-OR-INVERT gate



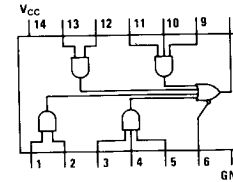
DM54H55/DM74H55
expandable 2-wide 4-input
AND-OR-INVERT gate



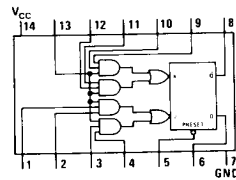
DM54H60/DM74H60
dual 4-input expander



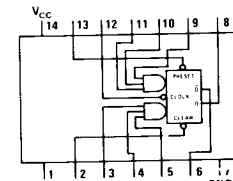
DM54H61/DM74H61
triple 3-input expander



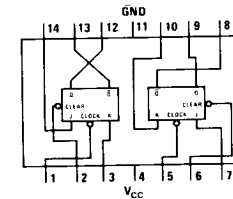
DM54H62/DM74H62
3-2-2-3-input expander



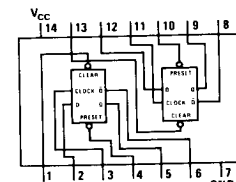
DM54H71/DM74H71
J-K flip flop with AND-OR inputs



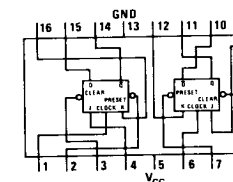
DM54H72/DM74H72
J-K master-slave flip flop



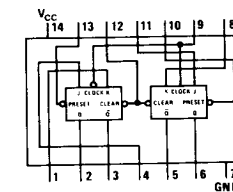
DM54H73/DM74H73
dual J-K flip flop with
separate clocks



DM54H74/DM74H74
dual D edge-triggered flip flop

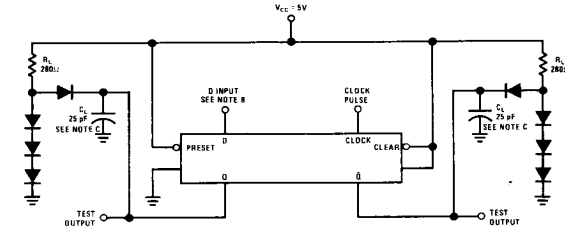


DM54H76/DM74H76
dual J-K master-slave flip flop



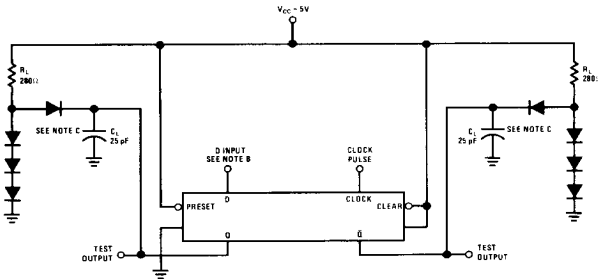
DM54H78/DM74H78
dual J-K flip flop with preset
and clear inputs

ac test circuits



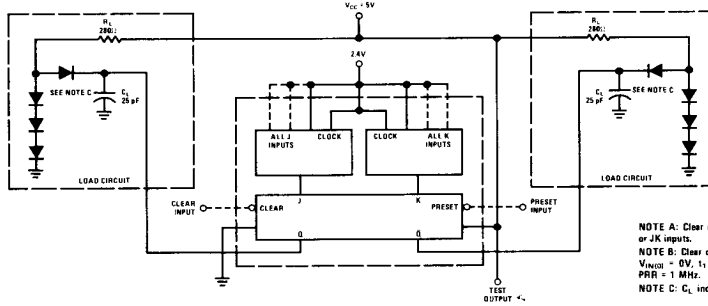
Switching Characteristics, Clock and Synchronous Inputs
(High Level Data)

NOTE A: Clock input pulse has the following characteristics: $t_{w(CLOCK)} = 20$ ns, PRR = 1 MHz.
NOTE B: D input (pulse A) has the following characteristics: $t_{setup} = 10$ ns, $t_w = 60$ ns, PRR is 50% of clock PRR. D input (pulse B) has the following characteristics: $t_{hold} = 0$ ns, $t_w = 60$ ns, PRR is 50% of clock PRR.
NOTE C: C_L includes probe and jig capacitance.



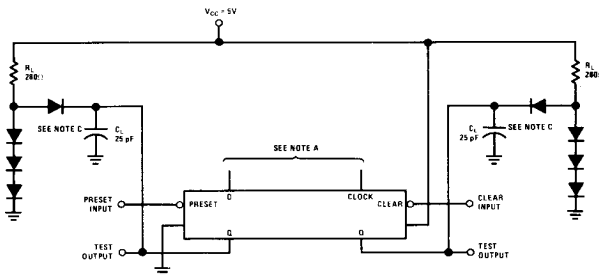
Switching Characteristics, Clock and Synchronous Inputs
(Low-Level Data)

NOTE A: Clock input pulse has the following characteristics: $t_w = 20$ ns, PRR = 1 MHz.
NOTE B: D input (pulse A) has the following characteristics: $t_{setup} = 15$ ns, $t_w = 60$ ns, PRR = 1 MHz and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $t_{hold} = 0$ ns, $t_w = 60$ ns, and PRR is 50% of clock PRR.
NOTE C: C_L includes probe and jig capacitance.



Flip Flop Preset/Clear Propagation Delay Times

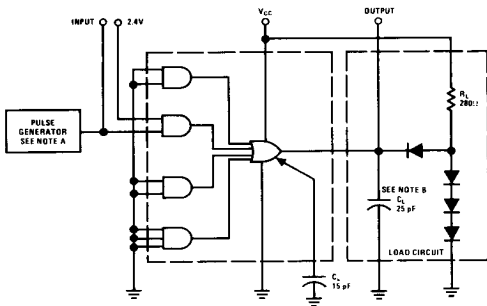
NOTE A: Clear or Preset inputs are dominate regardless of clock or JK inputs.
NOTE B: Clear or Preset input pulse characteristics: $V_{in(1)} = 3V$, $V_{in(0)} = 0V$, $t_1 = t_0 = 7$ ns, $t_{w(CLEAR)} = t_{w(PRESET)} = 16$ ns, PRR = 1 MHz.
NOTE C: C_L includes jig capacitance.



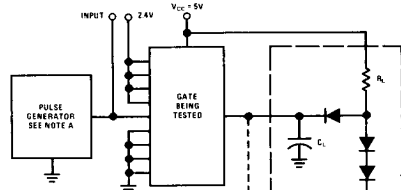
Asynchronous Inputs Switching Characteristics

NOTE A: Clear and Preset input dominates clock or D inputs.
NOTE B: Clear or Preset input pulse characteristics: $t_{w(CLEAR)} = t_{w(PRESET)} = 25$ ns, PRR = 1 MHz.
NOTE C: C_L includes probe and jig capacitance.

ac test circuits (con't)



NOTE A: $V_{IN(1)} = 3V$, $V_{IN(2)} = 0V$, $t_0 = t_1 = 7 ns$, duty cycle = 50%, PRR = 1 MHz, $Z_{OUT} = 50\Omega$.
 NOTE B: C_L includes jig capacitance.
 NOTE C: C_L includes jig capacitance.



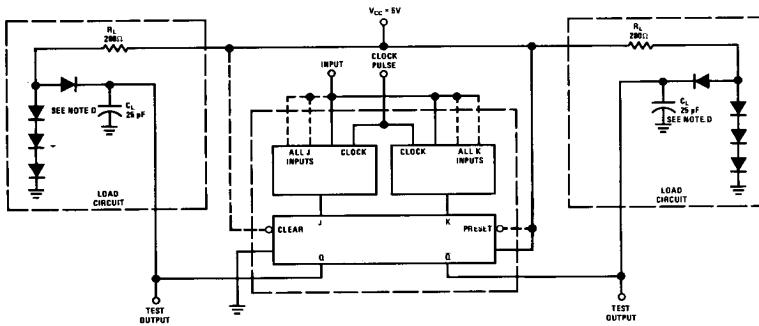
NOTE A: The pulse generator has the following characteristics: $V_{IN(1)} = 3V$, $V_{IN(2)} = 0V$, $t_1 = t_0 = 7 ns$, PRR = 1 MHz, duty cycle = 50%, and $Z_{OUT} = 50\Omega$.
 NOTE B: Input conditions are established for each gate as follows:

- (1) Input pulse is applied to one input and 2.4V is applied to all unused inputs of the DM54H00/DM74H00, DM54H01/DM74H01, DM54H04/DM74H04, DM54H05/DM74H05, DM54H10/DM74H10, DM54H11/DM74H11, DM54H20/DM74H20, DM54H21/DM74H21, DM54H22/DM74H22, DM54H30/DM74H30, or DM54H40/DM74H40 gate.
- (2) Input pulse is applied to one input of one AND section, and 2.4V is applied to all unused inputs of that AND section of the DM54H50/DM74H50, DM54H51/DM74H51, DM54H52/DM74H52, DM54H53/DM74H53, DM54H54/DM74H54, or DM54H55/DM74H55 gate. All inputs of all unused AND sections are grounded.

NOTE C: All gates are inverting except the DM54H11/DM74H11, DM54H21/DM74H21, and DM54H52/DM74H52 only.
 NOTE D: C_L includes probe and jig capacitance.

DM54H52/DM74H52

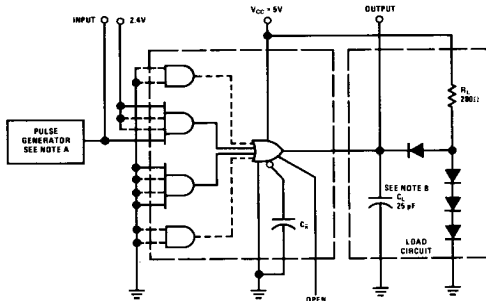
DM54H52/DM74H52 Loading For Gates



NOTE A: When testing t_{QD} and t_{Q1} (all types), the clock input pulse characteristics are: $V_{IN(1)} = 3V$, $V_{IN(2)} = 0V$, $t_1 = t_0 = 7 ns$, $t_{CLOCK1} = 20 ns$, and PRR = 1 MHz.
 NOTE B: All J and K inputs are at 2.4V.
 NOTE C: When testing t_{CLOCK} , the clock input characteristics are: $V_{IN(1)} = 3V$, $V_{IN(2)} = 0V$, $t_1 = t_0 = 3 ns$, $t_{CLOCK1} = 10 ns$, PRR = 40 MHz. All J and K inputs are at 2.4V.
 NOTE D: C_L includes probe and jig capacitance.

Flip Flop Propagation Delay Times

truth tables



NOTE A: $V_{IN(1)} = 3V$, $V_{IN(2)} = 0V$, $t_0 = t_1 = 7 ns$, duty cycle = 50%, PRR = 1 MHz.
 NOTE B: C_L includes probe and jig capacitance.
 NOTE C: C_L includes jig capacitance.

DM54H50, DM54H53, DM54H55

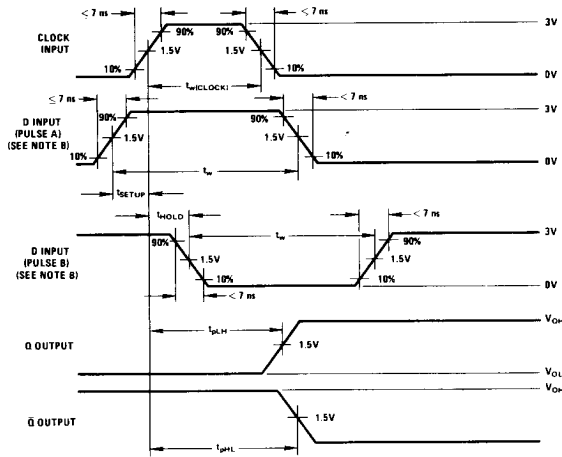
t_n	t_{n+1}
J	K
0	0
0	1
1	0
1	1

all J-K flip flops

t_n	t_{n+1}
D	Q
0	0
1	1

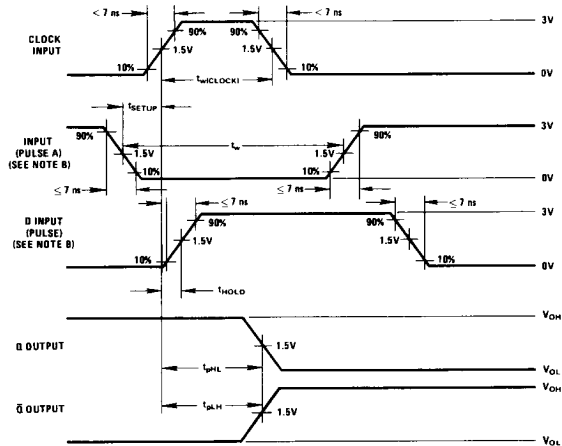
DM74H74 only

switching time waveforms



NOTE A: Clock input pulse has the following characteristics: t_{CLOCK} = 20 ns, PRR = 1 MHz.
 NOTE B: D input (pulse A) has the following characteristics: t_{SETUP} = 10 ns, t_{H} = 60 ns, PRR is 50% of clock PRR. D input (pulse B) has the following characteristics: t_{HOLD} = 0 ns, t_{H} = 60 ns, PRR is 50% of clock PRR.
 NOTE C: C_L includes probe and jig capacitance.

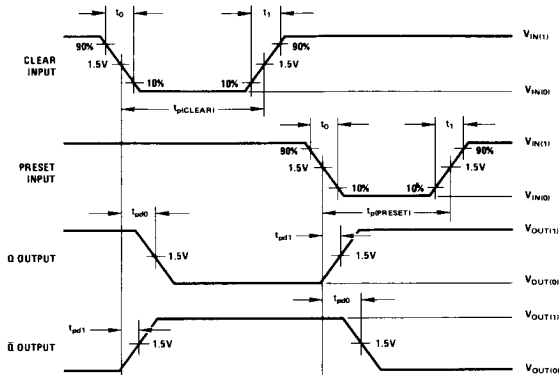
Switching Characteristics, Clock and Synchronous Inputs
(High Level Data)



NOTE A: Clock input pulse has the following characteristics: t_{C} = 20 ns, PRR = 1 MHz.
 NOTE B: D input (pulse A) has the following characteristics: t_{SETUP} = 15 ns, t_{H} = 60 ns, PRR = 1 MHz and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{HOLD} = 0 ns, t_{H} = 60 ns, and PRR is 50% of clock PRR.
 NOTE C: C_L includes probe and jig capacitance.

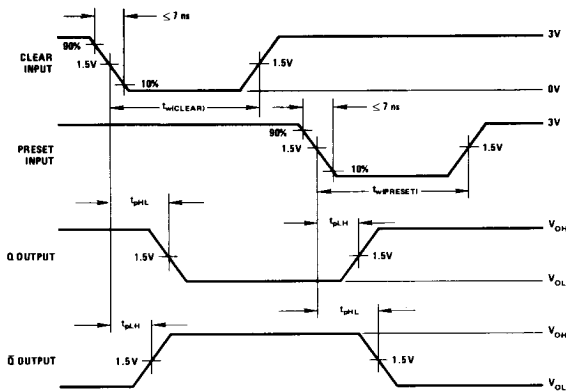
Switching Characteristics, Clock and Synchronous Inputs
(Low Level Data)

switching time waveforms (con't)



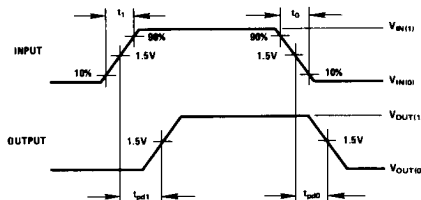
NOTE A: Clear or Preset inputs are dominate regardless of clock or JK inputs.
 NOTE B: Clear or Preset input pulse characteristic: $V_{IN(1)} = 3V$, $V_{IN(0)} = 0V$, $t_0 = t_1 = 7 ns$, $t_{P(CLEAR)} = t_{P(PRESET)} = 16 ns$, PRR = 1 MHz.
 NOTE C: C_L includes jig capacitance.

Flip Flop Preset/Clear Propagation Delay Times



NOTE A: Clear and Preset input dominates clock or D inputs.
 NOTE B: Clear or Preset impulse characteristic: $t_{P(CLEAR)} = t_{P(PRESET)} = 25 ns$, PRR = 1 MHz.
 NOTE C: C_L includes probe and jig capacitance.

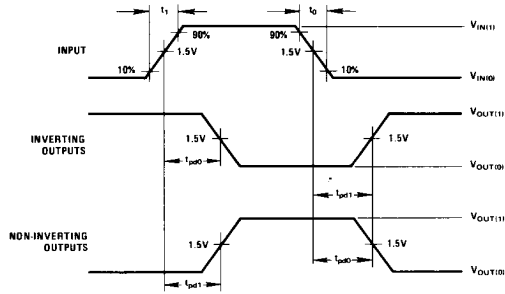
Asynchronous Inputs Switching Characteristics



NOTE A: $V_{IN(1)} = 3V$, $V_{IN(0)} = 0V$, $t_0 = t_1 = 7 ns$, duty cycle = 50%, PRR = 1 MHz, $Z_{OUT} = 50\Omega$.
 NOTE B: C_L includes jig capacitance.
 NOTE C: C_L includes jig capacitance.

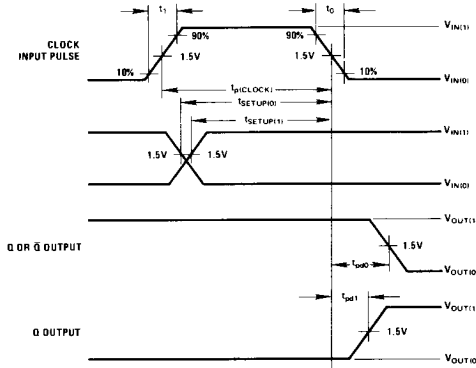
DM54H52/DM74H52

switching time waveforms (con't)



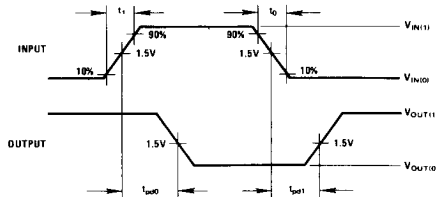
NOTE A: $V_{IN(1)} = 3V$, $V_{IN(0)} = 0V$, $t_1 = t_0 = 7 ns$, PRR = 1 MHz, duty cycle = 50%, $Z_{OUT} \approx 50\Omega$.
 NOTE B: C_L includes probe and jig capacitance, $R_L = 280\Omega$ on all gates except DM54H40 where $R_L = 93\Omega$.
 NOTE C: $C_L = 25 pF$ on all devices.
 NOTE D: $C_L = 1.3 pF$ typical for expanders.

DM54H52/DM74H52 Propagation Delays



NOTE A: When testing t_{pD0} and t_{pD1} (all types), the clock input pulse characteristics are: $V_{IN(1)} = 3V$, $V_{IN(0)} = 0V$, $t_1 = t_0 = 7 ns$, $f_{CLOCK} = 20 ns$, and PRR = 1 MHz.
 NOTE B: All J and K inputs are at 2.4V.
 NOTE C: When testing f_{CLOCK} , the clock input characteristics are: $V_{IN(0)} = 3V$, $V_{IN(0)} = 0V$, $t_1 = t_0 = 3 ns$, $f_{CLOCK} = 10 ns$, PRR = 40 MHz. All J and K inputs are at 2.4V.
 NOTE D: C_L includes probe and jig capacitance.

Flip Flop Propagation Delay Times



NOTE A: $V_{IN(1)} = 3V$, $V_{IN(0)} = 0V$, $t_0 = t_1 = 7 ns$, duty cycle = 50%, PRR = 1 MHz.
 NOTE B: C_L includes probe and jig capacitance.
 NOTE C: C_L includes jig capacitance.

DM54H50, DM54H53, DM54H55