M5M5408AFP,TP,RT-70L-I,-70LL-I, -10L-I,-10LL-I

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408A is 4,194,304-bit CMOS static RAM organized as 524,288-words by 8-bit, fabricated using high-performance quadruple-polysilicon and double metal CMOS technology.
The use of thin film transistor (TFT) load cells and CMOS periphery results in a high density and low power static RAM. The M5M5408A is designed for memory applications where the high performance, high reliability, large storage, simple interfacing and battery back-up are important design objectives.

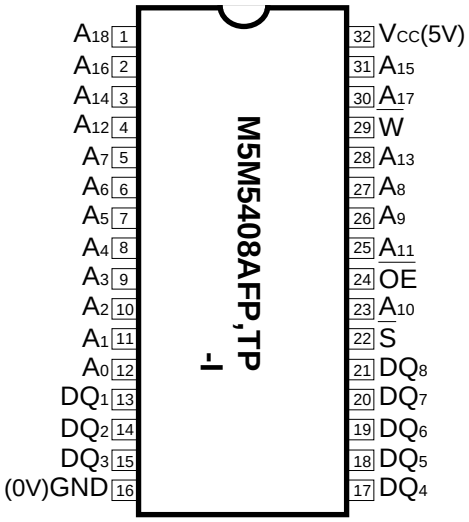
The M5M5408A is offered in a 32-pin plastic small outline package (SOP) and a 32-pin thin small outline package (TSOP), providing high board level packing densities. Two types of TSOP packages are available, M5M5408ATP(normal lead bend type package) and M5M5408ART (reverse lead bend type package). Using both two types makes it easy to design a printed circuit board.

FEATURES

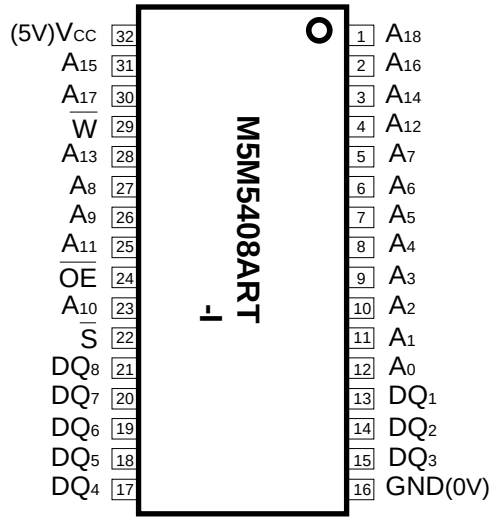
Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5408AFP,TP,RT-70L-I M5M5408AFP,TP,RT-10L-I	70ns 100ns	90mA (Vcc=5.5V)	200µA (Vcc=5.5v)
M5M5408AFP,TP,RT-70LL-I M5M5408AFP,TP,RT-10LL-I	70ns 100ns		40µA (Vcc=5.5v)

- Single +5V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion and power down by $\overline{S}$
- Data retention supply voltage=+2.0V
- Three-state outputs: OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common Data I/O
- Small stand-by current……0.4µA(typ.)
- Package
  - M5M5408AFP : 32 pin 525 mil SOP
  - M5M5408ATP : 32 pin 400 mil TSOP(II)
  - M5M5408ART : 32 pin 400 mil TSOP(II)

PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A(FP)
32P3Y-H(TP)



Outline 32P3Y-J(RT)

APPLICATION

Small capacity memory units, IC card, Battery operating system, asynchronous server system

M5M5408AFP,TP,RT-70L-I,-70LL-I, -10L-I,-10LL-I

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FUNCTION

The operation mode of the M5M5408A is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

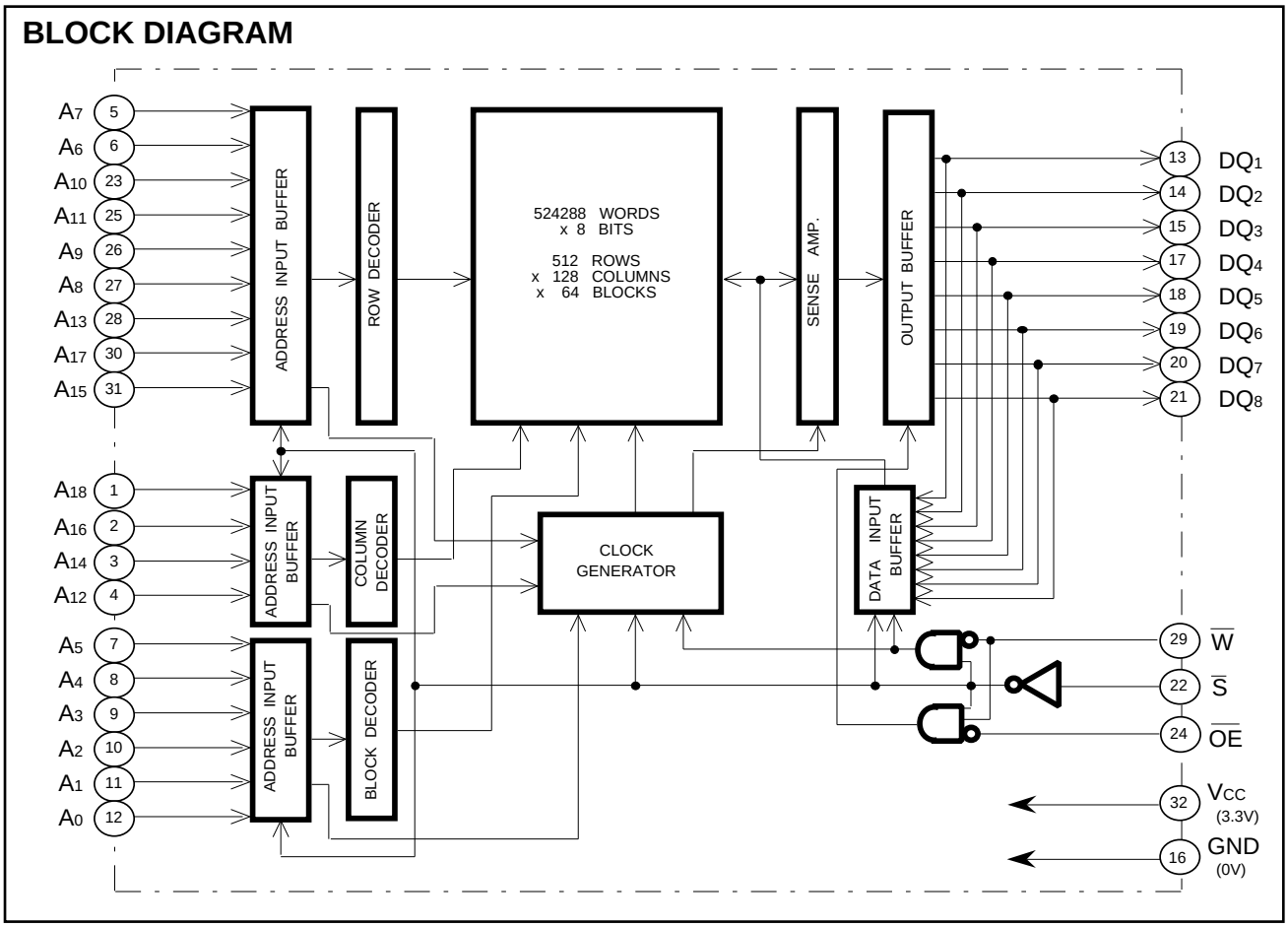
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state($\overline{S}$=L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-0.3~ 7	V
V_I	Input voltage		-0.3*~ Vcc+0.3	V
V_O	Output voltage		0~Vcc	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		-40 ~ 85	°C
Tstg	Storage temperature		-65 ~150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

ELECTRICAL CHARACTERISTICS (Ta= -40~85°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Units
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		Vcc+0.3	V
V_{IL}	Low-level input voltage			-0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=-1mA		2.4			V
		I_{OH}=-0.1mA		Vcc-0.5			
V_{OL}	Low-level output voltage	I_{OL} =2mA				0.4	V
I_I	Input leakage current	V_I =0~Vcc				±1	µA
I_O	Output leakage current	$\overline{S}$=V_{IH},OE=V_{IH},$V_{I/O}$=0~Vcc				±1	µA
I_{CC1}	Active supply current (AC,MOS level)	$\overline{S}$≤0.2V Other inputs≤ 0.2V or ≥Vcc-0.2V Output-open (duty 100%)	Minimum cycle		50	80	mA
			1MHz		25	30	
I_{CC2}	Active supply current (AC,TTL level)	$\overline{S}$=V_{IL} ,$\overline{W}$=V_{IH} Other inputs=V_{IH} or V_{IL} Output-open (duty 100%)	Minimum cycle		60	90	mA
			1MHz		30	40	
I_{CC3}	Stand by supply current	$\overline{S}$ ≥Vcc-0.2V Other inputs=0 ~Vcc	FP,VP,RT-L			200	µA
			FP,VP,RT-LL		1.0	40	µA
I_{CC4}	Stand by supply current	$\overline{S}$=V_{IH},Other inputs=0 ~Vcc				3	mA

* -3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE (Ta=-40~85°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C_i	Input capacitance (Ta=25°C)	V_I =GND, V_i =25mVrms,f=1MHz			6	pF
C_o	Output capacitance (Ta=25°C)	V_O=GND, V_o =25mVrms,f=1MHz			8	pF

Note 1: Direction for current flowing into IC is indicated as positive (no mark)
Note 2: Typical value is Vcc=5V,Ta=25°C
Note 3: Ci, Co are periodically sampled and are not 100% tested.

SWITCHING CHARACTERISTICS (Ta=-40~85°C, Vcc=5V±10%, unless otherwise noted)

READ CYCLE

Symbol	Parameter	Limits				Units
		M5M5408FP,TP, RT-70L-I,-70LL-I		M5M5408FP,TP, RT-10L-I,-10LL-I		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	70		100		ns
$t_{a(A)}$	Address access time		70		100	ns
$t_{a(S)}$	Chip select access time		70		100	ns
$t_{a(OE)}$	Output enable access time		35		50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		35	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		ns

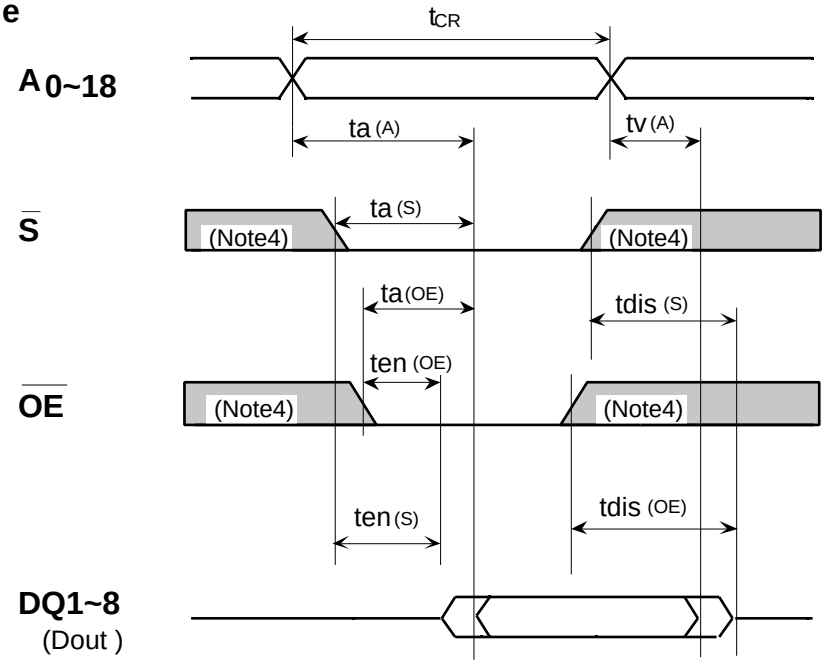
TIMING REQUIREMENTS (Ta=-40~85°C, Vcc=5V±10%, unless otherwise noted)

WRITE CYCLE

Symbol	Parameter	Limits				Units
		M5M5408FP,TP, RT-70L-I,-70LL-I		M5M5408FP,TP, RT-10L-I,-10LL-I		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	70		100		ns
$t_{w(W)}$	Write pulse width	50		60		ns
$t_{su(A)}$	Address set up time	0		0		ns
$t_{su(A-\overline{W}H)}$	Address set up time with respect to $\overline{W}$ high	60		80		ns
$t_{su(S)}$	Chip select set up time	60		80		ns
$t_{su(D)}$	Data set up time	30		35		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		35	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		ns

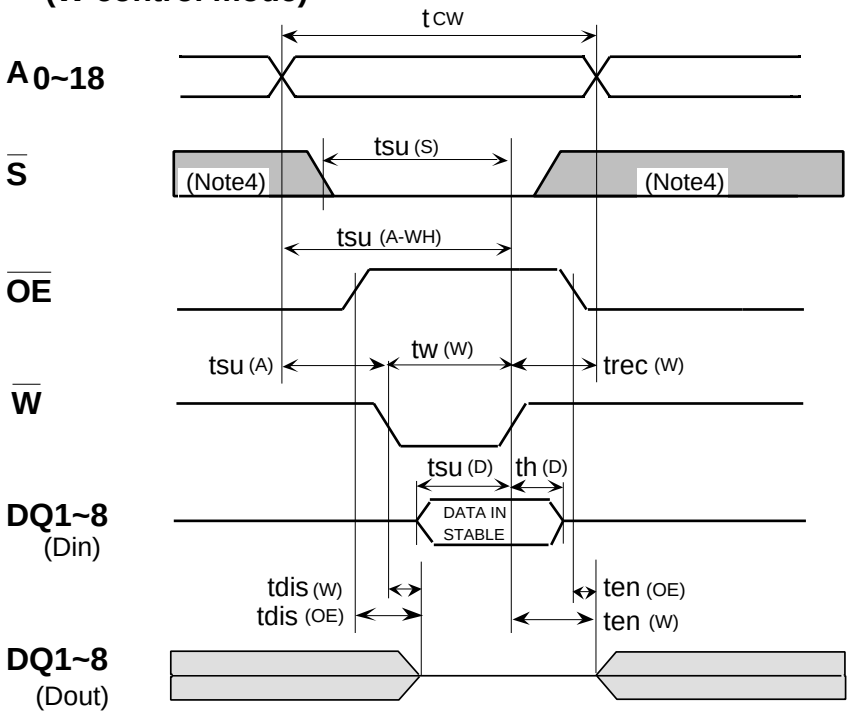
TIMING DIAGRAMS

Read cycle

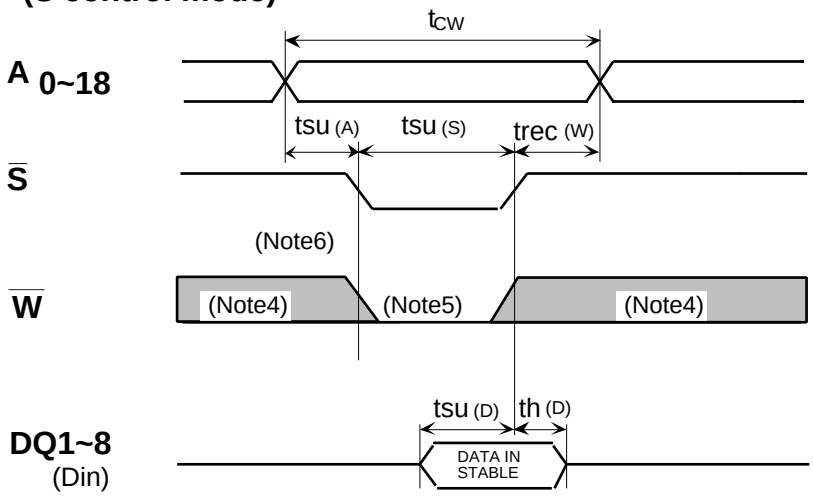


W="H" level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



MEASUREMENT CONDITIONS

Input pulse ····· V_{IH}=2.4V, V_{IL}=0.6V
Input rise time and fall time ····· 5ns
Reference level ····· V_H=V_{OL}=1.5V
Transition is measured ±500mV from steady state voltage (for t_{en},t_{dis}).
Output loads ····· Fig. 1, C_L=100pF (FP,TP,RT-10L,-10LL)
C_L=30pF (FP,TP,RT-70L,-70LL)
C_L=5pF (for ten,tdis)

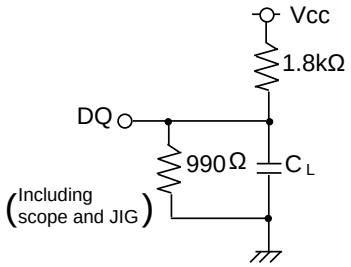


Fig.1 Output load

Note 4: Hatching indicates the state is "don't care".

Note 5: A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

Note 6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$,the output remains in the highimpedance state.

Note 7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta=-40~85°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Units
					Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage				2			V
$V_{I(S)}$	Chip select input $\overline{S}$	2.2V≤ $V_{CC(PD)}$			2.2			V
		2V≤ $V_{CC(PD)}$ ≤2.2V				$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	Vcc=3V, $\overline{S}$≥ Vcc-0.2V, Other inputs=0~3V	-L	-40~70°C			50	µA
				70~85°C			100	µA
			-LL	-40~70°C		0.4	10*	µA
				70~85°C			20	µA

* $I_{CC(PD)}$=1µA at Ta=25°C

(2) TIMING REQUIREMINTS (Ta=-40~85°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms