MOTOROLA

MCM10470*15
MCM10470*25

Advance Information

4096 x 1-BIT RANDOM ACCESS MEMORY

The MCM10470 is a 4096-bit Read/Write RAM organized for 4096 words by 1 bit. Data is selected or stored by means of a 12-bit address (A0 through A11) decoded on the chip. The chip is designed with a separate data-in line, a noninverting data output, and an active-low chip select.

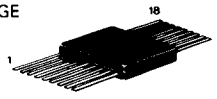
This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10K/10KH
- Pin-for-Pin Compatible with the Industry's Standard 10470
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature
- Address Access Time: MCM10470*25 25 ns (Max)
  MCM10470*15 15 ns (Max)

MECL

4096 x 1-BIT RANDOM ACCESS MEMORY

F SUFFIX
CERAMIC PACKAGE
CASE 747-01



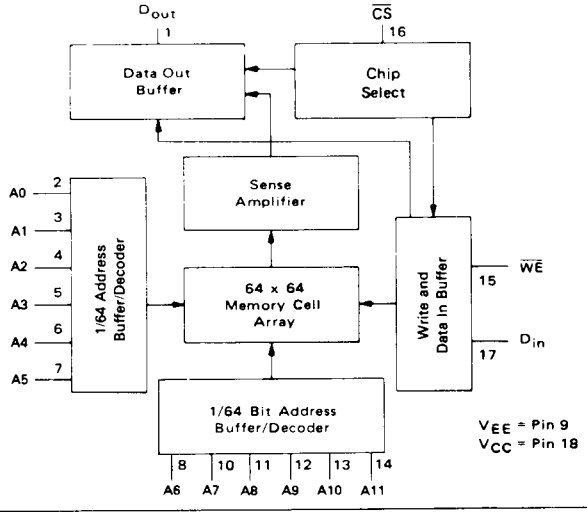
L SUFFIX
CERAMIC PACKAGE
CASE 680-06

ORDERING INFORMATION
Suffix Denotes
*MCM10470L15—Ceramic Dual-in-Line Package
*MCM10470F15—Ceramic Flat Package
*MCM10470L25—Ceramic Dual-in-Line Package
*MCM10470F25—Ceramic Flat Package

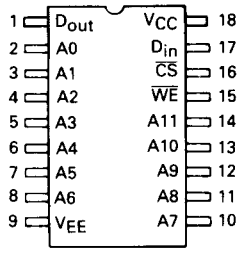
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current	I_O	−30	mAdc
Junction Operating Temperature	T_J	≤ 165	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESIGNATION

$\overline{CS}$	Chip Select
A0-A11	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L
ϕ = Irrelevant				

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 4-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, Q_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented noninverted at Q_{out}. (See Truth Table)

DC OPERATING CONDITIONS AND CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

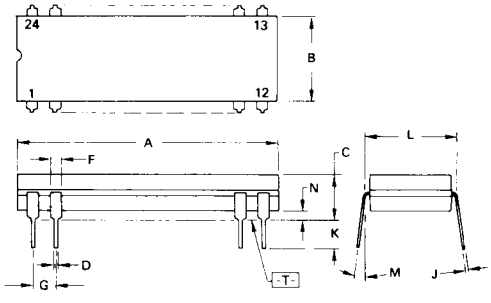
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

DC Characteristics	Symbol	MCM10474 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	Conditions
Power Supply Drain Current	I_{EE}		200		195		185	mAdc	All outputs and inputs open. Measure Pin 12.
Input Current High	I_{inH}		220		220		220	µAdc	Test one input at a time, all other inputs are open. V_{in} $V_{IH(max)}$.
Input Current Low Chip Select	I_{inL}	0.5		0.5		0.3		µAdc	Test one input at a time, all other inputs are open.
Input Current Low*	I_{inL}	-50		-50		-50		µAdc	V_{in} $V_{IL(min)}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V.
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020		-0.980		-0.920		Vdc	Threshold testing is performed and guaranteed on one input at a time. V_{in} V_{IHA} or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}		-1.645		-1.630		-1.605	Vdc	

* Minimum limit equals the maximum negative current the driving circuitry will be required to sink

OUTLINE DIMENSIONS

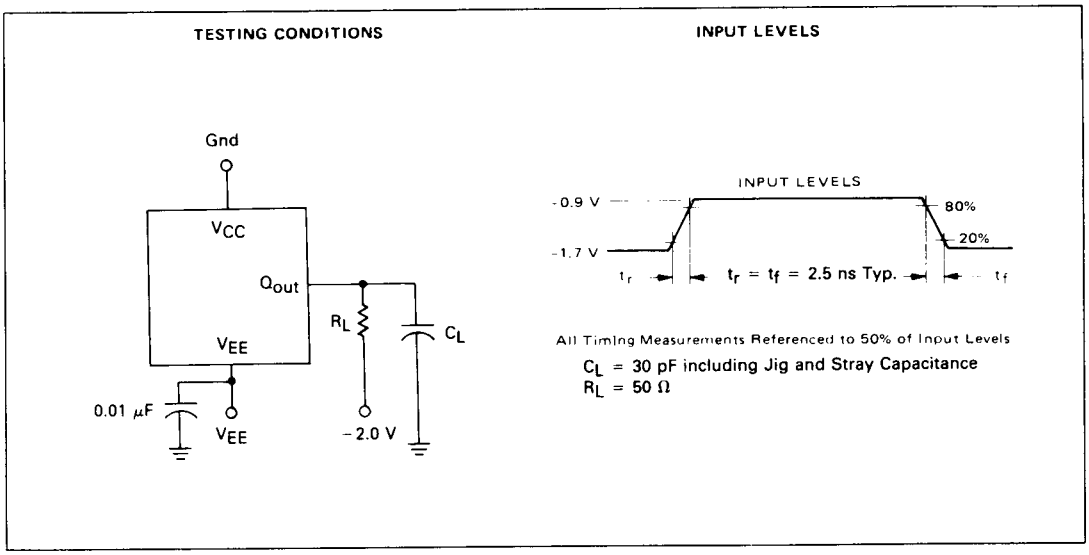


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.21	31.75	1.150	1.250
B	9.40	10.16	0.370	0.400
C		5.72		0.225
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.32	0.100	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

CASE 748-01

NOTES
1. DIMENSIONS [A] AND [B] ARE DATUM.
2. POSITIONAL TOLERANCES FOR LEADS: [Ø] [Ø 0.25 (0.010) Ⓜ T A Ⓜ B Ⓜ]
3. [T] IS SEATING PLANE.
4. DIMENSIONS A AND B INCLUDE MENISCUS.
5. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



AC OPERATING CONDITIONS AND CHARACTERISTICS

Guaranteed with V_{EE} = -5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10470*25 Min	MCM10470*25 Max	MCM10470*15 Min	MCM10470*15 Max	Unit	Conditions
Read Mode							See Figures 2 and 3. Measured at 50% of input to 50% of output.
Chip Select Access Time	t_{ACS}	—	10	—	8.0	ns	
Chip Select Recovery Time	t_{RCS}	—	10	—	8.0	ns	
Address Access Time	t_{AA}	—	25	—	15	ns	
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	—	15	—	ns	t_{WSA} = 3.0 ns MCM10470*25 t_{WSA} = 3.0 ns MCM10470*15 Measured at 50% of input to 50% of output. t_W = 25 ns MCM10470*25 t_W = 15 ns MCM10470*15
Data Setup Time Prior to Write	t_{WSD}	5.0	—	2.0	—	ns	
Data Hold Time After Write	t_{WHD}	5.0	—	2.0	—	ns	
Address Setup Time Prior to Write	t_{WSA}	8.0	—	3.0	—	ns	
Address Hold Time After Write	t_{WHA}	5.0	—	2.0	—	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	—	2.0	—	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	—	2.0	—	ns	
Write Disable Time	t_{WS}	—	10	—	8.0	ns	
Write Recovery Time	t_{WR}	—	15	—	8.0	ns	
Rise and Fall Time Output Rise and Fall Time	t_r, t_f	Typical 2.5				ns	Measured between 20% and 80% points.
Capacitance		Typical					Measured with a pulse technique.
Input Lead Capacitance	C_{in}	4.0				pF	
Output Lead Capacitance	C_{out}	7.0				pF	

Notes:
(1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 – CHIP SELECT ACCESS TIME

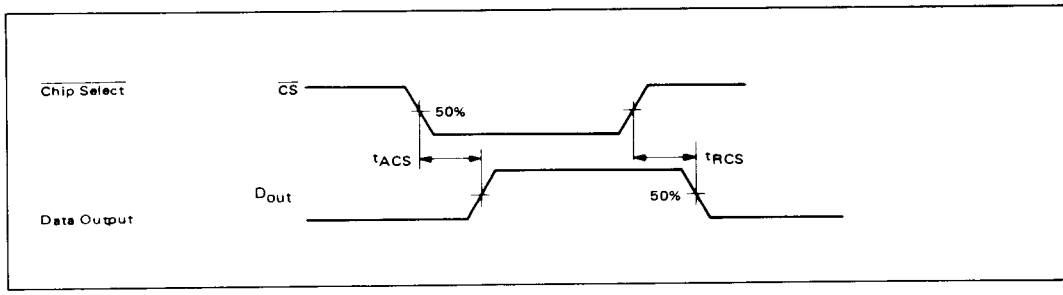


FIGURE 3 – ADDRESS ACCESS TIME

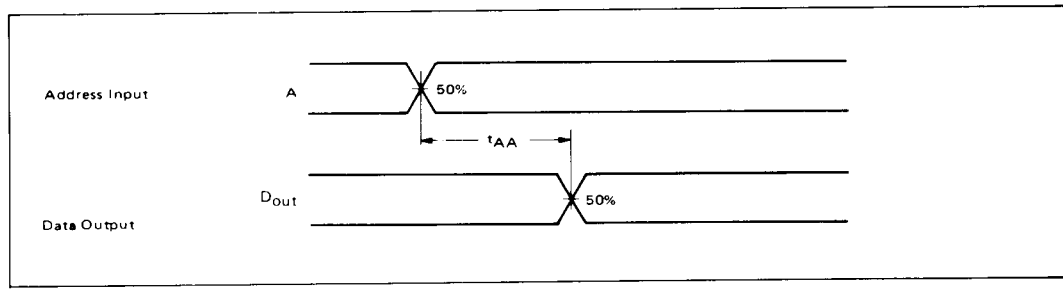


FIGURE 4 – WRITE STROBE MODE