MBM29PL64LM 90/10

Data Sheet *(Retired Product)*

This product has been retired and is not recommended for new designs. Availability of this document is retained for reference and historical purposes only.

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary.

For More Information

Please contact your local sales office for additional information about Spansion memory solutions.

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SPANSION™ Flash Memory

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

AMD

FUJITSU

FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20902-2E

FLASH MEMORY

CMOS

64 M (8M × 8/4M × 16) BIT

MirrorFlash™*

MBM29PL64LM 90/10

■ DESCRIPTION

The MBM29PL64LM is a 64M-bit, 3.0 V-only Flash memory organized as 8M bytes by 8 bits or 4M words by 16 bits. The MBM29PL64LM is offered in 48-pin, 58-pin TSOP(1) and 80-ball FBGA. The device is designed to be programmed in-system with the standard 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

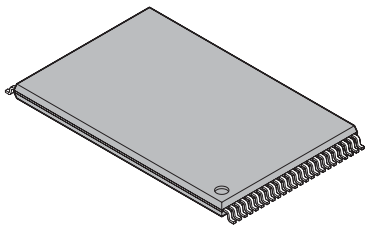
(Continued)

■ PRODUCT LINE UP

Part No.	MBM29PL64LM	
	90	10
V_{CC}	3.0 V to 3.6 V	3.0 V to 3.6 V
Max Address Access Time	90 ns	100 ns
Max $\overline{CE}$ Access Time	90 ns	100 ns
Max Page Read Access Time	25 ns	30 ns

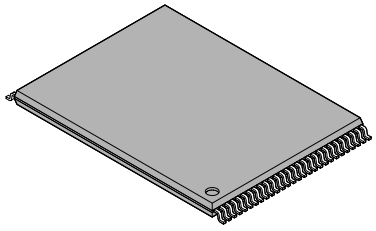
■ PACKAGES

48-pin plastic TSOP (1)



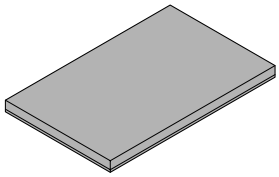
(FPT-48P-M19)

56-pin plastic TSOP (1)



(FPT-56P-M01)

80-ball plastic FBGA



(BGA-80P-M01)

* : MirrorFlash™ is a trademark of Fujitsu Limited.

Notes : • Programming in byte mode (× 8) is prohibited.
• Programming to the address that already contains data is prohibited.
(It is mandatory to erase data prior to overprogram on the same address.)

FUJITSU

(Continued)

The standard MBM29PL64LM offers access times of 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29PL64LM supports command set compatible with JEDEC single-power-supply EEPROMS standard. Commands are written into the command register. The register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29PL64LM is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm™ which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm™ which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. All sectors are erased when shipped from the factory.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6. Once the end of a program or erase cycle has been completed, the devices internally return to the read mode.

Fujitsu Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The devices electrically erase all bits within a sector simultaneously via hot-hole assisted erase. The words are programmed one word at a time using the EPROM programming mechanism of hot electron injection.

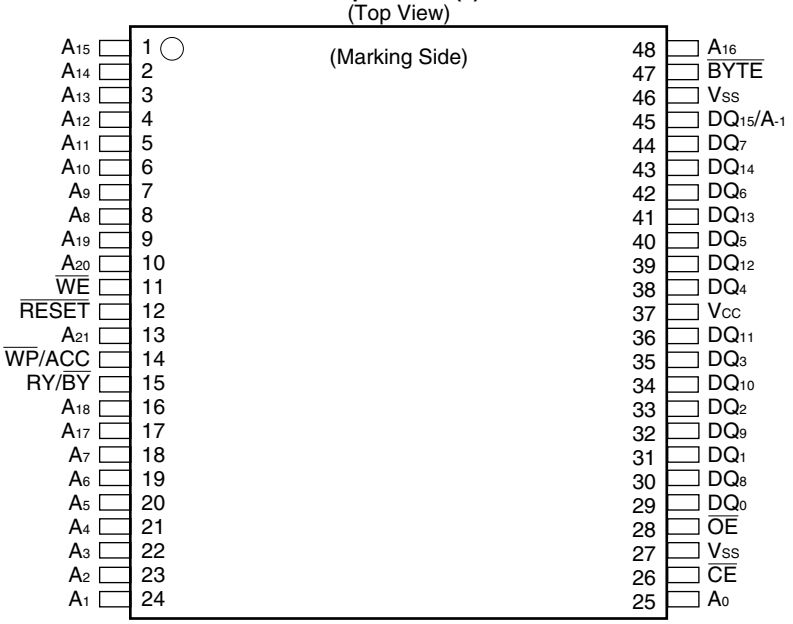
■ FEATURES

- **0.23 μm Process Technology**
- **Single 3.0 V read, program and erase**
  Minimizes system level power requirements
- **Industry-standard pinouts**
  48-pin TSOP (1) (Package suffix: TN - Normal Bend Type)
  56-pin TSOP (1) (Package suffix: PCN - Normal Bend Type)
  80-ball FBGA(Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance Page mode**
  Fast 8 bytes / 4 words access capablilty
- **Sector erase architecture**
  128 × 64K byte and 32K word sectors
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **HiddenROM**
  256 bytes / 128 words of HiddenROM, accessible through a “HiddenROM Entry” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC input pin**
  At V_{IL}, allows protection of first 64K bytes / 32K words sectors, regardless of sector protection/unprotection status
  At V_{ACC}, increases program performance
- **Embedded Erase™* Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™* Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switches themselves to low power mode
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another address
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector Group Protection**
  Hardware method disables any combination of sector groups from program or erase operations
- **Sector Group Protection Set function by Extended sector protect command**
- **Fast Programming Function by Extended Command**
- **Temporary sector group unprotection**
  Temporary sector group unprotection via the $\overline{\text{RESET}}$ pin
  This feature allows code changes in previously locked sectors
- **In accordance with CFI (Common Flash Memory Interface)**

***** : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

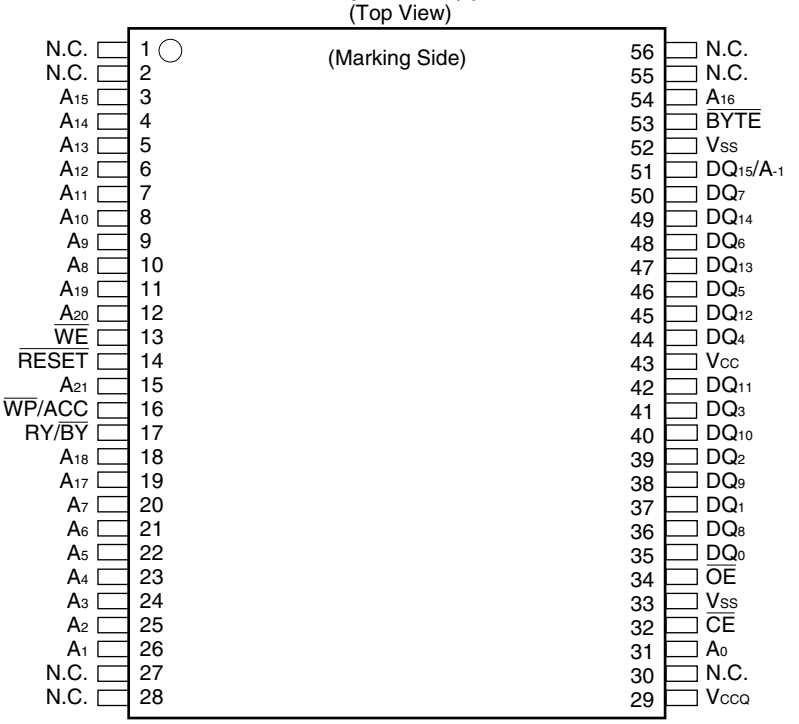
■ PIN ASSIGNMENTS

48 pin TSOP(1)
(Top View)



(FPT-48P-M19)

56 pin TSOP(1)
(Top View)



(FPT-56P-M01)

(Marking side)
FBGA
(Top view)

A8	B8	C8	D8	E8	F8	G8	H8	J8	K8	L8	M8
N.C.	N.C.	N.C.	N.C.	N.C.	V_{CCQ}	V_{SS}	N.C.	N.C.	N.C.	N.C.	N.C.
A7	B7	C7	D7	E7	F7	G7	H7	J7	K7	L7	M7
N.C.	N.C.	A_{13}	A_{12}	A_{14}	A_{15}	A_{16}	$\overline{BYTE}$	DQ_{15}/A_{-1}	V_{SS}	N.C.	N.C.
		C6	D6	E6	F6	G6	H6	J6	K6		
		A_9	A_8	A_{10}	A_{11}	DQ_7	DQ_{14}	DQ_{13}	DQ_6		
		C5	D5	E5	F5	G5	H5	J5	K5		
		$\overline{WE}$	$\overline{RESET}$	A_{21}	A_{19}	DQ_5	DQ_{12}	V_{CC}	DQ_4		
		C4	D4	E4	F4	G4	H4	J4	K4		
		RY/$\overline{BY}$	$\overline{WP}$/ACC	A_{18}	A_{20}	DQ_2	DQ_{10}	DQ_{11}	DQ_3		
		C3	D3	E3	F3	G3	H3	J3	K3		
		A_7	A_{17}	A_6	A_5	DQ_0	DQ_8	DQ_9	DQ_1		
A2	B2	C2	D2	E2	F2	G2	H2	J2	K2	L2	M2
N.C.	N.C.	A_3	A_4	A_2	A_1	A_0	$\overline{CE}$	$\overline{OE}$	V_{SS}	N.C.	N.C.
A1	B1	C1	D1	E1	F1	G1	H1	J1	K1	L1	M1
N.C.	N.C.	N.C.	V_{CC}	N.C.	N.C.	N.C.	V_{CCQ}	V_{SS}	N.C.	N.C.	N.C.

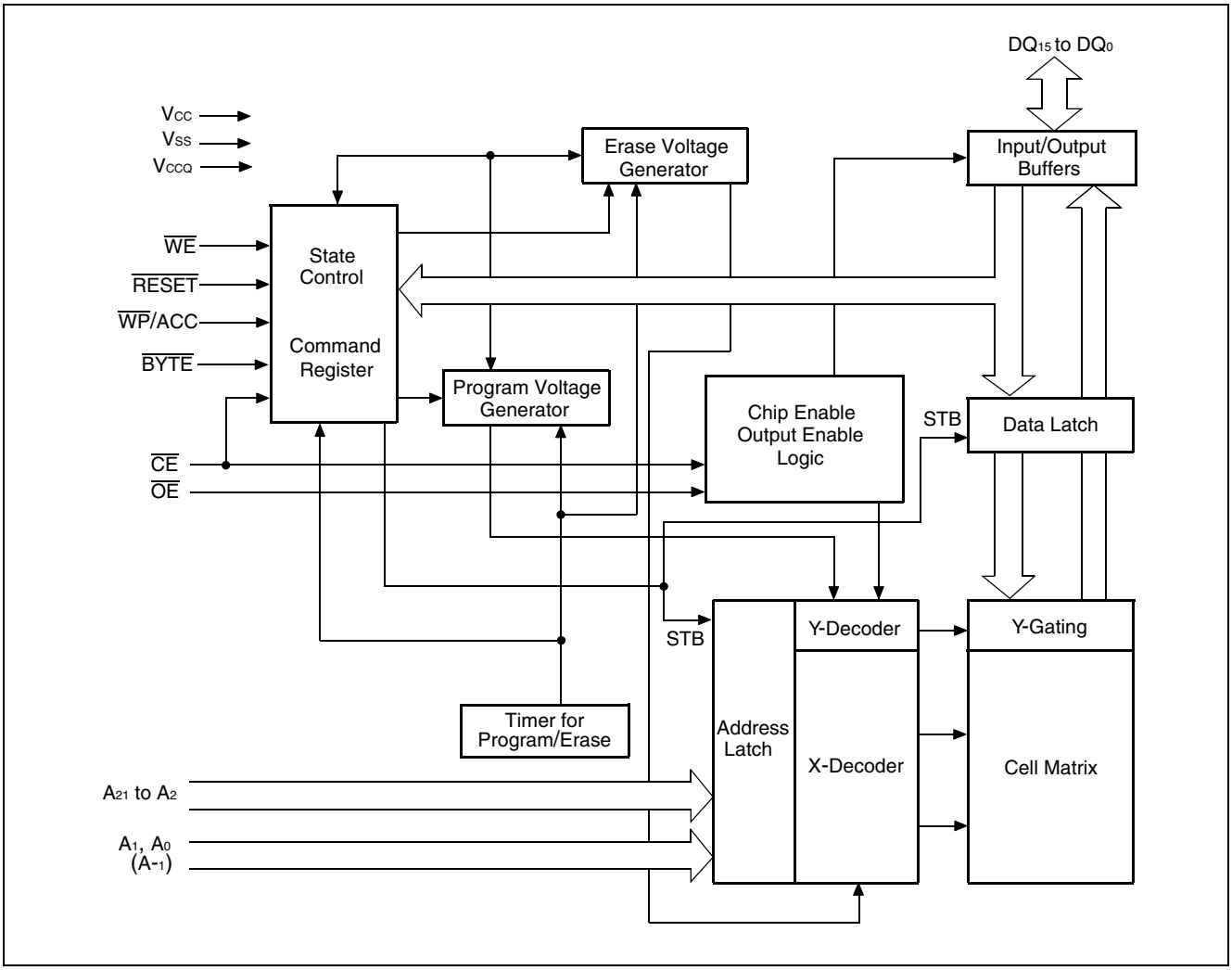
(BGA-80P-M01)

■ PIN DESCRIPTIONS

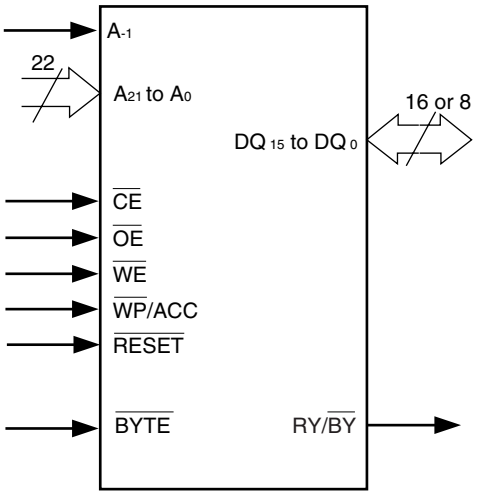
MBM29PL64LM Pin Configuration

Pin	Function
A_{21} to A_0, A_{-1}	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{WP}$/ACC	Hardware Write Protection/Program Acceleration
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Group Unprotection
$\overline{BYTE}$	Select 8-bit or 16-bit mode
RY/$\overline{BY}$	Ready/Busy Output
V_{CC}	Device Power Supply
V_{CCQ}	Ouput Voltage
V_{SS}	Device Ground
N.C.	No Internal Connection

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

MBM29PL64LM User Bus Operations (Word Mode : $\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_2	A_3	A_6	A_9	DQ_{15} to DQ_0	$\overline{RESET}$	$\overline{WP}$/ ACC
Standby	H	X	X	X	X	X	X	X	X	Hi-Z	H	X
Autoselect Manufacture Code*1	L	L	H	L	L	L	L	L	V_{ID}	Code	H	X
Autoselect Device Code*1	L	L	H	H	L	L	L	L	V_{ID}	Code	H	X
Read	L	L	H	A_0	A_1	A_2	A_3	A_6	A_9	D_{OUT}	H	X
Output Disable	L	H	H	X	X	X	X	X	X	Hi-Z	H	X
Write (Program/Erase)	L	H	L	A_0	A_1	A_2	A_3	A_6	A_9	*4	H	*5
Enable Sector Group Protection*2	L	H	L	L	H	L	L	L	X	*4	V_{ID}	H
Temporary Sector Group Unprotection	X	X	X	X	X	X	X	X	X	*4	V_{ID}	H
Reset (Hardware)	X	X	X	X	X	X	X	X	X	Hi-Z	L	X
Sector Write Protection*3	X	X	X	X	X	X	X	X	X	X	H	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.
Hi-Z = High-Z, V_{ID} = 11.5 V to 12.5 V

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See “MBM29PL64LM Standard Command Definitions”.

*2 : Refer to Sector Group Protection.

*3 : Protects the first 32K words sector (SA0)

*4 : D_{IN} or D_{OUT} as required by command sequence, data pulling, or sector protect algorithm

*5 : If $\overline{WP}$/ACC = V_{IL}, the first sector remain protected.
If $\overline{WP}$/ACC = V_{IH}, the first sector will be protected or unprotected as determined by the method specified in "Sector Group Protection".

MBM29PL64LM User Bus Operations (Byte Mode : $\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/A_{-1}	A_0	A_1	A_2	A_3	A_6	A_9	DQ_7 to DQ_0	$\overline{RESET}$	$\overline{WP}$/ ACC
Standby	H	X	X	X	X	X	X	X	X	X	Hi-Z	H	X
Autoselect Manufacture Code*1	L	L	H	L	L	L	L	L	L	V_{ID}	Code	H	X
Autoselect Device Code*1	L	L	H	L	H	L	L	L	L	V_{ID}	Code	H	X
Read	L	L	H	A_{-1}	A_0	A_1	A_2	A_3	A_6	A_9	D_{OUT}	H	X
Output Disable	L	H	H	X	X	X	X	X	X	X	Hi-Z	H	X
Write (Erase)	L	H	L	A_{-1}	A_0	A_1	A_2	A_3	A_6	A_9	*4	H	*5
Enable Sector Group Protection*2	L	H	L	L	L	H	L	L	L	X	*4	V_{ID}	H
Temporary Sector Group Unprotection	X	X	X	X	X	X	X	X	X	X	*4	V_{ID}	H
Reset (Hardware)	X	X	X	X	X	X	X	X	X	X	Hi-Z	L	X
Sector Write Protection*3	X	X	X	X	X	X	X	X	X	X	X	H	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.
Hi-Z = High-Z, V_{ID} = 11.5 V to 12.5 V

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See “MBM29PL64LM Standard Command Definitions”.

*2 : Refer to Sector Group Protection.

*3 : Protects the first 64K bytes sector (SA0)

*4 : D_{IN} or D_{OUT} as required by command sequence, data pulling, or sector protect algorithm

*5 : If $\overline{WP}$/ACC = V_{IL}, the first sector remain protected.
If $\overline{WP}$/ACC = V_{IH}, the first sector will be protected or unprotected as determined by the method specified in "Sector Group Protection".

MBM29PL64LM Standard Command Definitions*1

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset*2	Word/ Byte	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Reset*2	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA*13	RD*13	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect (Device ID)	Word	3	555h	AAh	2AAh	55h	555h	90h	00h*13	04h*13	—	—	—	—
	Byte		AAAh		555h		AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Program/Erase Suspend*3		1	XXXh	B0h	—	—	—	—	—	—	—	—	—	—
Program/Erase Resume*3		1	XXXh	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode*4	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program*4	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode*5	Word/ Byte	2	XXXh	90h	XXXh	00h*12	—	—	—	—	—	—	—	—
Write to Buffer	Word	20	555h	AAh	2AAh	55h	SA	25h	SA	0Fh	PA	PD	WBL	PD
	Byte		AAAh		555h									
Program Buffer to Flash (Confirm)		1	SA	29h	—	—	—	—	—	—	—	—	—	—
Write to Buffer Abort Reset*6	Word	3	555h	AAh	2AAh	55h	555h	F0h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Extended Sector Group Protection*7,*8	Word	4	XXXh	60h	SGA	60h	SGA	40h	SGA *13	SD*13	—	—	—	—
	Byte													
Query*9	Word	1	55h	98h	—	—	—	—	—	—	—	—	—	—
	Byte		AAh											
HiddenROM Entry*10	Word	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
HiddenROM Program *10,*11	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
HiddenROM Exit*11	Word	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h	—	—	—	—
	Byte		AAAh		555h		AAAh							

(Continued)

(Continued)

Legend : Address bits A_{21} to A_{15} = X = "H" or "L" for all address commands except for Program Address (PA), Sector Address (SA) and Sector Group Address (SGA).
Bus operations are defined in "MBM29PL64LM User Bus Operations (Word Mode : $\overline{BYTE}$ = V_{IH})" and "MBM29PL64LM User Bus Operations (Byte Mode : $\overline{BYTE}$ = V_{IL})".

- RA = Address of the memory location to be read.
- PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the write pulse.
- SA = Address of the sector to be programmed / erased. The combination of A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, and A_{15} will uniquely select any sector. See "Sector Address Table (MBM29PL64LM)".
- SGA = Sector Group Address to be protected. See "Sector Group Address Table (MBM29PL64LM)".
- RD = Data read from location RA during read operation.
- PD = Data to be programmed at location PA. Data is latched on the rising edge of write plus.
- SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- WBL = Write Buffer Location
- HRA = Address of the HiddenROM area ;
  Word Mode : 000000h to 000007h
  Byte Mode : 000000h to 0000FFh

*1 : The command combinations not described in "MBM29PL64LM Standard Command Definitions" are illegal.

*2 : Both of these reset commands are equivalent except for "Write to Buffer Abort" reset.

*3 : The Erase Suspend and Erase Resume command are valid only during a sector erase operation.

*4 : The Set to Fast Mode command is required prior to the Fast Program command.

*5 : The Reset from Fast Mode command is required to return to the read mode when the device is in fast mode.

*6 : Reset to the read mode. The Write to Buffer Abert Reset command is required after the Write to Buffer operation was aborted.

*7 : This command is valid while $\overline{RESET}$ = V_{ID}.

*8 : Sector Group Address (SGA) with A_6 = 0, A_3 = 0, A_2 = 0, A_1 = 1, and A_0 = 0

*9 : The valid address are A_6 to A_0.

*10 : The HiddenROM Entry command is required prior to the HiddenROM programming.

*11 : This command is valid during HiddenROM mode.

*12 : The data "F0h" is also acceptable.

*13 : Indicates read cycle.

Sector Group Protection Verify Autoselect Codes

Type		A_{21} to A_{15}	A_6	A_3	A_2	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacturer's Code		X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	Word	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	227Eh
	Byte							V_{IL}	7Eh
Extended Device Code*2	Word	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	220Ch
	Byte							V_{IL}	0Ch
	Word	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	2201h
	Byte							V_{IL}	01h
Sector Group Protection*4		Sector Group Addresses	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	*3

*1 : A_{-1} is for Byte mode.

*2 : At Word mode, a read cycle at address 01h (at Byte mode, 02h) outputs device code. When 227Eh (at Byte mode, 7Eh) is output, it indicates that reading two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of 0Eh (at Byte mode, 1Ch), as well as at 0Fh (at Byte mode, 1Eh).

*3 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*4 : Given $\overline{CE}$ = Fix, wait for one cycle after the rising edge of $\overline{WE}$ (the last write command) , then indicate SGA as (A_6, A_3, A_2, A_1, A_0, A_{-1}) = (0, 0, 0, 1, 0, 0) .

Sector Address Table (MBM29PL64LM)

Sector	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
SA0	0	0	0	0	0	0	0	64/32	000000h to 00FFFFh	000000h to 007FFFh
SA1	0	0	0	0	0	0	1	64/32	010000h to 01FFFFh	008000h to 00FFFFh
SA2	0	0	0	0	0	1	0	64/32	020000h to 02FFFFh	010000h to 017FFFh
SA3	0	0	0	0	0	1	1	64/32	030000h to 03FFFFh	018000h to 01FFFFh
SA4	0	0	0	0	1	0	0	64/32	040000h to 04FFFFh	020000h to 027FFFh
SA5	0	0	0	0	1	0	1	64/32	050000h to 05FFFFh	028000h to 02FFFFh
SA6	0	0	0	0	1	1	0	64/32	060000h to 06FFFFh	030000h to 037FFFh
SA7	0	0	0	0	1	1	1	64/32	070000h to 07FFFFh	038000h to 03FFFFh
SA8	0	0	0	1	0	0	0	64/32	080000h to 08FFFFh	040000h to 047FFFh
SA9	0	0	0	1	0	0	1	64/32	090000h to 09FFFFh	048000h to 04FFFFh
SA10	0	0	0	1	0	1	0	64/32	0A0000h to 0AFFFFh	050000h to 057FFFh
SA11	0	0	0	1	0	1	1	64/32	0B0000h to 0BFFFFh	058000h to 05FFFFh
SA12	0	0	0	1	1	0	0	64/32	0C0000h to 0CFFFFh	060000h to 067FFFh
SA13	0	0	0	1	1	0	1	64/32	0D0000h to 0DFFFFh	068000h to 06FFFFh
SA14	0	0	0	1	1	1	0	64/32	0E0000h to 0EFFFFh	070000h to 077FFFh
SA15	0	0	0	1	1	1	1	64/32	0F0000h to 0FFFFFh	078000h to 07FFFFh
SA16	0	0	1	0	0	0	0	64/32	100000h to 10FFFFh	080000h to 087FFFh
SA17	0	0	1	0	0	0	1	64/32	110000h to 11FFFFh	088000h to 08FFFFh
SA18	0	0	1	0	0	1	0	64/32	120000h to 12FFFFh	090000h to 097FFFh
SA19	0	0	1	0	0	1	1	64/32	130000h to 13FFFFh	098000h to 09FFFFh
SA20	0	0	1	0	1	0	0	64/32	140000h to 14FFFFh	0A0000h to 0A7FFFh
SA21	0	0	1	0	1	0	1	64/32	150000h to 15FFFFh	0A8000h to 0AFFFFh
SA22	0	0	1	0	1	1	0	64/32	160000h to 16FFFFh	0B0000h to 0B7FFFh
SA23	0	0	1	0	1	1	1	64/32	170000h to 17FFFFh	0B8000h to 0BFFFFh
SA24	0	0	1	1	0	0	0	64/32	180000h to 18FFFFh	0C0000h to 0C7FFFh
SA25	0	0	1	1	0	0	1	64/32	190000h to 19FFFFh	0C8000h to 0CFFFFh
SA26	0	0	1	1	0	1	0	64/32	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
SA27	0	0	1	1	0	1	1	64/32	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
SA28	0	0	1	1	1	0	0	64/32	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
SA29	0	0	1	1	1	0	1	64/32	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
SA30	0	0	1	1	1	1	0	64/32	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh

(Continued)

Sector	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
SA31	0	0	1	1	1	1	1	64/32	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
SA32	0	1	0	0	0	0	0	64/32	200000h to 20FFFFh	100000h to 107FFFh
SA33	0	1	0	0	0	0	1	64/32	210000h to 21FFFFh	108000h to 10FFFFh
SA34	0	1	0	0	0	1	0	64/32	220000h to 22FFFFh	110000h to 117FFFh
SA35	0	1	0	0	0	1	1	64/32	230000h to 23FFFFh	118000h to 11FFFFh
SA36	0	1	0	0	1	0	0	64/32	240000h to 24FFFFh	120000h to 127FFFh
SA37	0	1	0	0	1	0	1	64/32	250000h to 25FFFFh	128000h to 12FFFFh
SA38	0	1	0	0	1	1	0	64/32	260000h to 26FFFFh	130000h to 137FFFh
SA39	0	1	0	0	1	1	1	64/32	270000h to 27FFFFh	138000h to 13FFFFh
SA40	0	1	0	1	0	0	0	64/32	280000h to 28FFFFh	140000h to 147FFFh
SA41	0	1	0	1	0	0	1	64/32	290000h to 29FFFFh	148000h to 14FFFFh
SA42	0	1	0	1	0	1	0	64/32	2A0000h to 2AFFFFh	150000h to 157FFFh
SA43	0	1	0	1	0	1	1	64/32	2B0000h to 2BFFFFh	158000h to 15FFFFh
SA44	0	1	0	1	1	0	0	64/32	2C0000h to 2CFFFFh	160000h to 167FFFh
SA45	0	1	0	1	1	0	1	64/32	2D0000h to 2DFFFFh	168000h to 16FFFFh
SA46	0	1	0	1	1	1	0	64/32	2E0000h to 2EFFFFh	170000h to 177FFFh
SA47	0	1	0	1	1	1	1	64/32	2F0000h to 2FFFFFh	178000h to 17FFFFh
SA48	0	1	1	0	0	0	0	64/32	300000h to 30FFFFh	180000h to 187FFFh
SA49	0	1	1	0	0	0	1	64/32	310000h to 31FFFFh	188000h to 18FFFFh
SA50	0	1	1	0	0	1	0	64/32	320000h to 32FFFFh	190000h to 197FFFh
SA51	0	1	1	0	0	1	1	64/32	330000h to 33FFFFh	198000h to 19FFFFh
SA52	0	1	1	0	1	0	0	64/32	340000h to 34FFFFh	1A0000h to 1A7FFFh
SA53	0	1	1	0	1	0	1	64/32	350000h to 35FFFFh	1A8000h to 1AFFFFh
SA54	0	1	1	0	1	1	0	64/32	360000h to 36FFFFh	1B0000h to 1B7FFFh
SA55	0	1	1	0	1	1	1	64/32	370000h to 37FFFFh	1B8000h to 1BFFFFh
SA56	0	1	1	1	0	0	0	64/32	380000h to 38FFFFh	1C0000h to 1C7FFFh
SA57	0	1	1	1	0	0	1	64/32	390000h to 39FFFFh	1C8000h to 1CFFFFh
SA58	0	1	1	1	0	1	0	64/32	3A0000h to 3AFFFFh	1D0000h to 1D7FFFh
SA59	0	1	1	1	0	1	1	64/32	3B0000h to 3BFFFFh	1D8000h to 1DFFFFh
SA60	0	1	1	1	1	0	0	64/32	3C0000h to 3CFFFFh	1E0000h to 1E7FFFh
SA61	0	1	1	1	1	0	1	64/32	3D0000h to 3DFFFFh	1E8000h to 1EFFFFh
SA62	0	1	1	1	1	1	0	64/32	3E0000h to 3EFFFFh	1F0000h to 1F7FFFh

(Continued)

Sector	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
SA63	0	1	1	1	1	1	1	64/32	3F0000h to 3FFFFFh	1F8000h to 1FFFFFh
SA64	1	0	0	0	0	0	0	64/32	400000h to 40FFFFh	200000h to 207FFFh
SA65	1	0	0	0	0	0	1	64/32	410000h to 41FFFFh	208000h to 20FFFFh
SA66	1	0	0	0	0	1	0	64/32	420000h to 42FFFFh	210000h to 217FFFh
SA67	1	0	0	0	0	1	1	64/32	430000h to 43FFFFh	218000h to 21FFFFh
SA68	1	0	0	0	1	0	0	64/32	440000h to 44FFFFh	220000h to 227FFFh
SA69	1	0	0	0	1	0	1	64/32	450000h to 45FFFFh	228000h to 22FFFFh
SA70	1	0	0	0	1	1	0	64/32	460000h to 46FFFFh	230000h to 237FFFh
SA71	1	0	0	0	1	1	1	64/32	470000h to 47FFFFh	238000h to 23FFFFh
SA72	1	0	0	1	0	0	0	64/32	480000h to 48FFFFh	240000h to 247FFFh
SA73	1	0	0	1	0	0	1	64/32	490000h to 49FFFFh	248000h to 24FFFFh
SA74	1	0	0	1	0	1	0	64/32	4A0000h to 4AFFFFh	250000h to 257FFFh
SA75	1	0	0	1	0	1	1	64/32	4B0000h to 4BFFFFh	258000h to 25FFFFh
SA76	1	0	0	1	1	0	0	64/32	4C0000h to 4CFFFFh	260000h to 267FFFh
SA77	1	0	0	1	1	0	1	64/32	4D0000h to 4DFFFFh	268000h to 26FFFFh
SA78	1	0	0	1	1	1	0	64/32	4E0000h to 4EFFFFh	270000h to 277FFFh
SA79	1	0	0	1	1	1	1	64/32	4F0000h to 4FFFFFh	278000h to 27FFFFh
SA80	1	0	1	0	0	0	0	64/32	500000h to 50FFFFh	280000h to 287FFFh
SA81	1	0	1	0	0	0	1	64/32	510000h to 51FFFFh	288000h to 28FFFFh
SA82	1	0	1	0	0	1	0	64/32	520000h to 52FFFFh	290000h to 297FFFh
SA83	1	0	1	0	0	1	1	64/32	530000h to 53FFFFh	298000h to 29FFFFh
SA84	1	0	1	0	1	0	0	64/32	540000h to 54FFFFh	2A0000h to 2A7FFFh
SA85	1	0	1	0	1	0	1	64/32	550000h to 55FFFFh	2A8000h to 2AFFFFh
SA86	1	0	1	0	1	1	0	64/32	560000h to 56FFFFh	2B0000h to 2B7FFFh
SA87	1	0	1	0	1	1	1	64/32	570000h to 57FFFFh	2B8000h to 2BFFFFh
SA88	1	0	1	1	0	0	0	64/32	580000h to 58FFFFh	2C0000h to 2C7FFFh
SA89	1	0	1	1	0	0	1	64/32	590000h to 59FFFFh	2C8000h to 2CFFFFh
SA90	1	0	1	1	0	1	0	64/32	5A0000h to 5AFFFFh	2D0000h to 2D7FFFh
SA91	1	0	1	1	0	1	1	64/32	5B0000h to 5BFFFFh	2D8000h to 2DFFFFh
SA92	1	0	1	1	1	0	0	64/32	5C0000h to 5CFFFFh	2E0000h to 2EE7FFh
SA93	1	0	1	1	1	0	1	64/32	5D0000h to 5DFFFFh	2E8000h to 2EFFFFh
SA94	1	0	1	1	1	1	0	64/32	5E0000h to 5EFFFFh	2F0000h to 2F7FFFh

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Sector	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
SA95	1	0	1	1	1	1	1	64/32	5F0000h to 5FFFFFh	2F8000h to 2FFFFFh
SA96	1	1	0	0	0	0	0	64/32	600000h to 60FFFFh	300000h to 307FFFh
SA97	1	1	0	0	0	0	1	64/32	610000h to 61FFFFh	308000h to 30FFFFh
SA98	1	1	0	0	0	1	0	64/32	620000h to 62FFFFh	310000h to 317FFFh
SA99	1	1	0	0	0	1	1	64/32	630000h to 63FFFFh	318000h to 31FFFFh
SA100	1	1	0	0	1	0	0	64/32	640000h to 64FFFFh	320000h to 327FFFh
SA101	1	1	0	0	1	0	1	64/32	650000h to 65FFFFh	328000h to 32FFFFh
SA102	1	1	0	0	1	1	0	64/32	660000h to 66FFFFh	330000h to 337FFFh
SA103	1	1	0	0	1	1	1	64/32	670000h to 67FFFFh	338000h to 33FFFFh
SA104	1	1	0	1	0	0	0	64/32	680000h to 68FFFFh	340000h to 347FFFh
SA105	1	1	0	1	0	0	1	64/32	690000h to 69FFFFh	348000h to 34FFFFh
SA106	1	1	0	1	0	1	0	64/32	6A0000h to 6AFFFFh	350000h to 357FFFh
SA107	1	1	0	1	0	1	1	64/32	6B0000h to 6BFFFFh	358000h to 35FFFFh
SA108	1	1	0	1	1	0	0	64/32	6C0000h to 6CFFFFh	360000h to 367FFFh
SA109	1	1	0	1	1	0	1	64/32	6D0000h to 6DFFFFh	368000h to 36FFFFh
SA110	1	1	0	1	1	1	0	64/32	6E0000h to 6EFFFFh	370000h to 377FFFh
SA111	1	1	0	1	1	1	1	64/32	6F0000h to 6FFFFFh	378000h to 37FFFFh
SA112	1	1	1	0	0	0	0	64/32	700000h to 70FFFFh	380000h to 387FFFh
SA113	1	1	1	0	0	0	1	64/32	710000h to 71FFFFh	388000h to 38FFFFh
SA114	1	1	1	0	0	1	0	64/32	720000h to 72FFFFh	390000h to 397FFFh
SA115	1	1	1	0	0	1	1	64/32	730000h to 73FFFFh	398000h to 39FFFFh
SA116	1	1	1	0	1	0	0	64/32	740000h to 74FFFFh	3A0000h to 3A7FFFh
SA117	1	1	1	0	1	0	1	64/32	750000h to 75FFFFh	3A8000h to 3AFFFFh
SA118	1	1	1	0	1	1	0	64/32	760000h to 76FFFFh	3B0000h to 3B7FFFh
SA119	1	1	1	0	1	1	1	64/32	770000h to 77FFFFh	3B8000h to 3BFFFFh
SA120	1	1	1	1	0	0	0	64/32	780000h to 78FFFFh	3C0000h to 3C7FFFh
SA121	1	1	1	1	0	0	1	64/32	790000h to 79FFFFh	3C8000h to 3CFFFFh
SA122	1	1	1	1	0	1	0	64/32	7A0000h to 7AFFFFh	3D0000h to 3D7FFFh
SA123	1	1	1	1	0	1	1	64/32	7B0000h to 7BFFFFh	3D8000h to 3DFFFFh
SA124	1	1	1	1	1	0	0	64/32	7C0000h to 7CFFFFh	3E0000h to 3E7FFFh
SA125	1	1	1	1	1	0	1	64/32	7D0000h to 7DFFFFh	3E8000h to 3EFFFFh
SA126	1	1	1	1	1	1	0	64/32	7E0000h to 7EFFFFh	3F0000h to 3F7FFFh
SA127	1	1	1	1	1	1	1	64/32	7F0000h to 7FFFFFh	3F8000h to 3FFFFFh

Note : The address range is A_{21} : A_{-1} if in Byte mode ($\overline{BYTE}$ = V_{IL}) .
The address range is A_{21} : A_0 if in Word mode ($\overline{BYTE}$ = V_{IH}) .

Sector Group Address Table (MBM29PL64LM)

Sector Group	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector group size (Kbytes/Kwords)	Sectors
SGA0	0	0	0	0	0	0	0	64/32	SA0
SGA1	0	0	0	0	0	0	1	64/32	SA1
SGA2	0	0	0	0	0	1	0	64/32	SA2
SGA3	0	0	0	0	0	1	1	64/32	SA3
SGA4	0	0	0	0	1	0	0	256/128	SA4 to SA7
SGA5	0	0	0	1	0	0	0	256/128	SA8 to SA11
SGA6	0	0	0	1	1	0	0	256/128	SA12 to SA15
SGA7	0	0	1	0	0	0	0	256/128	SA16 to SA19
SGA8	0	0	1	0	1	0	0	256/128	SA20 to SA23
SGA9	0	0	1	1	0	0	0	256/128	SA24 to SA27
SGA10	0	0	1	1	1	0	0	256/128	SA28 to SA31
SGA11	0	1	0	0	0	0	0	256/128	SA32 to SA35
SGA12	0	1	0	0	1	0	0	256/128	SA36 to SA39
SGA13	0	1	0	1	0	0	0	256/128	SA40 to SA43
SGA14	0	1	0	1	1	0	0	256/128	SA44 to SA47
SGA15	0	1	1	0	0	0	0	256/128	SA48 to SA51
SGA16	0	1	1	0	1	0	0	256/128	SA52 to SA55
SGA17	0	1	1	1	0	0	0	256/128	SA56 to SA59
SGA18	0	1	1	1	1	0	0	256/128	SA60 to SA63
SGA19	1	0	0	0	0	0	0	256/128	SA64 to SA67
SGA20	1	0	0	0	1	0	0	256/128	SA68 to SA71
SGA21	1	0	0	1	0	0	0	256/128	SA72 to SA75
SGA22	1	0	0	1	1	0	0	256/128	SA76 to SA79
SGA23	1	0	1	0	0	0	0	256/128	SA80 to SA83
SGA24	1	0	1	0	1	0	0	256/128	SA84 to SA87
SGA25	1	0	1	1	0	0	0	256/128	SA88 to SA91
SGA26	1	0	1	1	1	0	0	256/128	SA92 to SA95
SGA27	1	1	0	0	0	0	0	256/128	SA96 to SA99
SGA28	1	1	0	0	1	0	0	256/128	SA100 to SA103
SGA29	1	1	0	1	0	0	0	256/128	SA104 to SA107
SGA30	1	1	0	1	1	0	0	256/128	SA108 to SA111
SGA31	1	1	1	0	0	0	0	256/128	SA112 to SA115
SGA32	1	1	1	0	1	0	0	256/128	SA116 to SA119
SGA33	1	1	1	1	0	0	0	256/128	SA120 to SA123
SGA34	1	1	1	1	1	0	0	64/32	SA124
SGA35	1	1	1	1	1	0	1	64/32	SA125
SGA36	1	1	1	1	1	1	0	64/32	SA126
SGA37	1	1	1	1	1	1	1	64/32	SA127

Common Flash Memory Interface Code

A_0 to A_6	DQ_0 to DQ_{15}	Description
10h 11h 12h	0051h 0052h 0059h	Query-unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set (02h = Fujitsu standard)
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = not applicable)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = not applicable)
1Bh	0027h	V_{CC} Min (write/erase) DQ_7 to DQ_4: 1 V/bit, DQ_3 to DQ_0: 100 mV/bit
1Ch	0036h	V_{CC} Max (write/erase) DQ_7 to DQ_4: 1 V/bit, DQ_3 to DQ_0: 100 mV/bit
1Dh	0000h	V_{PP} Min voltage (00h = no V_{pp} pin)
1Eh	0000h	V_{PP} Max voltage (00h =no V_{pp} pin)
1Fh	0007h	Typical timeout per single write 2^N μs
20h	0007h	Typical timeout for Min size buffer write 2^N μs
21h	000Ah	Typical timeout per individual sector erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms
23h	0001h	Max timeout for write 2^N times typical
24h	0005h	Max timeout for buffer write 2^N times typical
25h	0004h	Max timeout per individual sector erase 2^N times typical
26h	0000h	Max timeout for full chip erase 2^N times typical
27h	0017h	Device Size = 2^N byte
28h 29h	0002h 0000h	Flash Device Interface description 02h : × 8/ × 16
2Ah 2Bh	0005h 0000h	Max number of byte in multi-byte write = 2^N
2Ch	0002h	Number of Erase Block Regions within device (02h = Boot)
2Dh 2Eh 2Fh 30h	007Fh 0000h 0020h 0000h	Erase Block Region 1 Information
31h 32h 33h 34h	003Eh 0000h 0000h 0001h	Erase Block Region 2 Information

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A_0 to A_6	DQ_0 to DQ_{15}	Description
35h 36h 37h 38h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0008h	Address Sensitive Unlock Required
46h	0002h	Erase Suspend (02h = To Read & Write)
47h	0004h	Number of sectors in per group
48h	0001h	Sector Temporary Unprotection (01h = Supported)
49h	0004h	Sector Protection Algorithm
4Ah	0000h	Dual Operation (00h = Not Supported)
4Bh	0000h	Burst Mode Type (00h = Not Supported)
4Ch	0001h	Page Mode Type (01h = 4-Word Page Supported)
4Dh	00B5h	V_{ACC} (Acceleration) Supply Minimum DQ_7 to DQ_4: 1 V/bit, DQ_3 to DQ_0: 100 mV/bit
4Eh	00C5h	V_{ACC} (Acceleration) Supply Maximum DQ_7 to DQ_4: 1 V/bit, DQ_3 to DQ_0: 100 mV/bit
4Fh	0004h	Write Protect (04h = Uniform Sectors Bottom Write Protect)
50h	01h	Program Suspend (01h = Supported)

■ FUNCTIONAL DESCRIPTION

Standby Mode

There are two ways to implement the standby mode on the device, one using both the $\overline{CE}$ and $\overline{RESET}$ pins, and the other via the $\overline{RESET}$ pin only.

When using both pins, CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ input held at V_{CC} ±0.3 V. Under this condition the current consumed is less than 5 µA Max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even when $\overline{CE}$ = "H". The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, CMOS standby mode is achieved with $\overline{RESET}$ input held at V_{SS} ±0.3 V ($\overline{CE}$ = "H" or "L") . Under this condition the current consumed is less than 5 µA Max. Once the $\overline{RESET}$ pin is set high, the device requires t_{RH} as a wake-up time for output to be valid for read access.

During standby mode, the output is in the high impedance state, regardless of $\overline{OE}$ input.

Automatic Sleep Mode

Automatic sleep mode works to restrain power consumption during read-out of device data. It can be useful in applications such as handy terminal, which requires low power consumption.

To activate this mode, the device automatically switch themselves to low power mode when the device addresses remain stable after 30 ns from data valid. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ in this mode. The current consumed is typically 1 µA (CMOS Level).

Since the data are latched during this mode, the data are continuously read out. When the addresses are changed, the mode is automatically canceled and the device read-out the data for changed addresses.

Autoselect

The Autoselect mode allows reading out of a binary code and identifies its manufacturer and type.It is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling A_0. All addresses can be either High or Low except A_6, A_3,A_2,A_1 and A_0. See "MBM29PL64LM User Bus Operations (Word Mode : BYTE = VIH)" and "MBM29PL64LM User Bus Operations (Byte Mode : BYTE = VIL)" in ■DEVICE BUS OPERATION.

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in "MBM29PL64LM Standard Command Definitions" in ■DEVICE BUS OPERATION.Refer to Autoselect Command section.

In Word mode, a read cycle from address 00h returns the manufacturer's code (Fujitsu = 04h) . A read cycle at address 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at addresses of 0Eh and 0Fh. Notice that the above applies to Word mode. The addresses and codes differ from those of Byte mode. Refer to "Sector Group Protection Verify Autoselect Codes" in ■DEVICE BUS OPERATION.

Read Mode

The device has two control functions required to obtain data at the outputs. $\overline{CE}$ is the power control and used for a device selection. $\overline{OE}$ is the output control and used to gate data to the output pins.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least t_{ACC}-t_{OE} time.) When reading out a data without changing addresses after power-up, input hardware reset or to change $\overline{CE}$ pin from "H" or "L".

Page Mode Read

The device is capable of fast read access for random locations within limited address location called Page. The Page size of the device is 8 bytes / 4 words, within the appropriate Page being selected by the higher address bits A_{21} to A_2 and the address bits A_1 to A_0 in Word mode (A_1 to A_{-1} in Byte mode) determining the specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The initial page access is equal to the random access (t_{ACC}) and subsequent Page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to the page address access time(t_{PACC}). Here again, $\overline{CE}$ selects the device and $\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected. Fast Page mode, accesses are obtained by keeping A_{20} to A_2 constant and changing A_1 and A_0 in Word mode (A_1 to A_{-1} in Byte mode) to select the specific word within that Page.

Output Disable

With the $\overline{OE}$ input at logic high level (V_{IH}), output from the devices are disabled. This may cause the output pins to be in a high impedance state.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the device function.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever starts later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever starts first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Group Protection

The device features hardware sector group protection. This feature will disable both program and erase operations in any combination of 38 sector groups of memory.See “Sector Group Address Table (MBM29PL64LM)” in ■DEVICE BUS OPERATION. The user‘s side can use the sector group protection using programming equipment. The device is shipped with all sector groups that are unprotected.

To activate it, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, $\overline{CE}$ = V_{IL} and $A_6 = A_3 = A_2 = A_0 = V_{IL}$, $A_1 = V_{IH}$. The sector group addresses (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, and A_{15}) should be set to the sector to be protected. “Sector Address Table (MBM29PL64LM)” in ■DEVICE BUS OPERATION defines the sector address for each of the seventy-one (71) individual sectors, and “Sector Group Address Table (MBM29PL64LM)” in ■DEVICE BUS OPERATION defines the sector group address for each of the twenty-four (24) individual group sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector group addresses must be held constant during the $\overline{WE}$ pulse. See “Sector Group Protection Timing Diagram” in ■TIMING DIAGRAM and “Sector Group Protection Algorithm” in ■FLOW CHART for sector group protection timing diagram and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector group addresses (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, and A_{15}) while (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) will produce a logical “1” code at device output DQ_0 for a protected sector. Otherwise the device will produce “0” for unprotected sectors. In this mode, the lower order addresses, except for A_0, A_1, A_2, A_3, and A_6 can be either High or Low. A_{-1} requires applying to V_{IL} on Byte mode.

Where the higher order addresses(A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, and A_{15}) are the desired sector group address will produce a logical “1” at DQ_0 for a protected sector group. See “Sector Group Protection Verify Autoselect Codes” in ■DEVICE BUS OPERATION for Autoselect codes.

Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the devices in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{\text{RESET}}$ pin to high voltage (V_{ID}). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{ID} is taken away from the $\overline{\text{RESET}}$ pin, all the previously protected sector groups will be protected again. Refer to “Temporary Sector Group Unprotection Timing Diagram” in ■TIMING DIAGRAM and “Temporary Sector Group Unprotection Algorithm” in ■FLOW CHART.

Hardware Reset

The devices may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL} from V_{IH}. The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least “t_{RP}” in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode “t_{READY}” after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the devices require an additional “t_{RH}” before it will allow read access. When the $\overline{\text{RESET}}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted.

Write Protect ($\overline{\text{WP}}$)

The Write Protection function provides a hardware method of protecting certain first 64K bytes words sectors without using V_{ID}. This function is one of two provided by the $\overline{\text{WP}}$/ACC pin.

If the system asserts V_{IL} on the $\overline{\text{WP}}$/ACC pin, the device disables program and erase functions in the first 64K bytes / 32K words sectors independently of whether this sector was protected or unprotected using the method described in “Sector Group Protection" above.

If the system asserts V_{IH} on the $\overline{\text{WP}}$/ACC pin, the device reverts of whether the outermost 8K bytes / 4K words sectors were last set to be protected to the unprotected status. Sector protection or unprotection for this sector depends on whether this was last protected or unprotected using the method described in “Sector protection/ unprotection”.

Accelerated Program Operation

The device offers accelerated program operation which enables programming in high speed. If the system asserts V_{ACC} to the $\overline{\text{WP}}$/ACC pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 85%. This function is primarily intended to allow high speed programing, so caution is needed as the sector group becomes temporarily unprotected.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device is automatically set to fast mode. Therefore, the present sequence could be used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the $\overline{\text{WP}}$/ACC pin returns the device to normal operation. Do not remove V_{ACC} from the $\overline{\text{WP}}$/ ACC pin while programming. See “Accelerated Program Timing Diagram” in ■TIMING DIAGRAM.

Enhanced V_{CCQ} Feature

The output voltage generated on the device is determined based on the V_{CCQ} level. This feature allows the device to operate in mixed-voltage environments, driving and receiving signals to and from other devices on the same bus.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. “MBM29PL64LM Standard Command Definitions” in ■DEVICE BUS OPERATION shows the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0h) and Program Resume (30h) commands are valid only while the Program operation is in progress.Moreover Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands must be asserted to DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Read mode, the Reset operation is initiated by writing the Reset command sequence into the command register. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically be in the reset state after power-up. In this case, a command sequence is not required in order to read data.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. Therefore, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However applying high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated first by writing two unlock cycles. This is followed by a third write cycle that contains the address and the Autoselect command. Then the manufacture and device codes can be read from the address, and an actual data of memory cell can be read from the another address.

Following the command write, a read cycle from address 00h returns the manufactures’s code (Fujitsu = 04h). A read cycle at address 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at address of 0Eh as well as at 0Fh. Notice that above applies to Word mode. The addresses and codes differ from those of Byte mode. Refer to “Sector Group Protection Verify Autoselect Codes” in ■DEVICE BUS OPERATION.

To terminate the operation, it is necessary to write the Reset command into the register. To execute the Autoselect command during the operation, Reset command must be written before the Autoselect command.

Programming

The devices are programmed on a word-by-word basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) starts programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling), DQ_6 (Toggle Bit) or RY/$\overline{BY}$. The $\overline{Data}$ Polling and Toggle Bit are automatically performed at the memory location being programmed.

The programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which the devices return to the read mode and plogram addresses are no longer latched. Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance. Hence $\overline{Data}$ Polling requires the same address which is being programmed.

If hardware reset occurs during the programming operation, the data being written is not guaranteed.

Programming is allowed in any address sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may result in either failure condition or an apparent success according to the data polling algorithm. But a read from Reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Note that attempting to program a “1” over a “0” will result in programming failure. This precaution is the same with Fujitsu standard NOR devices. “Embedded Program™ Algorithm” in ■FLOW CHART illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Program Suspend/Resume

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any address. Writing the Program Suspend command (B0h) during Embedded Program operation immediately suspends the programming. Refer to "Erase Suspend/Resume" for the detail.

When the Program Suspend command is written during a programming process, the device halts the program operation within 1us and updates the status bits.After the program operation has been suspended, the system can read data from any address. The data at program-suspended address is not valid. Normal read timing and command definitions apply.

After the Program Resume command (30h) is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information. When issuing program suspend command in 4 μs after issuing program command, determine the status of program operation by reading status bit at more 4 μs after issuing program resume command.

The system also writes the Autoselect command sequence in the Program Suspend mode. The device allows reading Autoselect codes at the addresses within programming sectors, since the codes are not stored in the memory. When the device exits the Autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Program Resume command to exit from the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming. Do not read CFI code after HiddenROM Entry and Exit in program suspend mode.

Write Buffer Programming Operations

Write Buffer Programming allows the system write to series of 16 words in one programming operation. This results in faster effective word programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle selecting the Sector Address in which programming will occur. In forth cycle contains both Sector Address and unique code for data bus width will be loaded into the page buffer at the Sector Address in which programming will occur.

The system then writes the starting address/data combination. This “starting address” must be the same Sector Address used in third and fourth cycles and its lower addresses of A_3 to A_0 should be 0h. All subsequent address must be incremented by 1. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) starts programming. Upon executing the Write Buffer Programming Operations command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

DQ_7($\overline{Data}$ Polling), DQ_6(Toggle Bit), DQ_5(Exceeded Timing Limits), DQ_1(Write-to-Buffer Abort) should be monitored to determine the device status during Write Buffer Programming. In addition to these functions, it is also possible to indicate to the host system that Write Buffer Programming Operations are either in progress or have been completed by RY/$\overline{BY}$. See “Hardware Sequence Flags”.

The $\overline{Data}$ polling techniques described in “$\overline{Data}$ Polling Algorithm” in ■FLOW CHART should be used while monitoring the last address location loaded into the write buffer. In addition, it is not neccessary to specify an address in Toggle Bit techniques described in “Toggle Bit Algorithm” in ■FLOW CHART. The automatic pro-

graming operation is completed when the data on DQ7 is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (See "Hardware Sequence Flags").

The write-buffer programming operation can be suspended using the standard program suspend/resume commands.

Once the write buffer programming is set, the system must then write the “Program Buffer to Flash” command at the Sector Address. Any other address/data combination will abort the Write Buffer Programming operation and the device will continue busy state.

The Write Buffer Programming Sequence can be ABORTED by doing the following :

- Different Sector Address is asserted.
- Write data other than the “Program Buffer to Flash" command after the specified number of “data load” cycles.

A “Write-to-Buffer-Abort Reset” command sequence must be written to the device to return to read mode. (See “MBM29PL64LM Standard Command Definitions” in ■DEVICE BUS OPERATION for details on this command sequence.)

Chip Erase

Chip erase is a six bus cycle operation. It begins two “unlock” write cycles followed by writing the “set-up” command, and two “unlock” write cycles followed by the chip erase command which invokes the Embedded Erase algorithm.

The device does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm the devices automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The system can determine the erase operation status by using DQ_7 ($\overline{\text{Data}}$ Polling), DQ_6 (Toggle Bit I) and DQ_2 (Toggle Bit II) or RY/$\overline{\text{BY}}$ output signal. The chip erase begins on the rising edge of the last $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first from last command sequence and completes when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device returns to read mode.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command.

Multiple sectors may be erased concurrently by writing the same six bus cycle operations. This sequence is followed by writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than Erase Time-out time(t_{TOW}). Otherwise that command will not be accepted and erasure will not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can reoccur after the last Sector Erase command is written. A time-out of “t_{TOW}” from the rising edge of last $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first, will initiate the execution of the Sector Erase command(s). If another falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first occurs within the “t_{TOW}” time-out window the timer is reset (monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer). Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete (refer to the Write Operation Status). Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 127).

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector(s) to be erased prior to electrical erase using the Embedded Erase Algorithm. When erasing a sector, the remaining unselected sectors remain unaffected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling), DQ_6 (Toggle Bit) or RY/$\overline{\text{BY}}$.

The sector erase begins after the “t_{TOW}” time-out from the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever happens first for the last sector erase command pulse and completes when the data on DQ_7 is “1” (see Write Operation Status

section), at which the devices return to the read mode. $\overline{\text{Data}}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt Sector Erase operation and then perform read to a sector not being erased. This command is applicable ONLY during the Sector Erase operation within the time-out period for sector erase. Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the "Erase Resume" command (30h) resumes the erase operation.

When the "Erase Suspend" command is written during the Sector Erase operation, the device takes maximum of "t_{SPD}" to suspend the erase operation. When the devices enter the erase-suspended mode, the RY/$\overline{\text{BY}}$ output pin will be at High-Z and the DQ_7 bit will be at logic "1" and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation is suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode, except that the data must be read from sectors that have not been erase-suspended. Reading successively from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. See the section on DQ_2.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Do not issuing program command after entering erase-suspend-read mode.

Fast Mode Set/Reset

The device has Fast Mode function. It dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming consists of two cycles instead of four bus cycles in standard program command. The read operation is also executed after exiting this mode. During the Fast mode, do not write any command other than the Fast program/Fast mode reset command. To exit from this mode, write Fast Mode Reset command into the command register. (Refer to the "Embedded Program™ Algorithm for Fast Mode" in ■FLOW CHART.) The V_{CC} active current is required even $\overline{\text{CE}}$ = V_{IH} during Fast Mode.

Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). See "Embedded Program™ Algorithm for Fast Mode" in ■FLOW CHART.

Extended Sector Group Protection

In addition to normal sector group protection, the device has Extended Sector Group Protection as extended function. This function enables protection of the sector group by forcing V_{ID} on $\overline{RESET}$ pin and writes a command sequence. Unlike conventional procedures, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then the sector group addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16} and A_{15}) and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) should be set to the sector group to be protected (set V_{IL} for the other addresses pins is recommended), and write extended sector group protection command (60h). A sector group is typically protected in 250 μs. To verify programming of the protection circuitry, the sector group addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16} and A_{15}) and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) should be set and write a command (40h). Following the command write, a logical "1" at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical "0", write the extended sector group protection command (60h) again. To terminate the operation, set $\overline{RESET}$ pin to V_{IH}. (Refer to the "Extended Sector Group Protection Timing Diagram" in ■TIMING DIAGRAM and "Extended Sector Group Protection Algorithm" in ■FLOW CHART.)

Query Command (CFI : Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrieves device information. Please note that output data of upper byte (DQ_{15} to DQ_8) is "0". Refer to the CFI code table. To terminate operation, it is necessary to write the Reset command sequence into the register. (See "Common Flash Memory Interface Code" in ■DEVICE BUS OPERATION.)

HiddenROM Mode

(1) HiddenROM Region

The HiddenROM (HiddenROM) feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the HiddenROM region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.

The HiddenROM region is 256 bytes / 128 words in length. After the system writes the HiddenROM Entry command sequence, it may read the HiddenROM region by using device addresses A_6 to A_0 (A_{21} to A_{15} are all "0"). That is, the device sends only program command that would normally be sent to the address to the HiddenROM region. This mode of operation continues until the system issues the Exit HiddenROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the address.

If you request Fujitsu to program the ESN in the device, please contact a Fujitsu representative for more information.

(2) HiddenROM Entry Command

The device has a HiddenROM area with One Time Protect function. This area is to enter the security code and to unable the change of the code once set. Programming is allowed in this area until it is protected. However, once it gets protected, it is impossible to unprotect. Therefore, extreme caution is required.

The HiddenROM area is 256 bytes / 128 words. This area is in SA0 . Therefore, write the HiddenROM entry command sequence to enter the HiddenROM area. It is called HiddenROM mode when the HiddenROM area appears.

Sectors other than the block area SA0 can be read during HiddenROM mode. Read/program of the HiddenROM area is possible during HiddenROM mode. Write the HiddenROM reset command sequence to exit the HiddenROM mode. Note that any other commands should not be issued than the HiddenROM program/protection/reset commands during the HiddenROM mode. When you issue the other commands including the suspend resume capability, send the HiddenROM reset command first to exit the HiddenROM mode and then issue each command.

(3) HiddenROM Program Command

To program the data to the HiddenROM area, write the HiddenROM program command sequence during HiddenROM mode. This command is the same as the usual program command, except that it needs to write the command during HiddenROM mode. Therefore the detection of completion method is the same as in the past, using the DQ_7 data pooling, DQ_6 Toggle bit or RY/$\overline{BY}$. You should pay attention to the address to be programmed. If an address not in the HiddenROM area is selected, the previous data will be deleted.
During the write into the HiddenROM region, the program suspend command issuance is prohibited.

(4) HiddenROM Protect Command

There are two methods to protect the HiddenROM area. One is to write the sector group protect setup command (60h) , set the sector address in the HiddenROM area and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) , and write the sector group protect command (60h) during the HiddenROM mode. The same command sequence may be used because it is the same as the extension sector group protect in the past, except that it is in the HiddenROM mode and does not apply high voltage to the $\overline{RESET}$ pin. Please refer to above mentioned “Extended Sector Group Protection” for details of sector group protect setting.
The other method is to apply high voltage (V_{ID}) to A_9 and $\overline{OE}$, set the sector address in the HiddenROM area and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) , and apply the write pulse during the HiddenROM mode. To verify the protect circuit, apply high voltage (V_{ID}) to A_9, specify (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) and the sector address in the HiddenROM area, and read. When “1” appears on DQ_0, the protect setting is completed. “0” will appear on DQ_0 if it is not protected. Apply write pulse again. The same command sequence could be used for the above method because other than the HiddenROM mode, it is the same as the sector group protect previously mentioned.

Take note that other sector groups will be affected if an address other than those for the HiddenROM area is selected for the sector group address, so please be careful. Pay close attention that once it is protected, protection CANNOT BE CANCELLED.

Write Operation Status

Detailed in “Hardware Sequence Flags” are all the status flags which can determine the status of the device for current mode operation. When checking Hardware Sequence Flags during program operation, it should be checked 4 μs after issuing program command. During sector erase, the part provides the status flags automatically to the I/O ports. The information on DQ_2 is address sensitive. If an address from an erasing sector is consecutively read, then the DQ_2 bit will toggle. However DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows the user to determine which sectors are erasing.

Once erase suspend is entered address sensitivity still applies. If the address of a non-erasing sector (one available for read) is provided, then stored data can be read from the device. If the address of an erasing sector (one unavailable for read) is applied, the device will output its status bits.

Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2	DQ_1*3
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle*1	N/A
	Program Suspend Mode	Program-Suspend-Read (Program Suspended Sector)	Data	Data	Data	Data	Data	Data
		Program-Suspend-Read (Non-Program Suspended Sector)	Data	Data	Data	Data	Data	Data
	Erase Suspend Mode	Erase-Suspend-Read (Erase Suspended Sector)	1	1	0	0	Toggle*1	N/A
		Erase-Suspend-Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	Data
		Erase-Suspend-Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1*2	N/A
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1	N/A
	Embedded Erase Algorithm		0	Toggle	1	1	N/A	N/A
	Erase Suspend Mode	Erase-Suspend-Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A	N/A
Write to Buffer*4	BUSY State		$\overline{DQ_7}$	Toggle	0	N/A	N/A	0
	Exceeded Timing Limits		$\overline{DQ_7}$	Toggle	1	N/A	N/A	0
	ABORT State		N/A	Toggle	0	N/A	N/A	1

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle.

*2 : Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

*3 : DQ_1 indicates the Write-to-Buffer ABORT status during Write-Buffer-Programming operations.

*4 : The $\overline{Data}$ Polling algorithm detailed in “$\overline{Data}$ Polling Algorithm” in ■FLOW CHART should be used for Write-Buffer-Programming operations. Note that $\overline{DQ_7}$ during Write-Buffer-Programming indicates the data-bar for DQ_7 data for the LAST LOADED WRITE-BUFFER ADDRESS location.

DQ_7

$\overline{\text{Data}}$ Polling

The devices feature $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read devices will produce reverse data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read device will produce a "1" at the DQ_7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in "$\overline{\text{Data}}$ Polling Algorithm" in ■FLOW CHART.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector addresses of sectors being erased, not protected sectors. Otherwise, the status may become invalid.

If a program address falls within a protected sector, Data polling on DQ7 is active for approximately 1 μs, then the device returns to read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ_7 is active for approximately 100 μs, then the device returns to read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ_7 at one instant of time, and then that byte's valid data the next. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device completes the Embedded Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_6 to DQ_0 may still be invalid. The valid data on DQ_7 to DQ_0 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erace Suspendmode or sector erase time-out.

See "$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram" in ■TIMING DIAGRAM for the $\overline{\text{Data}}$ Polling timing specifications and diagram.

DQ_6

Toggle Bit I

The device also feature the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling) data from the devices will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequences. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequences. The Toggle Bit I is active during the sector time out.

In programm operation, if the sector being written to is protected, the Toggle bit will toggle for about 1 μs and then stop toggling with the data unchanged. In erase, the device will erase all the selected sectors except for the protected ones. If all selected sectors are protected, the chip will toggle the Toggle bit for about 100 μs and then drop back into read mode, having data kept remained.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ_6 to toggle. See "Toggle Bit I Timing Diagramduring Embedded Algorithm Operations" in ■TIMING DIAGRAM for the Toggle Bit I timing specifications and diagram.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a “1”. This is a failure condition indicating that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in “MBM29PL64LM User Bus Operations (Word Mode : $\overline{\text{BYTE}}$ = V_{IH})” and “MBM29PL64LM User Bus Operations (Byte Mode : $\overline{\text{BYTE}}$ = V_{IL})” in ■DEVICE BUS OPERATION.

The DQ_5 failure condition may also appear if a user tries to program a non blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 bit and DQ_6 never stop toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a “1”. Note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device with command sequence.

DQ_3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates a valid erase command has been written, DQ_3 may be used to determine whether the sector erase timer window is still open. If DQ_3 is “1” the internally controlled erase cycle has begun. If DQ_3 is “0”, the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See “Hardware Sequence Flags”.

DQ_2

Toggle Bit II

This Toggle bit II, along with DQ_6, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the non-erase suspended sector will indicate a logic “1” at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows:

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also “Hardware Sequence Flags” and “DQ_2 vs. DQ_6” in ■TIMING DIAGRAM.

Furthermore, DQ_2 can also be used to determine which sector is being erased. At the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Reading Toggle Bits DQ_6 / DQ_2

Whenever the system initially begins reading Toggle bit status, it must read DQ_7 to DQ_0 at least twice in a row to determine whether a Toggle bit is toggling. Typically a system would note and store the value of the Toggle bit after the first read. After the second read, the system would compare the new value of the Toggle bit with the first. If the Toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ_7 to DQ_0 on the following read cycle.

However, if, after the initial two read cycles, the system determines that the Toggle bit is still toggling, the system also should note whether the value of DQ_5 is high (see the section on DQ_5) . If it is, the system should then determine again whether the Toggle bit is toggling, since the Toggle bit may have stopped toggling just as DQ_5 went high. If the Toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the Toggle bit is toggling and DQ_5 has not gone high. The system may continue to monitor the Toggle bit and DQ_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to “Toggle Bit Algorithm” in ■FLOW CHART.)

Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle *1
Erase-Suspend-Read (Erase-Suspended Sector)	1	1	Toggle *1
Erase-Suspend-Program	$\overline{DQ_7}$	Toggle	1 *2

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle.

*2 : Reading from the non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

DQ_1

Write-to-Buffer Abort

DQ_1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ_1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See "Write Buffer Programming Operations" section for more details.

RY/$\overline{BY}$

Ready/Busy

The device provides a RY/$\overline{BY}$ open-drain output pin to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. If the device is placed in an Erase Suspend mode, the RY/$\overline{BY}$ output will be high, by means of connecting with a pull-up resister to V_{CC}.

During programming, the RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth $\overline{WE}$ pulse. During an erase operation, the RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth $\overline{WE}$ pulse. The RY/$\overline{BY}$ pin will indicate a busy condition during the $\overline{RESET}$ pulse. See “RY/$\overline{BY}$ Timing Diagram during Program/Erase Operation Timing Diagram” and “RESET Timing Diagram (During Embedded Algorithms)” in ■TIMING DIAGRAM for a detailed timing diagram. The RY/$\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

Word/Byte Configuration

$\overline{BYTE}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the device. When this pin is driven high, the device operates in the word (16-bit) mode. Data is read and programmed at DQ_{15} to DQ_0. When this pin is driven low, the device operates in byte (8-bit) mode. In this mode, DQ_{15}/A_{-1} pin becomes the lowest address bit, and DQ_{14} to DQ_8 bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically reset the internal state machine in Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

(1) Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO}. If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO}.

If Embedded Erase Algorithm is interrupted, the intervened erasing sector(s) is(are) not valid.

(2) Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

(3) Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

(4) Power-up Write Inhibit

Power-up of the devices with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to read mode on power-up.

(5) Sector Protection

Device user is able to protect each sector group individually to store and protect data. Protection circuit voids both write and erase commands that are addressed to protected sectors.
Any commands to write or erase addressed to protected sector are ignored .

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–20	+85	°C
Voltage with Respect to Ground All Pins Except A_9, $\overline{OE}$, and $\overline{RESET}$ *1,*2	V_{IN}, V_{OUT}	–0.5	V_{CC} +0.5	V
Power Supply Voltage *1	V_{CC}	–0.5	+4.0	V
A_9, $\overline{OE}$, and $\overline{RESET}$ *1,*3	V_{IN}	–0.5	+12.5	V
$\overline{WP}$/ACC *1,*3	V_{ACC}	–0.5	+12.5	V

*1 : Voltage is defined on the basis of VSS = GND = 0 V.

*2 : Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –0.2 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns

*3 : Minimum DC input voltage is –0.5 V. During voltage transitions, these pins may undershoot V_{SS} to –0.2 V for periods of up to 20 ns.Voltage difference between input and supply voltage (V_{IN}–V_{CC}) dose not exceed to +9.0 V. Maximum DC input voltage is +12.5 V which may overshoot to +14.0 V for periods of up to 20 ns .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES*1

Parameter		Symbol	Value		Unit
			Min	Max	
Ambient Temperature	90	T_A	–20	+70	°C
	10		–20	+85	
V_{CC} Supply Voltage *2, *3		V_{CC}	+3.0	+3.6	V
V_{CCQ} Supply Voltage *2, *3 *4		V_{CCQ}	V_{CC}		V

*1 : Operating ranges define those limits between which the functionality of the device is guaranteed.

*2 : Voltage is defined on the basis of V_{SS} = GND = 0 V.

*3 : V_{CC} and V_{CCQ} supply voltage must be on the same level.

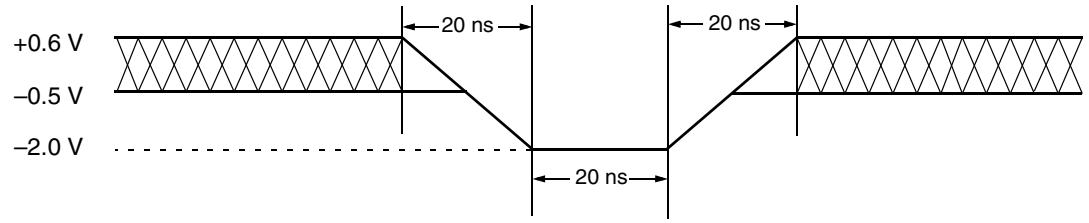
*4 : V_{CCQ} supply voltage is only for MBM29PL64LMxxPCN : 56 pin TSOP

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

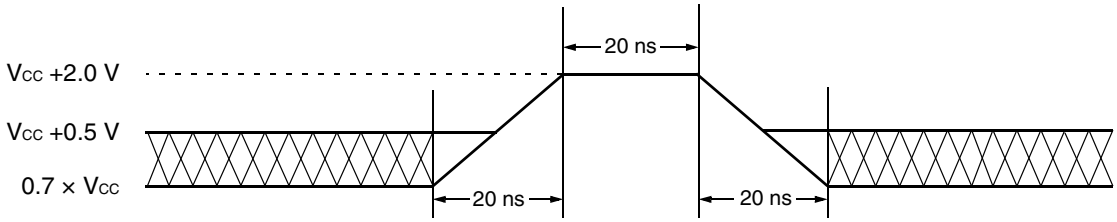
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

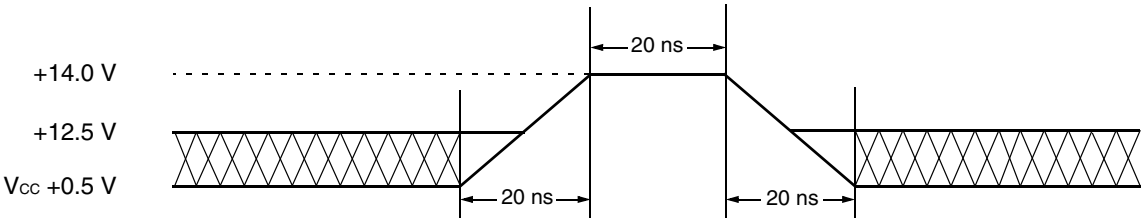
■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT



Maximum Undershoot Waveform



Maximum Overshoot Waveform 1



Note: This waveform is applied for A_9, $\overline{OE}$, $\overline{RESET}$, and A_{CC}.

Maximum Overshoot Waveform 2

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max	$\overline{WP}$/ACC pin	–2.0	—	+2.0	µA
			Others	–1.0	—	+1.0	
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max		–1.0	—	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	V_{CC} = V_{CC} Max, A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	—	35	µA
V_{CC} Active Current (Read) *1,*2	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz	Word	—	15	25	mA
			Byte	—	15	25	
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 10 MHz	Word	—	35	50	
			Byte	—	35	50	
V_{CC} Active Current (Intra-Page Read) *2	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, t_{PRC} = 25 ns, 4-Word		—	10	20	mA
V_{CC} Active Current (Program / Erase) *2,*3	I_{CC3}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	50	60	mA
V_{CC} Standby Current *2	I_{CC4}	$\overline{CE}$ = V_{CC} ±0.3 V, $\overline{RESET}$ = V_{CC} ±0.3 V, $\overline{OE}$ = V_{IH}, $\overline{WP}$/ACC = V_{CC} ±0.3 V		—	1	5	µA
V_{CC} Reset Current *2	I_{CC5}	$\overline{RESET}$ = V_{CC} ±0.3 V, $\overline{WP}$/ACC = V_{CC} ±0.3 V		—	1	5	µA
V_{CC} Automatic Sleep Current *4	I_{CC6}	$\overline{CE}$ = V_{SS} ±0.3 V, $\overline{RESET}$ = V_{CC} ±0.3 V, V_{IN} = V_{CC} ±0.3 V or V_{ss} ±0.3 V, $\overline{WP}$/ACC = V_{CC} ±0.3 V		—	1	5	µA
V_{CC} Active Current (Erase-Suspend-Program) *2	I_{CC7}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	50	60	mA
ACC Accelerated Program Current	I_{ACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Vcc = Vcc Max, $\overline{WP}$/ACC = V_{ACC} Max	$\overline{WP}$/ACC pin	—	—	45	mA
			Vcc Pin	—	—	60	
Input Low Level	V_{IL}	—		–0.5	—	0.6	V
Input High Level	V_{IH}	—		0.7×V_{CC}	—	V_{CC} + 0.3	V
Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Acceleration	V_{ACC}	V_{CC} = 3.0 V to 3.6 V		11.5	12.0	12.5	V
Voltage for Autoselect, and Temporary Sector Unprotected	V_{ID}	V_{CC} = 3.0 V to 3.6 V		11.5	12.0	12.5	V
Output Low Voltage Level	V_{OL}	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min		—	—	0.45	V
Output High Voltage Level	V_{OH}	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min		0.85×V_{CC}	—	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—		2.3	—	2.5	V

*1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : Maximum I_{CC} values are tested with $V_{CC} = V_{CC}$ Max, and $V_{CCQ} = V_{CCQ}$ Max.
V_{CCQ} is only for MBM29PL64LMxxPCN : 56 pin TSOP.

*3 : I_{CC} active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.

*4 : Automatic sleep mode enables the low power mode when address remain stable for t_{ACC} + 30 ns.

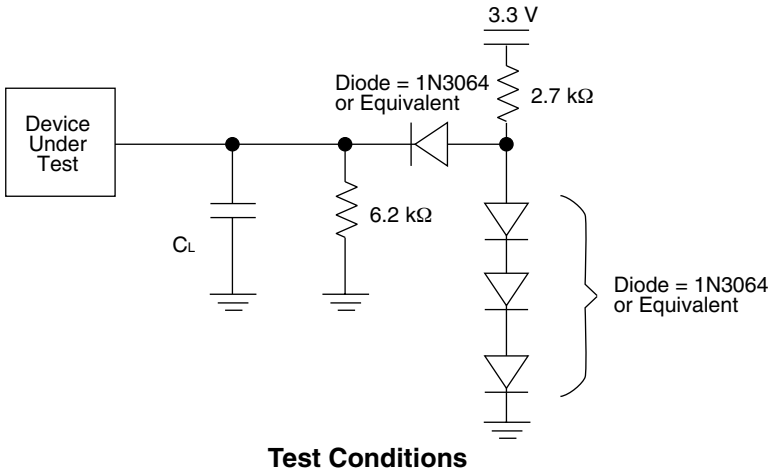
2. AC Characteristics

- Read Only Operations Characteristics

Parameter		Symbols		Condition	Value*				Unit
					90		10		
		JEDEC	Standard		Min	Max	Min	Max	
Read Cycle Time		t_{AVAV}	t_{RC}	—	90	—	100	—	ns
Address to Output Delay		t_{AVQV}	t_{ACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	—	90	—	100	ns
Chip Enable to Output Delay		t_{ELQV}	t_{CE}	$\overline{OE}$ = V_{IL}	—	90	—	100	ns
Page Read Cycle Time		—	t_{PRC}	—	25	—	30	—	ns
Page Address to Output Delay		—	t_{PACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	—	25	—	30	ns
Output Enable to Output Delay		t_{GLQV}	t_{OE}	—	—	25	—	30	ns
Chip Enable to Output High-Z		t_{EHQZ}	t_{DF}	—	—	25	—	30	ns
Output Enable Hold Time	Read	—	t_{OEH}	—	0	—	0	—	ns
	Toggle and $\overline{Data}$ Polling			—	10	—	10	—	ns
Output Enable to Output High-Z		t_{GHQZ}	t_{DF}	—	—	25	—	30	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		t_{AXQX}	t_{OH}	—	0	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode		—	t_{READY}	—	—	20	—	20	µs

* : Test Conditions :

Output Load : 1 TTL gate and 30 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V or V_{CC}
Timing measurement reference level
Input : V_{CC} / 2
Output : V_{CC} / 2



Test Conditions

• **Write (Erase/Program) Operations**

Parameter		Symbol		Value						Unit
				90			10			
		JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time		t_{AVAV}	t_{WC}	90	—	—	100	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		—	t_{ASO}	15	—	—	15	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	45	—	—	45	—	—	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling		—	t_{AHT}	0	—	—	0	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	35	—	—	35	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	0	—	—	ns
Output Enable Setup Time		—	t_{OES}	0	—	—	0	—	—	ns
$\overline{CE}$ High During Toggle Bit Polling		—	t_{CEPH}	20	—	—	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling		—	t_{OEPH}	20	—	—	20	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	ns
$\overline{CE}$ Setup Time		t_{ELWL}	t_{CS}	0	—	—	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	0			ns
$\overline{CE}$ Hold Time		t_{WHEH}	t_{CH}	0	—	—	0	—	—	ns
$\overline{WE}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	0	—	—	ns
$\overline{CE}$ Pulse Width		t_{ELEH}	t_{CP}	35	—	—	35	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	35	—	—	35	—	—	ns
$\overline{CE}$ Pulse Width High		t_{EHEL}	t_{CPH}	25	—	—	25	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	30	—	—	30	—	—	ns
Effective Page Programming Time (Write Buffer Programming)	Per Word	t_{WHWH1}	t_{WHWH1}	—	23.5	—	—	23.5	—	µs
Programming Time	Word			—	100	—	—	100	—	µs
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	1.0	—	—	1.0	—	s
V_{CC} Setup Time		—	t_{VCS}	50	—	—	50	—	—	µs
Recovery Time From RY/$\overline{BY}$		—	t_{PB}	0	—	—	0	—	—	ns
Erase/Program Valid to RY/$\overline{BY}$ Delay		—	t_{BUSY}	—	—	90	—	—	90	ns
Rise Time to V_{ID} *2		—	t_{VIDR}	500	—	—	500	—	—	ns
Rise Time to V_{ACC} *3		—	t_{VACCR}	500	—	—	500	—	—	ns
Voltage Transition Time *2		—	t_{VLHT}	4	—	—	4	—	—	µs

(Continued)

(Continued)

Parameter	Symbol		Value						Unit
			90			10			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Write Pulse Width *2	—	t_{WPP}	100	—	—	100	—	—	µs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{OESP}	4	—	—	4	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{CSP}	4	—	—	4	—	—	µs
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	—	500	—	—	ns
$\overline{RESET}$ High Time Before Read	—	t_{RH}	100	—	—	100	—	—	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	90	—	—	100	ns
Erase Time-out Time	—	t_{TOW}	50	—	—	50	—	—	µs
Erase Suspend Transition Time	—	t_{SPD}	—	—	20	—	—	20	µs

*1 : This does not include the preprogramming time.

*2 : This timing is for Sector Group Protection operation.

*3 : This timing is for Accelerated Program operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Remarks
	Min	Typ	Max		
Sector Erase Time	—	1	15	s	Excludes programming time prior to erasure
Programming Time	—	100	3000	µs	Excludes system-level overhead
Effective Page Programming Time (Write Buffer Programming)	—	23.5	—	µs	
Chip Programming Time	—	—	600	s	
Absolute Maximum Programming Time (16 words)	—	—	6	ms	Non programming within the same page
Erase/Program Cycle	100,000	—	—	cycle	—

■ TSOP (1) PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	8	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8.5	12	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8	10	pF
Reset pin and $\overline{WP}$/ACC Pin Capacitance	C_{IN3}	V_{IN} = 0	20	25	pF

Notes : • Test conditions T_A = +25°C, f = 1.0 MHz
• DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

■ FBGA PIN CAPACITANCE

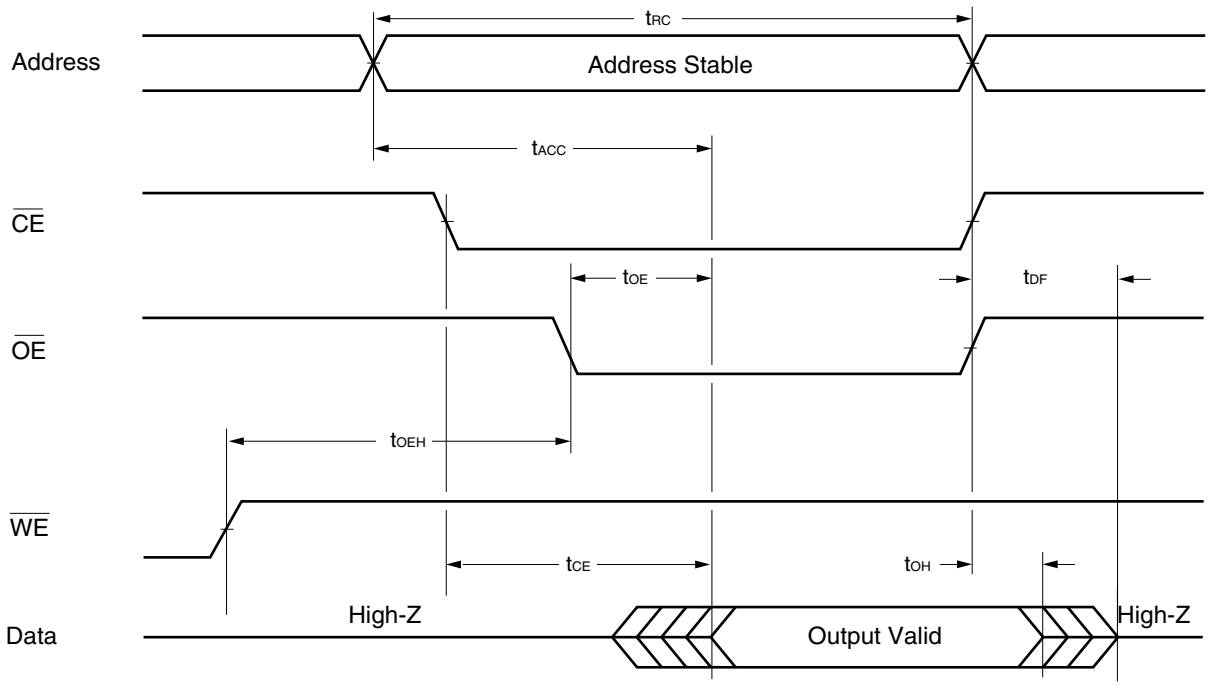
Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	8	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8.5	12	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8	10	pF
Reset pin and $\overline{WP}$/ACC Pin Capacitance	C_{IN3}	V_{IN} = 0	15	20	pF

Notes : • Test conditions T_A = +25°C, f = 1.0 MHz
• DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

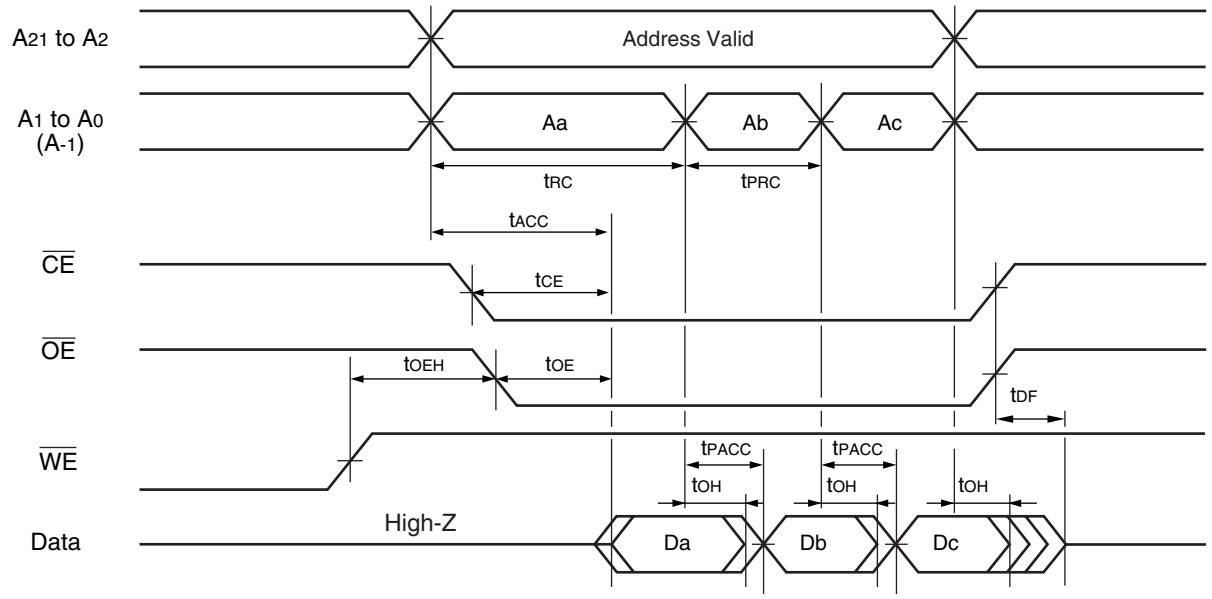
■ TIMING DIAGRAM

- **Key to Switching Waveforms**

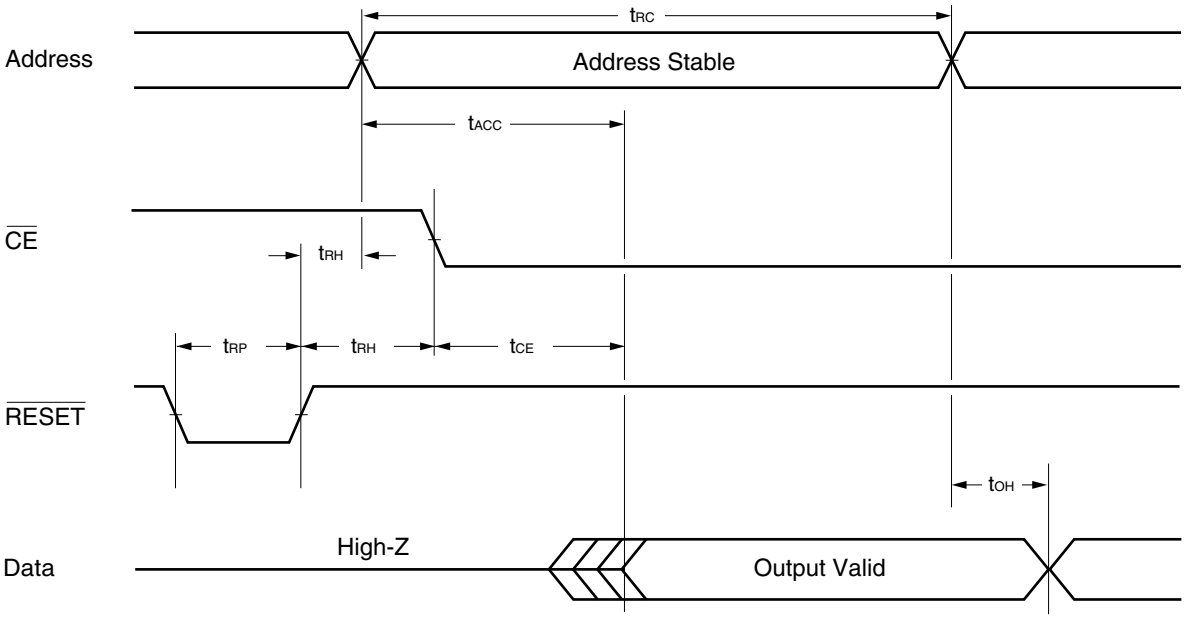
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	"H" or "L" Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State



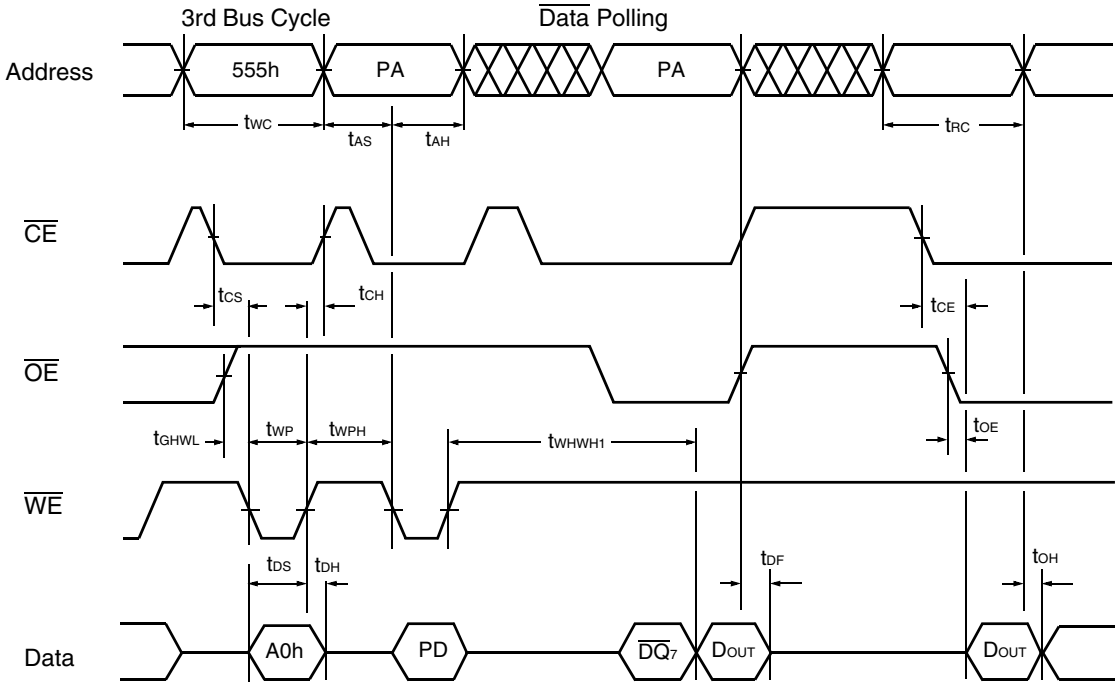
Read Operation Timing Diagram



Page Read Operation Timing Diagram

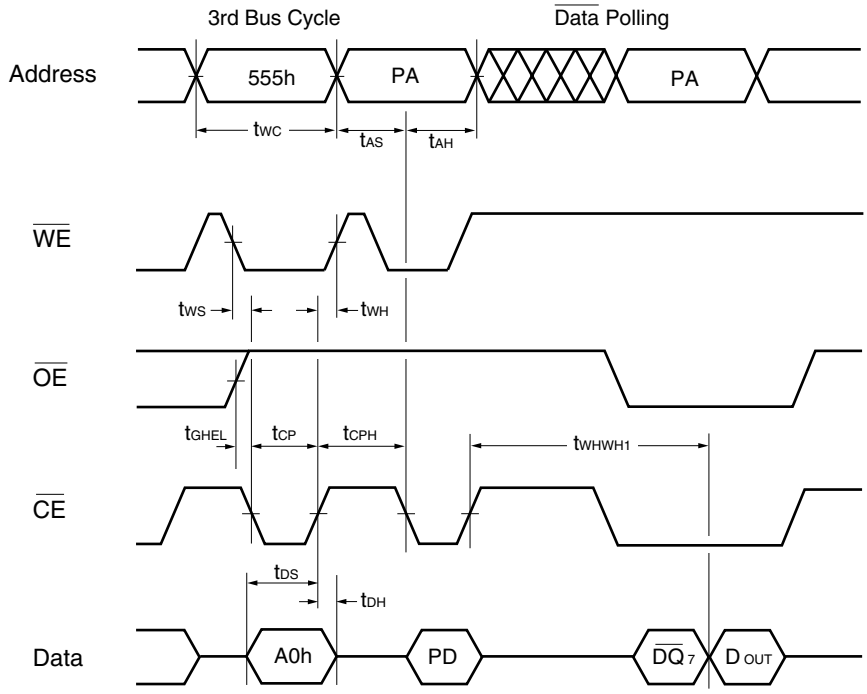


Hardware Reset/Read Operation Timing Diagram



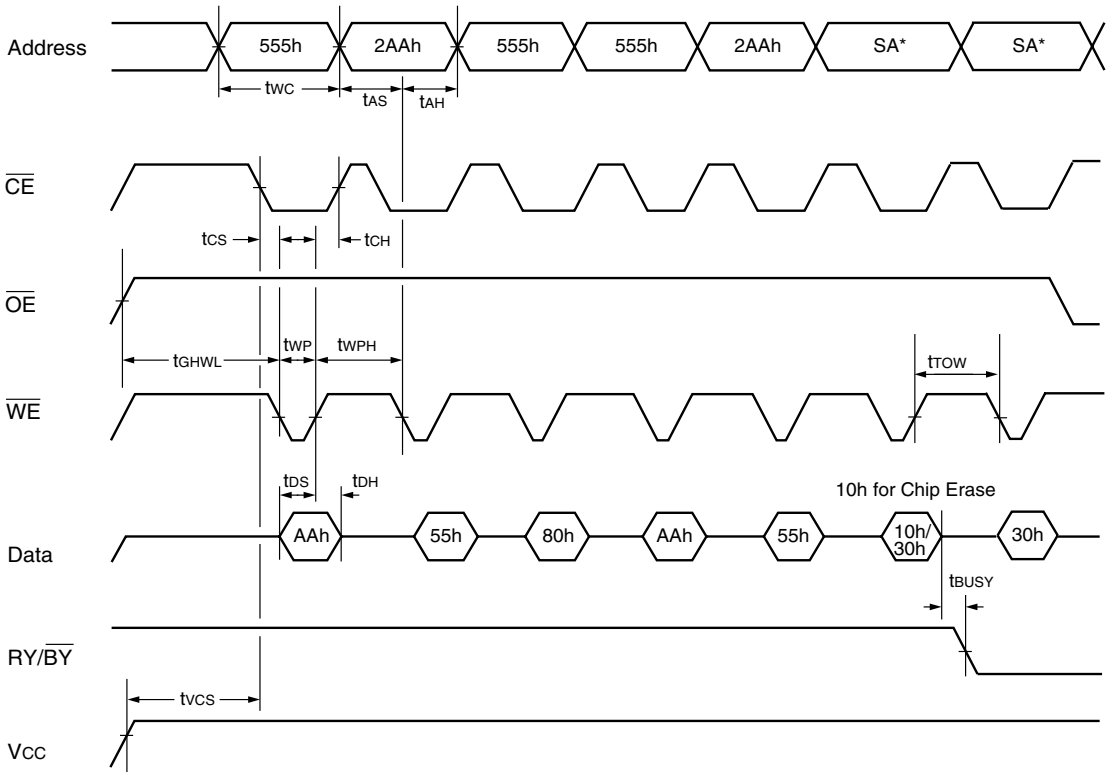
Notes : • PA is address of the memory location to be programmed.
• PD is data to be programmed at word address.
• $\overline{DQ_7}$ is the output of the complement of the data written to the device.
• D_{OUT} is the output of the data written to the device.
• Figure indicates the last two bus cycles out of four bus cycle sequence.

Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram



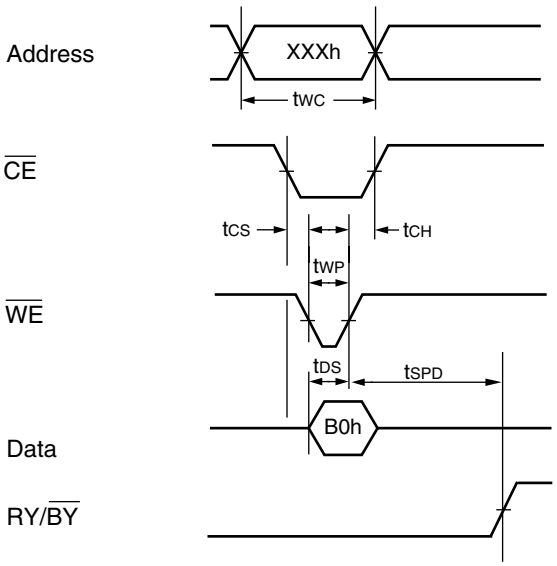
Notes : • PA is address of the memory location to be programmed.
• PD is data to be programmed at word address.
• $\overline{DQ_7}$ is the output of the complement of the data written to the device.
• D_{OUT} is the output of the data written to the device.
• Figure indicates the last two bus cycles out of four bus cycle sequence.

Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram

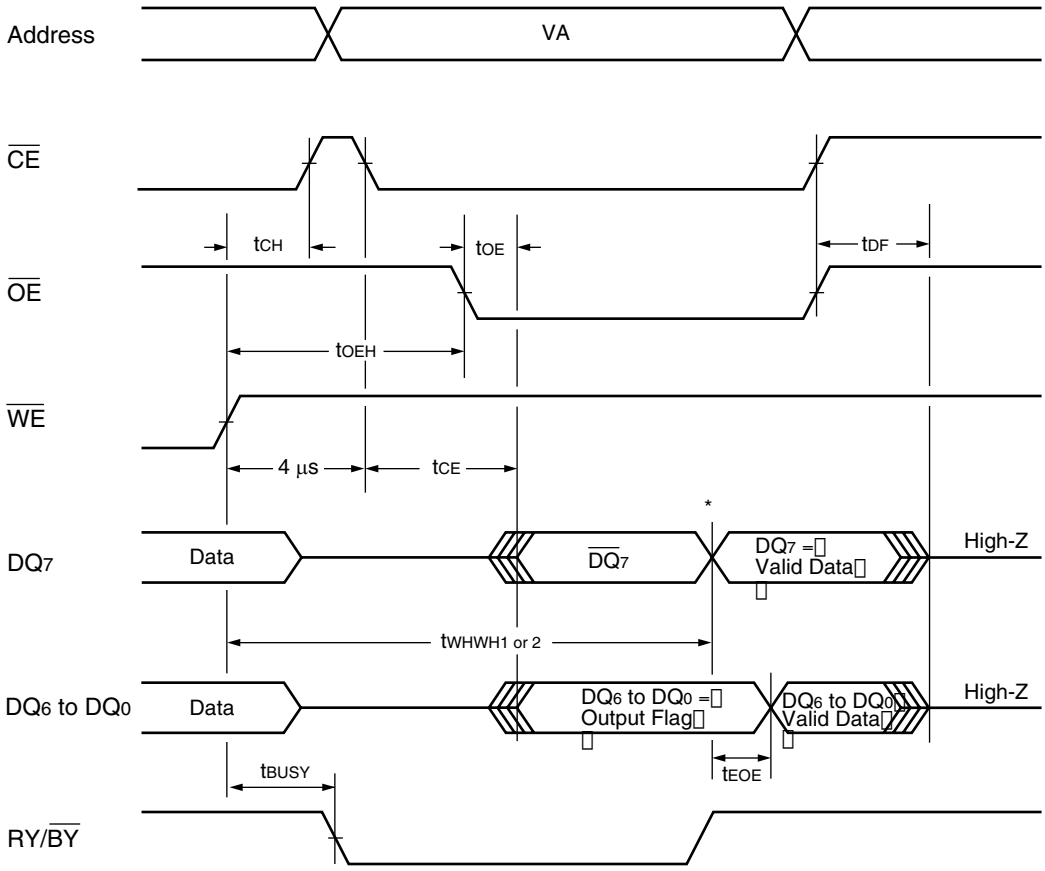


* : SA is the sector address for Sector Erase. Address = 555h (Word), AAAh (Byte) for Chip Erase.

Chip/Sector Erase Operation Timing Diagram



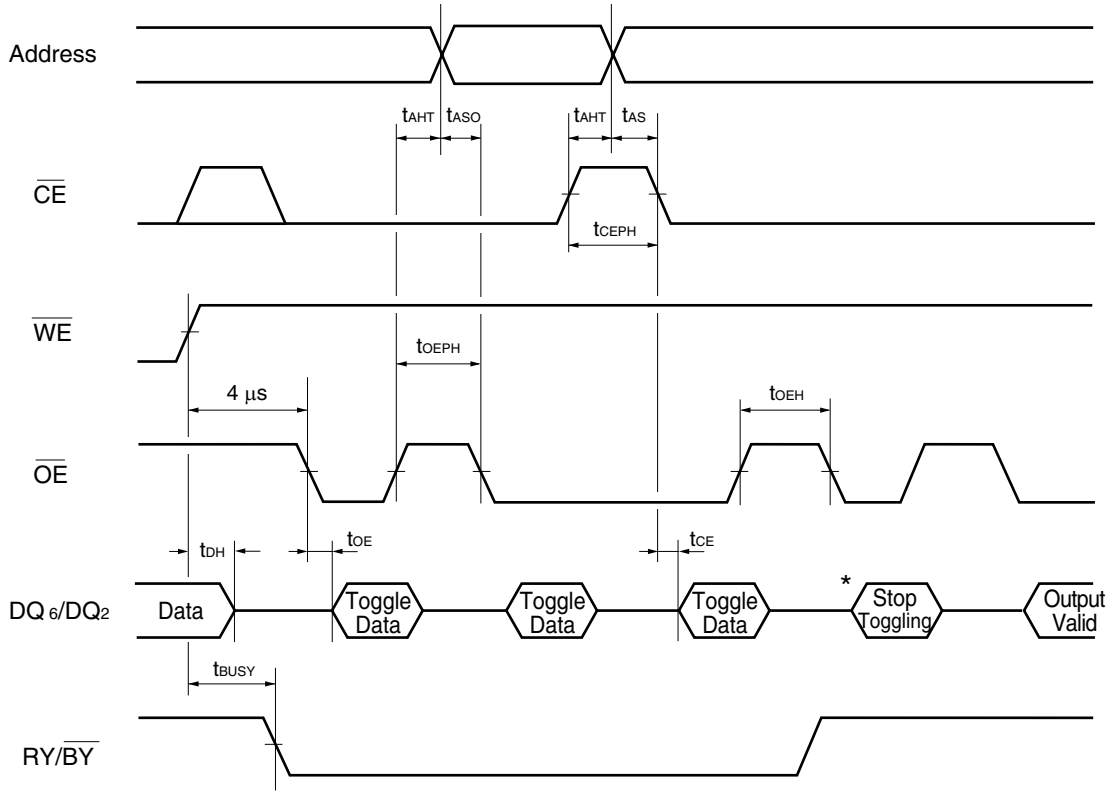
Erase Suspend Operation Timing Diagram



* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

Note : When checking Hardware Sequence Flags program operations, it should be checked 4 µs after issuing program command.

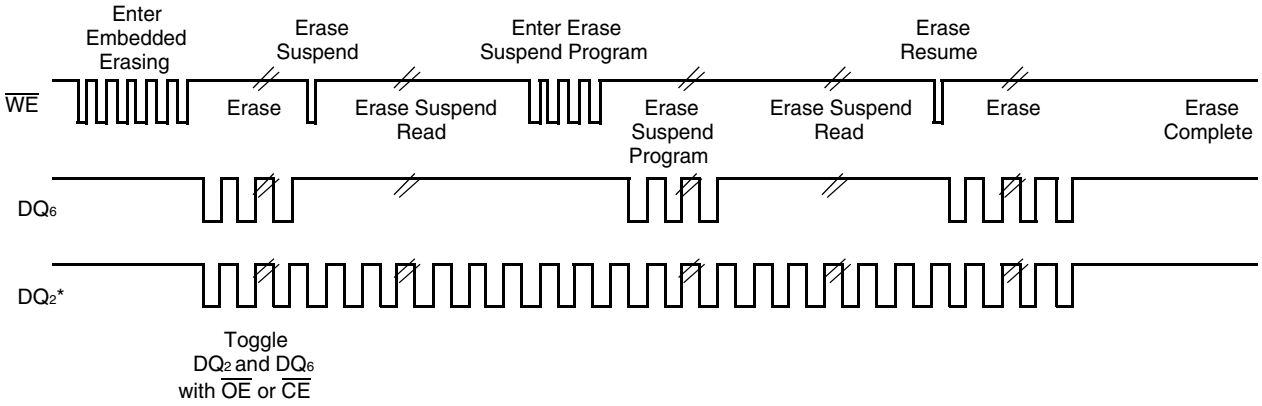
$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram



* : DQ_6 stops toggling (The device has completed the Embedded operation).

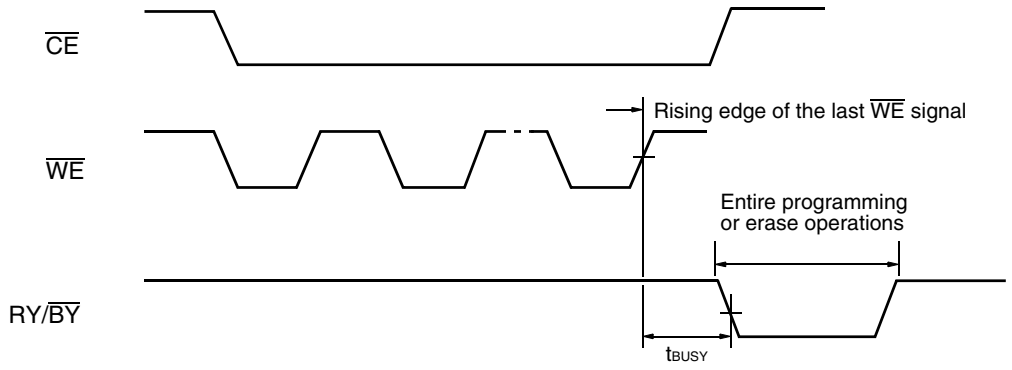
Note : When checking Hardware Sequence Flags program operations, it should be checked 4 µs after issuing program command.

Toggle Bit I Timing Diagram during Embedded Algorithm Operations

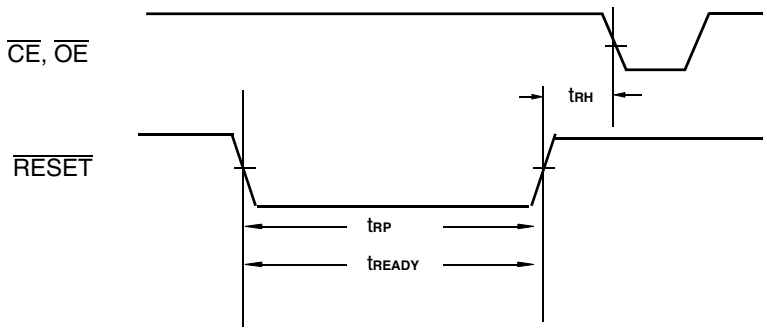


* : DQ_2 is read from the erase-suspended sector.

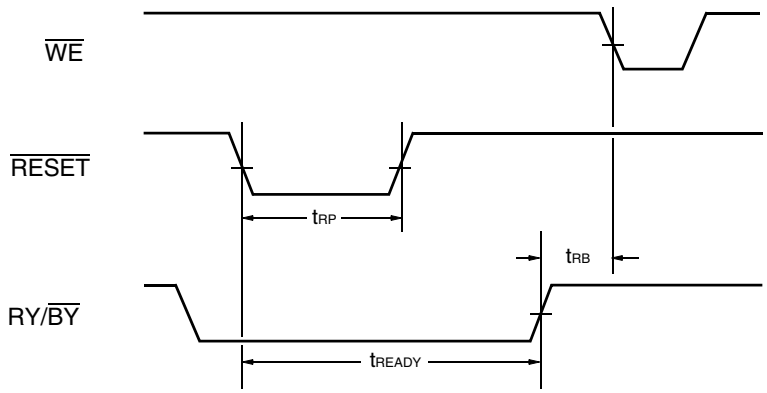
DQ_2 vs. DQ_6



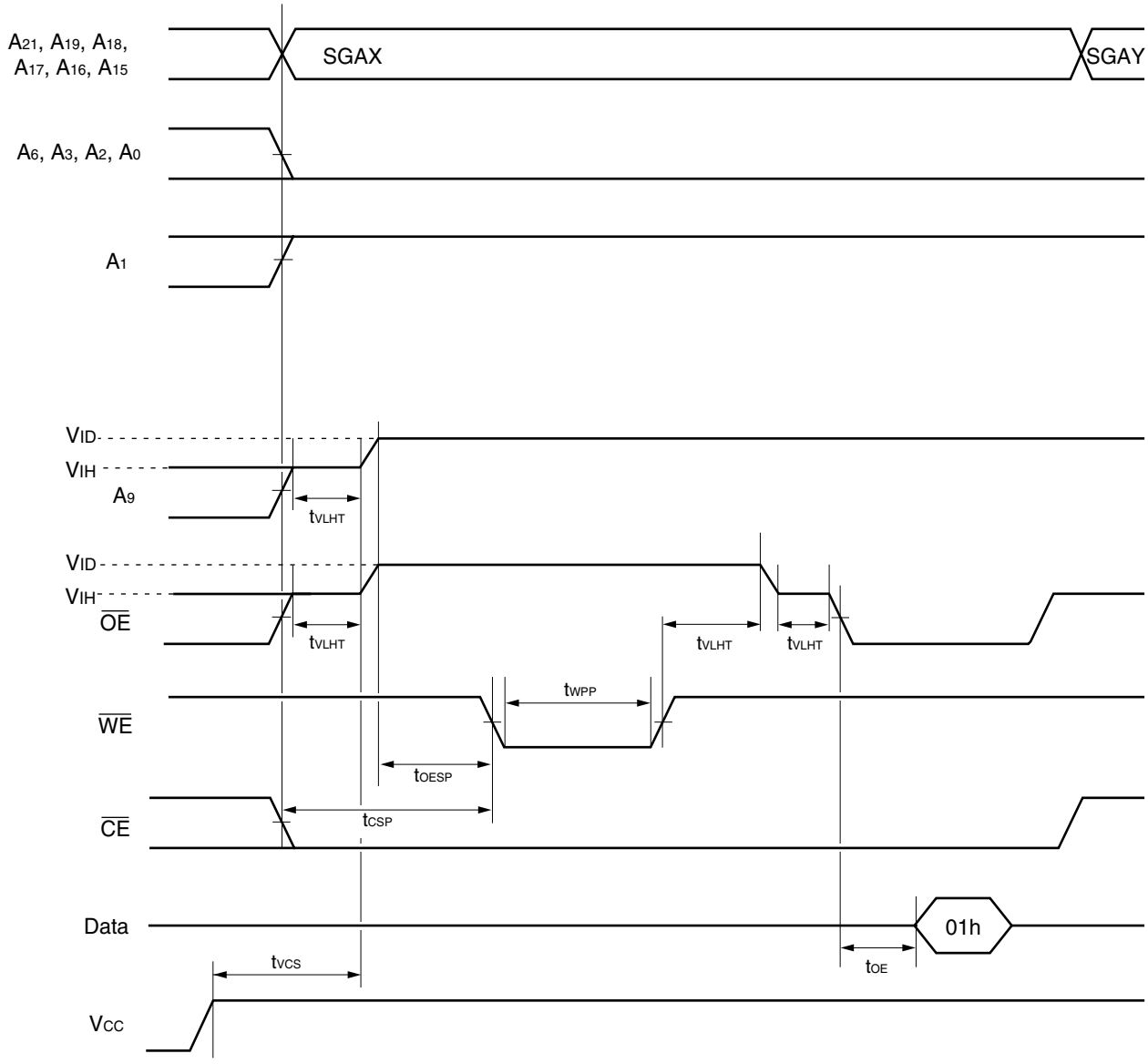
RY/$\overline{BY}$ Timing Diagram during Program/Erase Operation Timing Diagram



$\overline{RESET}$ Timing Diagram (Not during Embedded Algorithms)

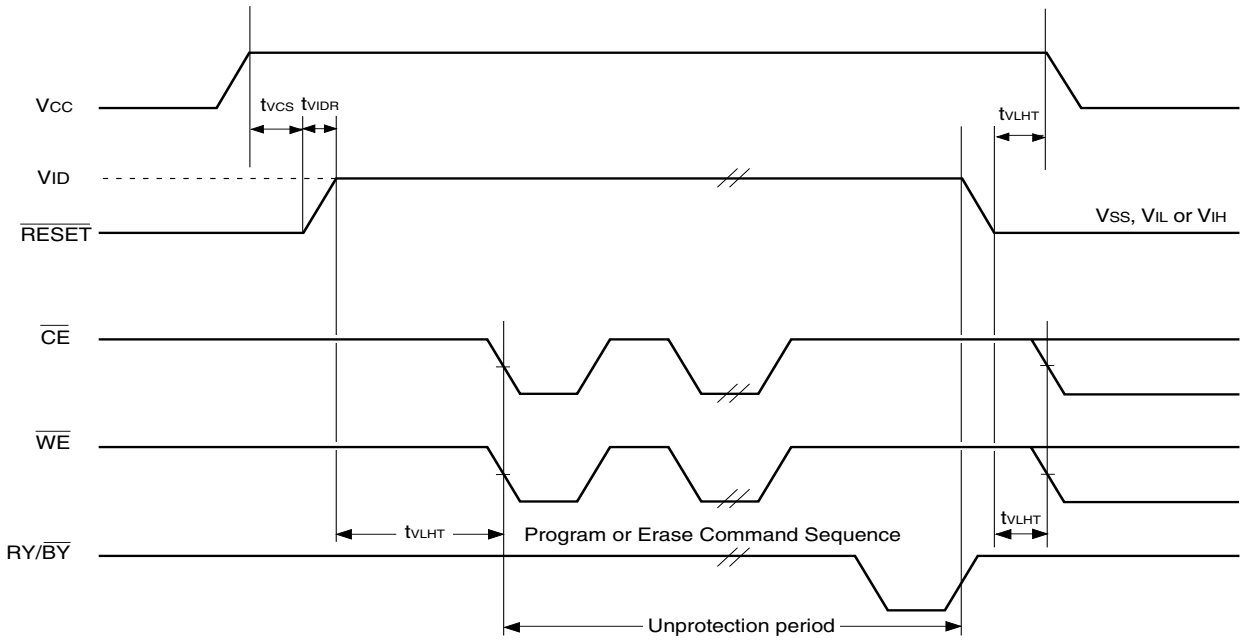


RESET Timing Diagram (During Embedded Algorithms)

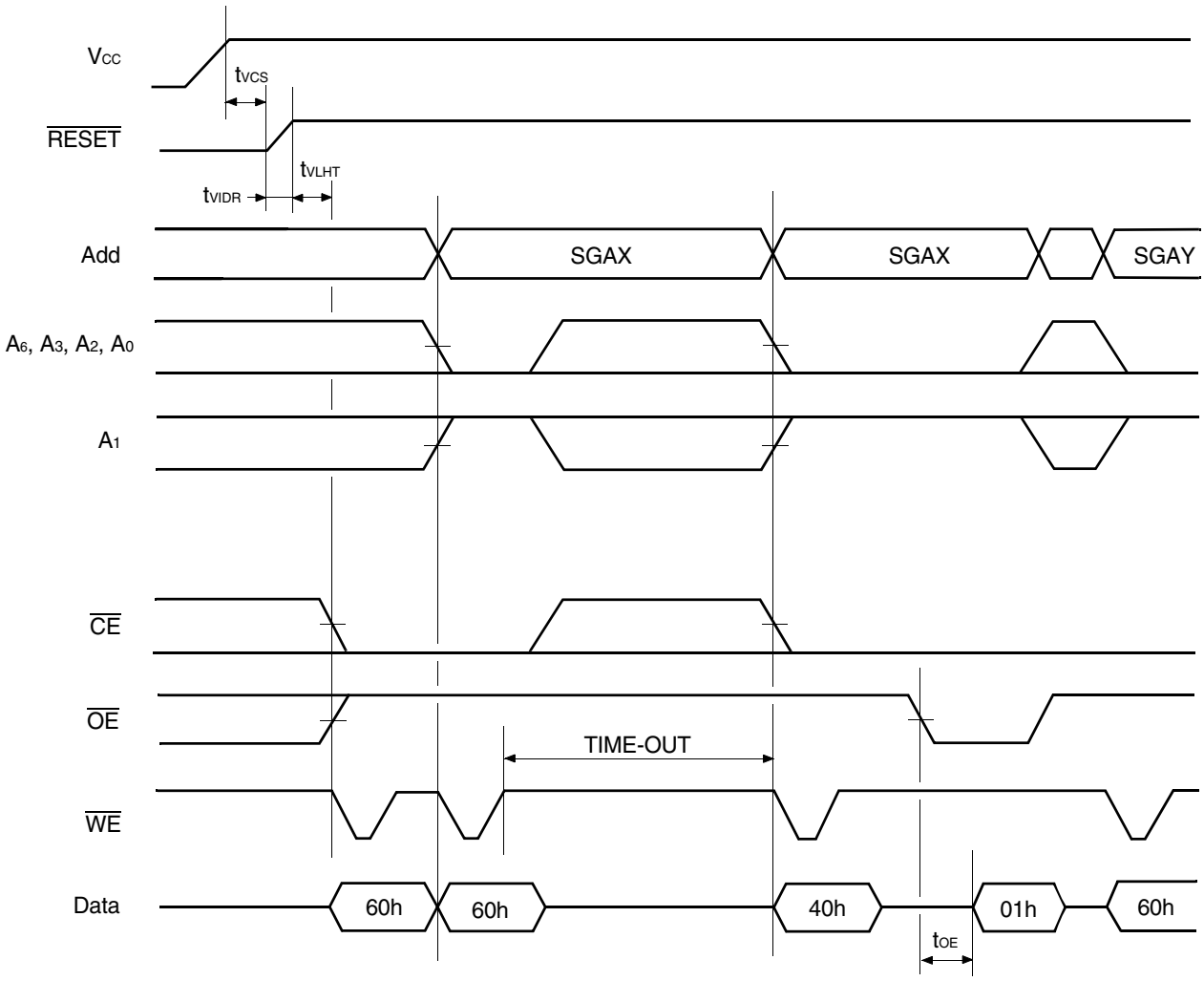


SGAX : Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected

Sector Group Protection Timing Diagram

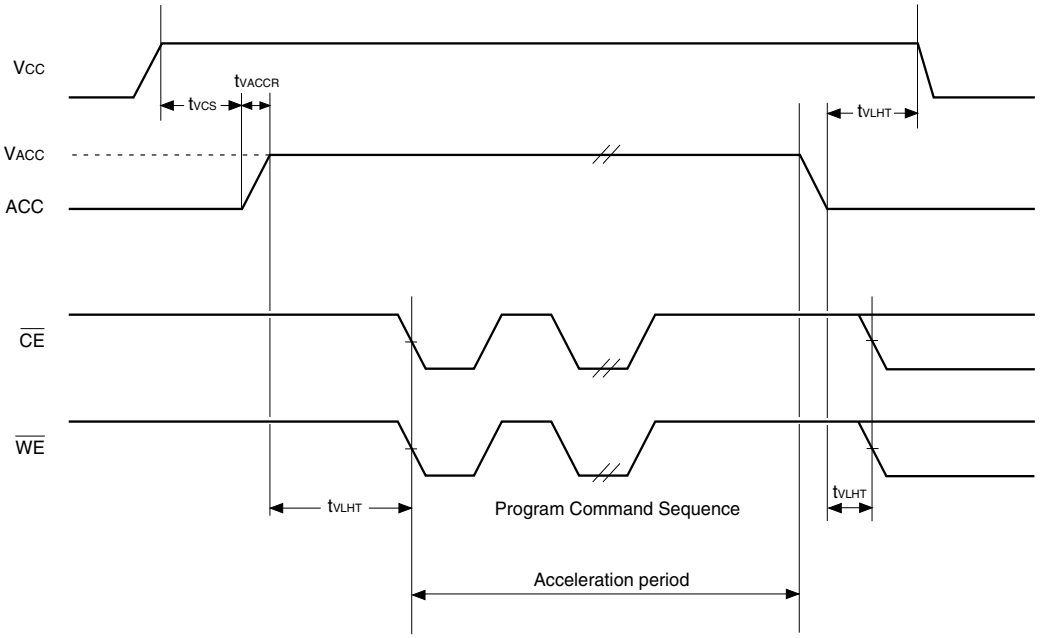


Temporary Sector Group Unprotection Timing Diagram



SGAX: Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 μs (Min)

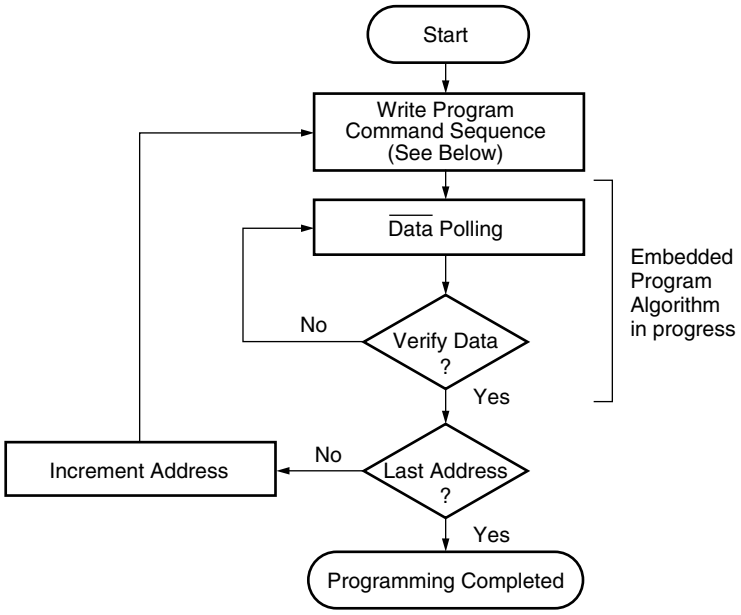
Extended Sector Group Protection Timing Diagram



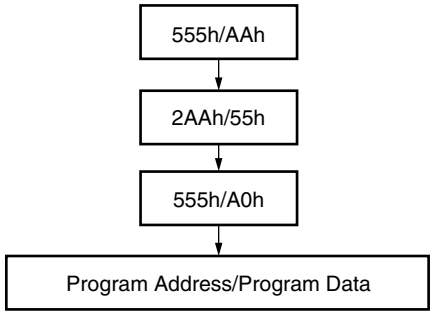
Accelerated Program Timing Diagram

■ FLOW CHART

EMBEDDED ALGORITHMS



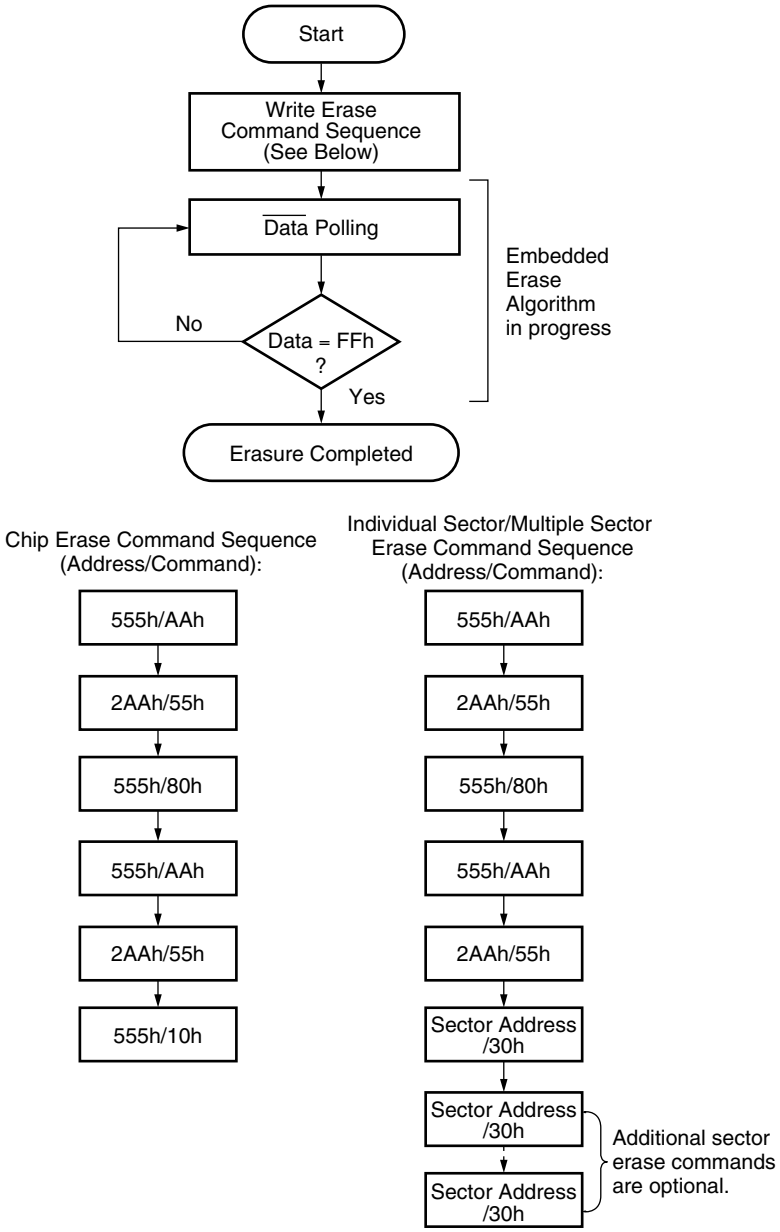
Program Command Sequence (Address/Command):



Note : The sequence is applied for Word (×16) mode.
The addresses differ from Byte (× 8) mode.

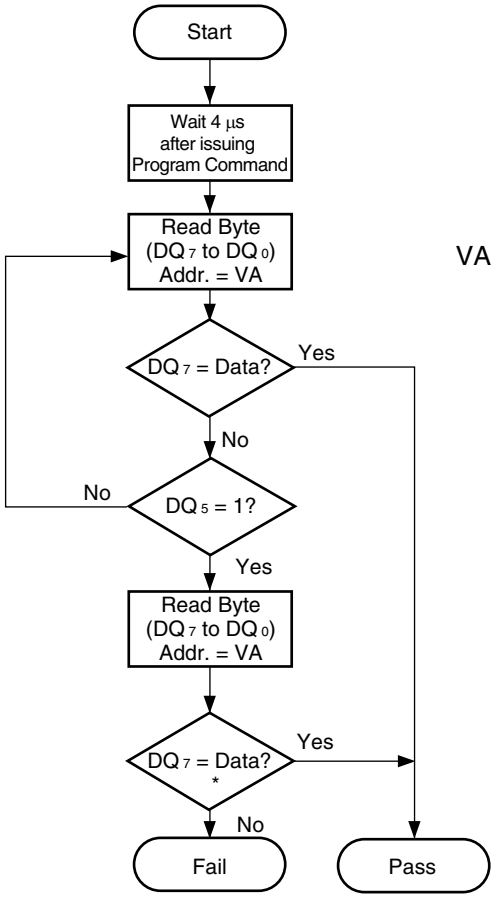
Embedded Program™ Algorithm

EMBEDDED ALGORITHMS



Note : The sequence is applied for Word (×16) mode.
The addresses differ from Byte (× 8) mode.

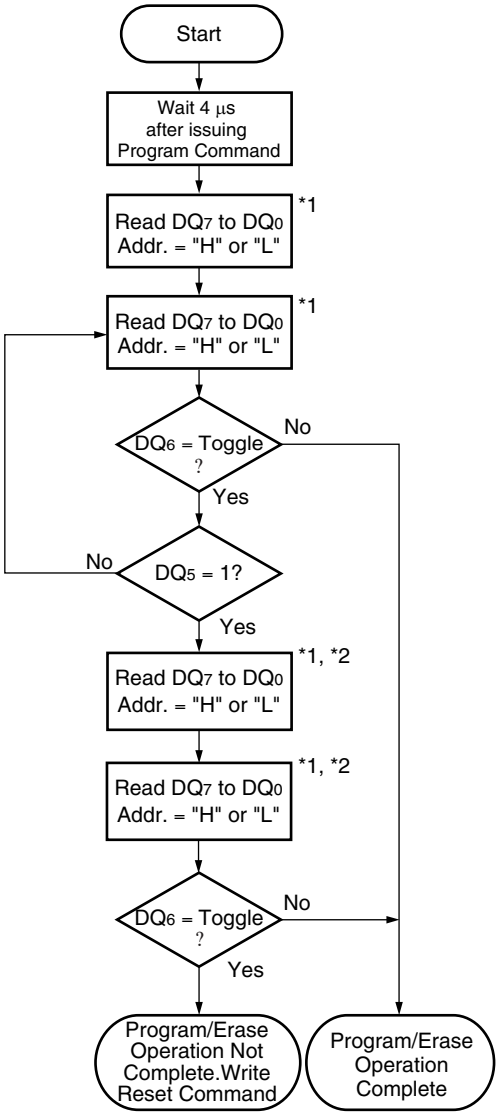
Embedded Erase™ Algorithm



VA = Valid address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple sector erases operation
= Any of the sector addresses within the sector not being protected during chip erase operation

* : DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

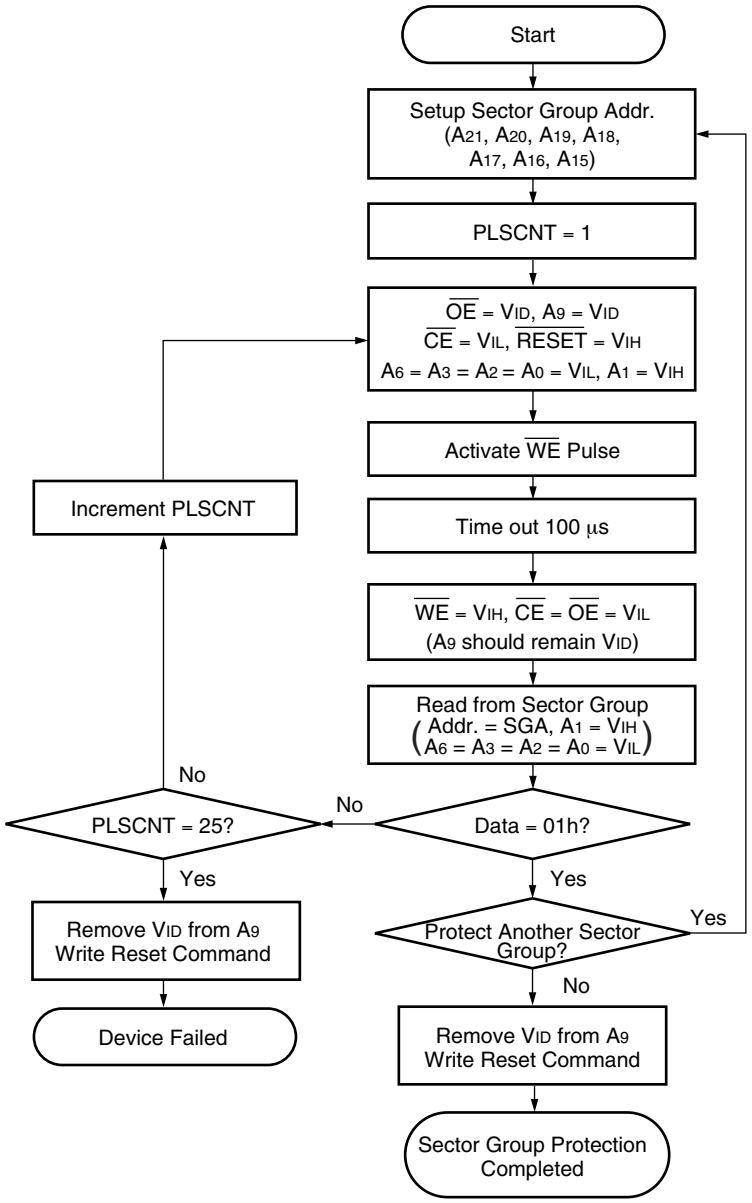
$\overline{\text{Data}}$ Polling Algorithm



*1 : Read Toggle bit twice to determine whether it is toggling.

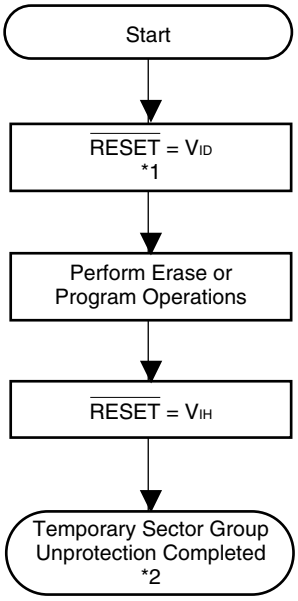
*2 : Recheck Toggle bit because it may stop toggling as DQ_5 changes to “1”.

Toggle Bit Algorithm



* : A_{-1} is V_{IL} in Byte (× 8) mode.

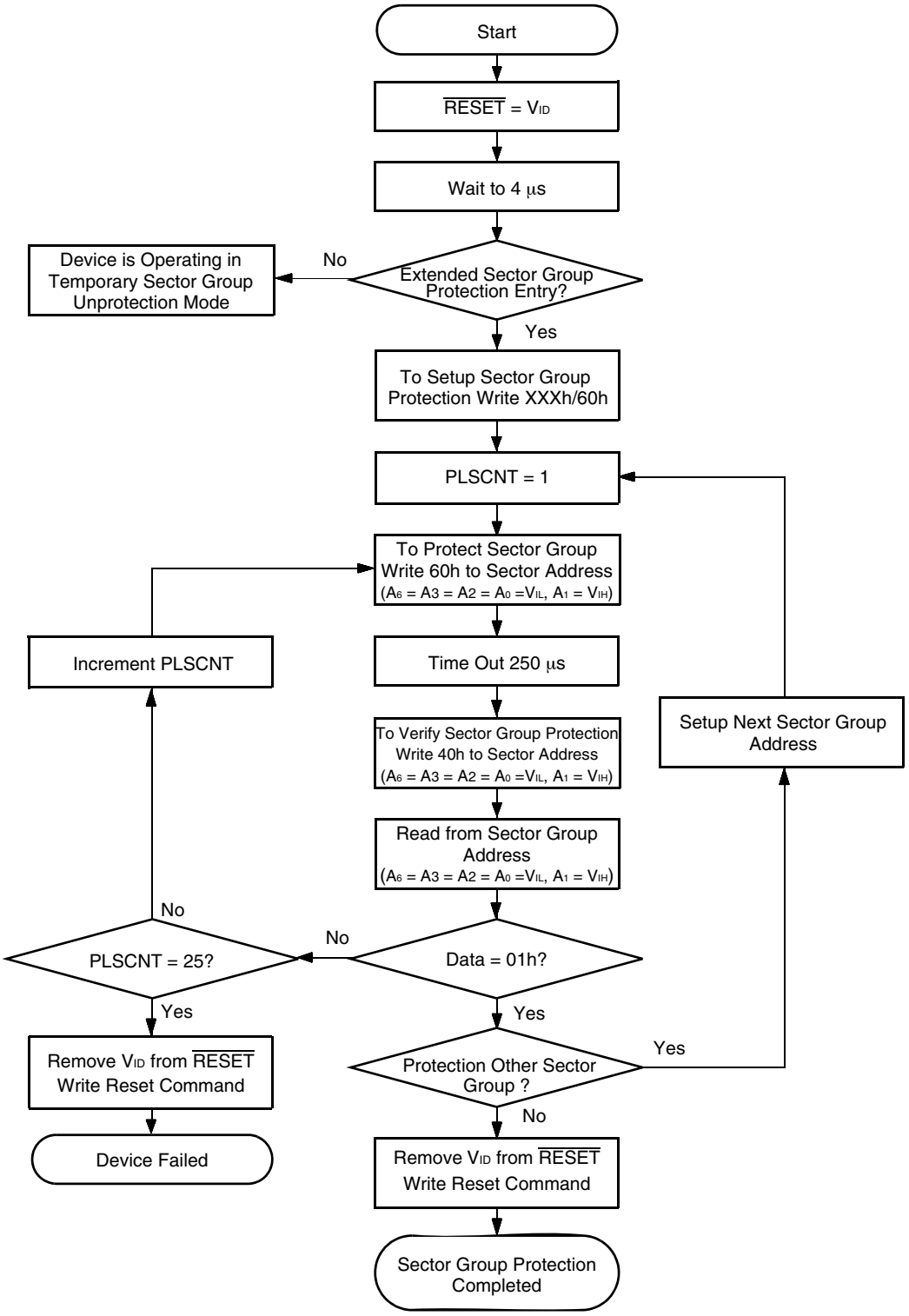
Sector Group Protection Algorithm



*1 : All protected sector groups are unprotected.

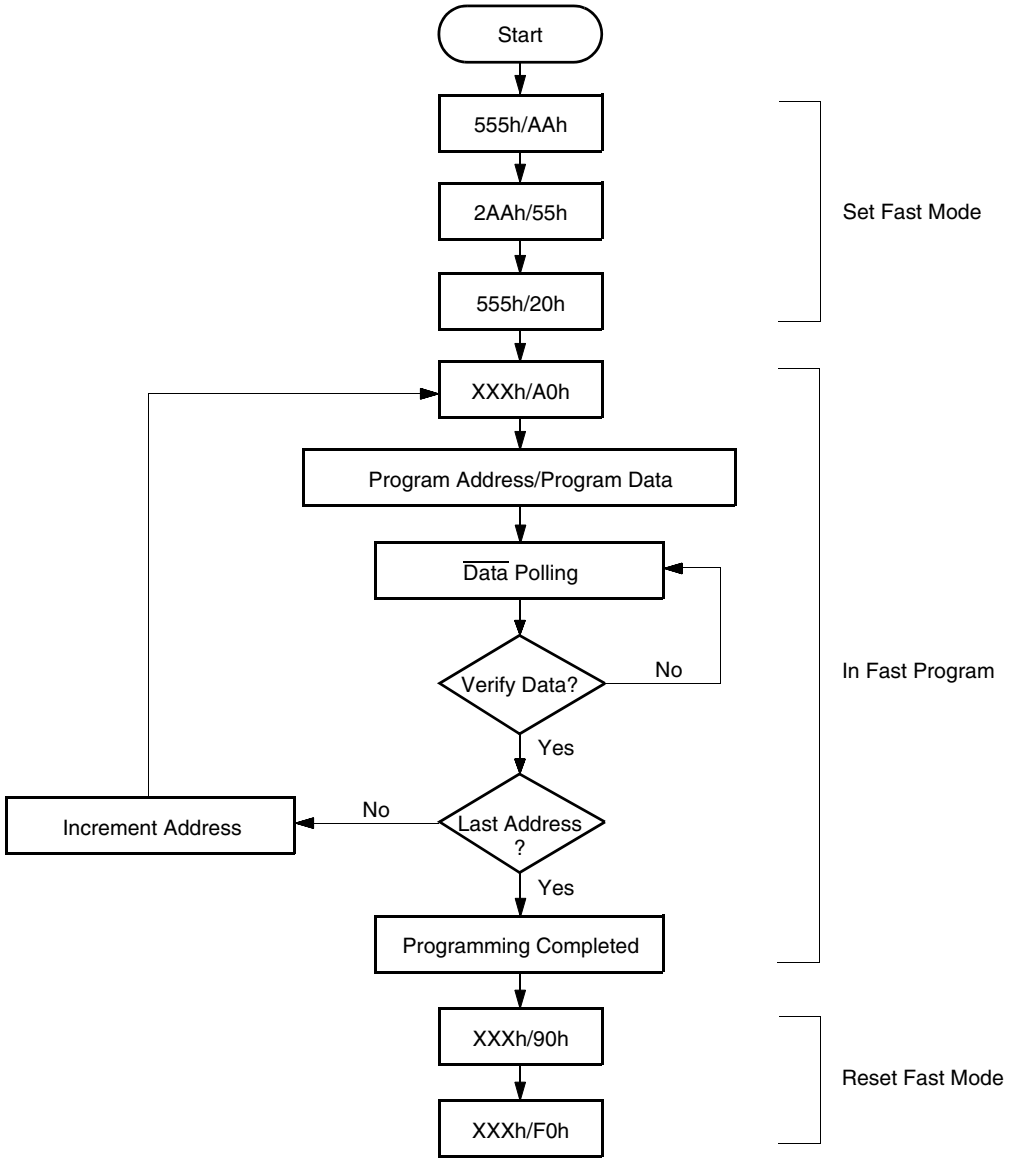
*2 : All previously protected sector groups are protected.

Temporary Sector Group Unprotection Algorithm



Extended Sector Group Protection Algorithm

FAST MODE ALGORITHM

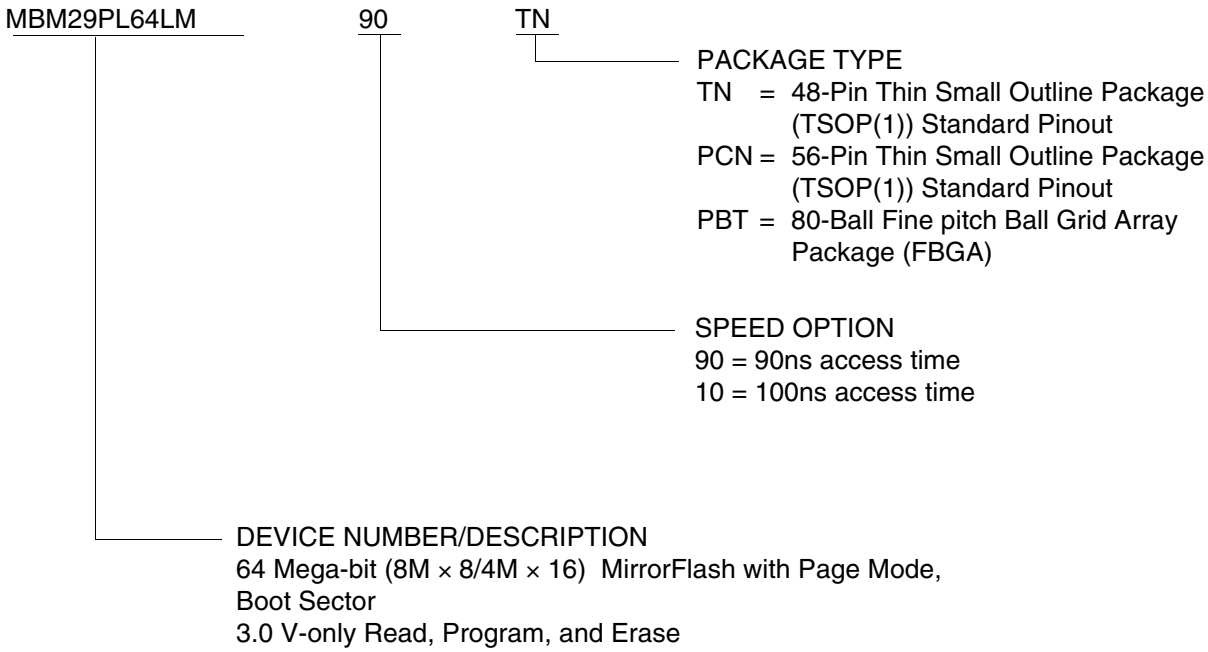


Notes : • The sequence is applied for Word (×16) mode.
• The addresses differ from Byte (× 8) mode.

Embedded Program™ Algorithm for Fast Mode

■ ORDERING INFORMATION

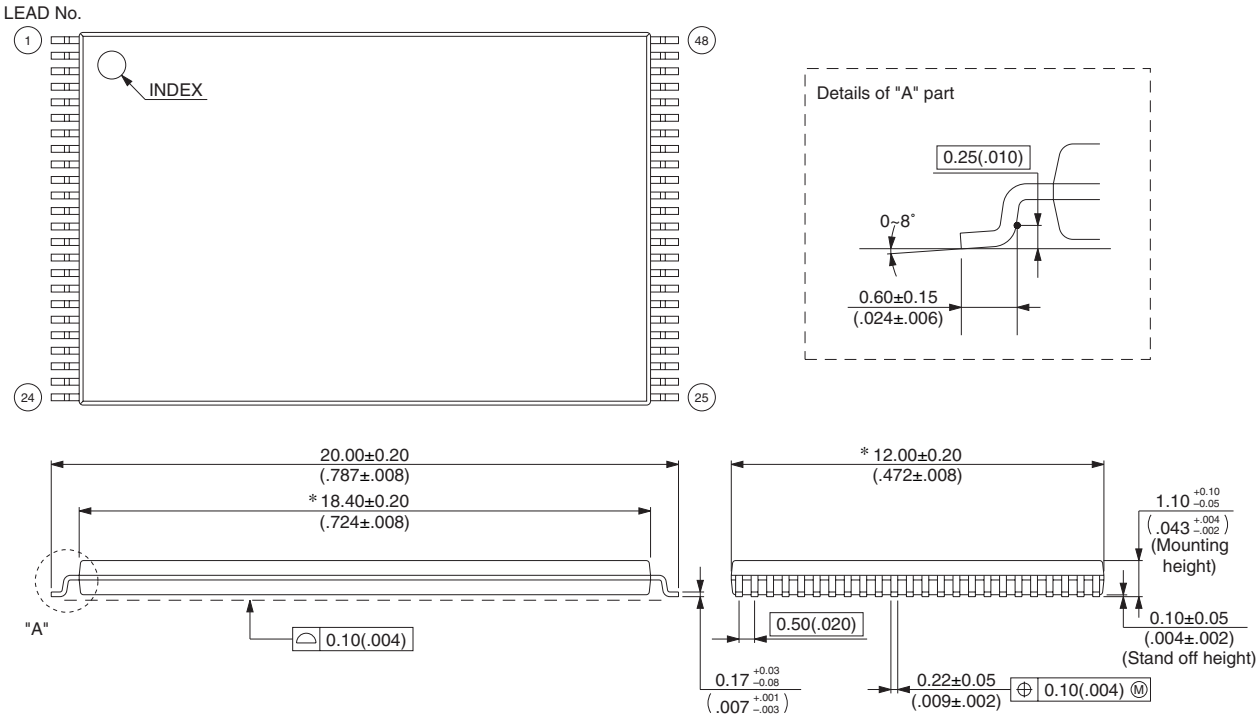
Part No.	Package	Access Time (ns)	Remarks
MBM29PL64LM90TN	48-pin, plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	90 ns	
MBM29PL64LM10TN		100 ns	
MBM29PL64LM90PCN	56-pin, plastic TSOP (1) (FPT-56P-M01) (Normal Bend)	90 ns	
MBM29PL64LM10PCN		100 ns	
MBM29PL64LM90PBT	80-ball, plastic FBGA (BGA-80P-M01)	90 ns	
MBM29PL64LM10PBT		100 ns	



■ PACKAGE DIMENSIONS

48-pin plastic TSOP(1)
(FPT-48P-M19)

Note 1) * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

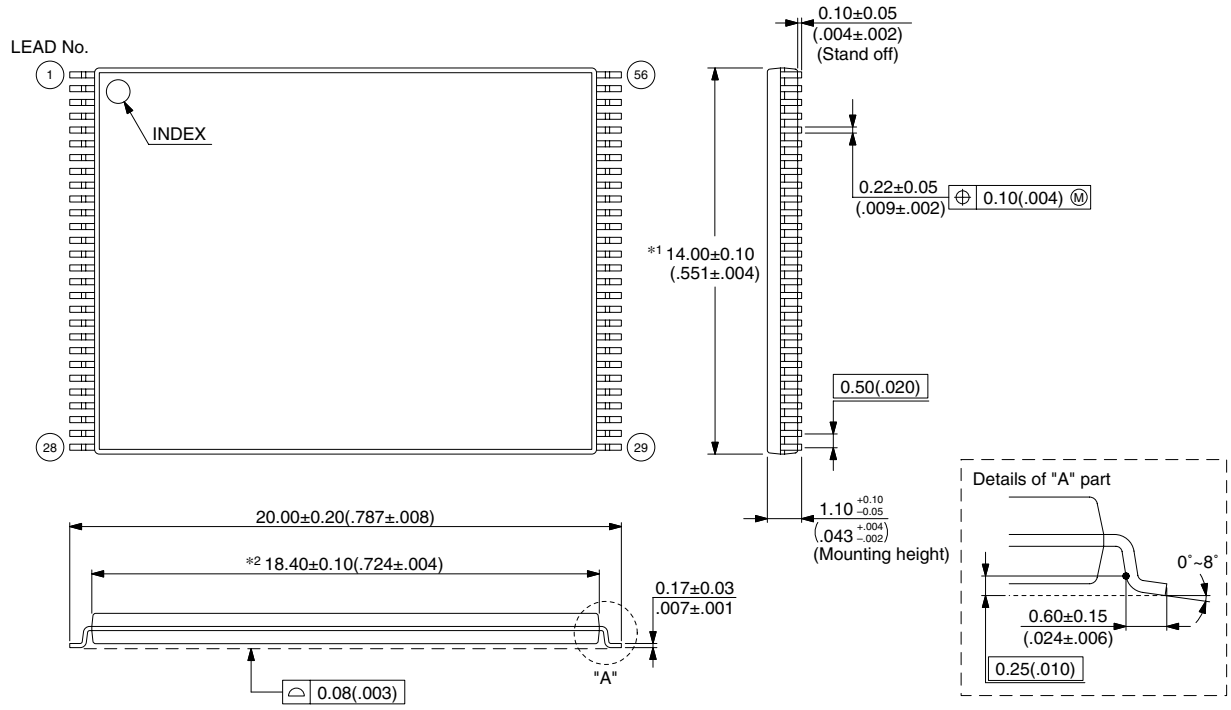


Dimensions in mm (inches)
Note : The values in parentheses are reference values.

(Continued)

56-pin plastic TSOP(1)
(FPT-56P-M01)

Note 1) *1 : Resn protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.

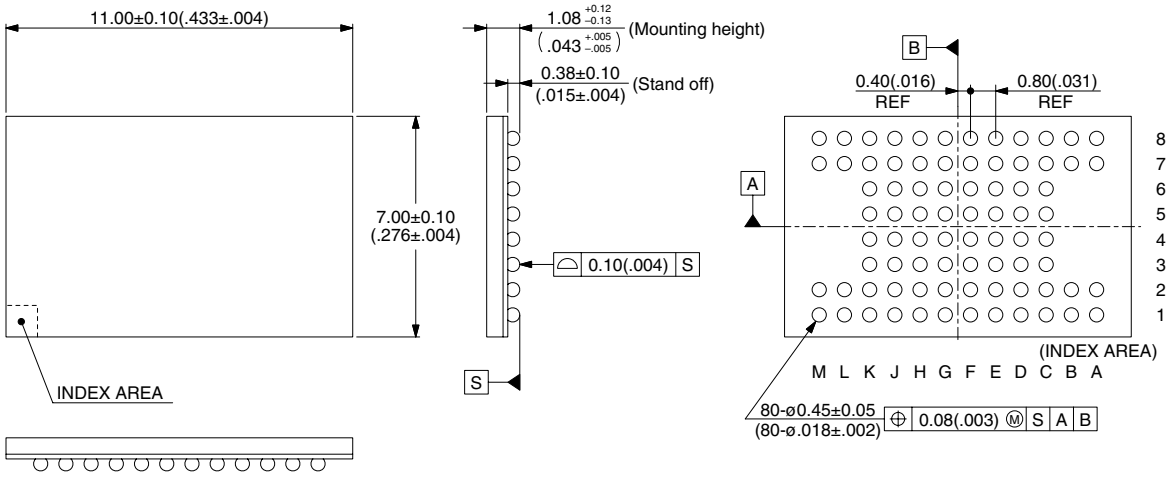


Dimensions in mm (inches)
Note : The values in parentheses are reference values.

(Continued)

(Continued)

80-ball plastic FBGA
(BGA-80P-M01)



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

Revision History

Revision DS05-20902-2E（July 31, 2007）

The following comment is added.

This product has been retired and is not recommended for new designs. Availability of this document is retained for reference and historical purposes only.

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