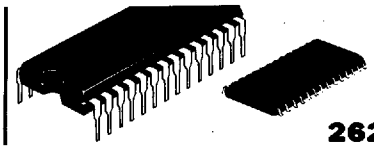


M5M5256AP, AFP-70, -85, -10, -70L, -85L, -10L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

MITSUBISHI (MEMORY/ASIC)

DESCRIPTION

This M5M5256AP, AFP is a 262,144-bit CMOS static RAM organized as 32,768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 32K x 8-bit pinout.

FEATURES

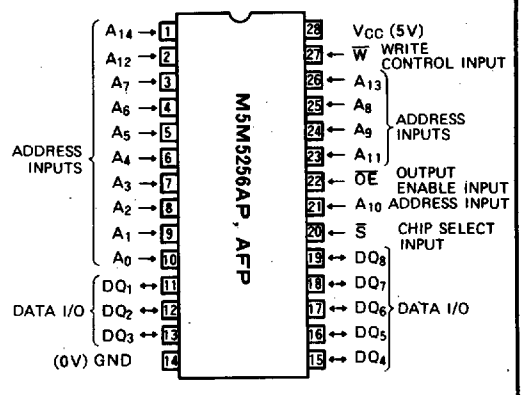
Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256AP, AFP-70 M5M5256AP, AFP-85 M5M5256AP, AFP-10	70ns 85ns 100ns	70mA	2mA
M5M5256AP, AFP-70L M5M5256AP, AFP-85L M5M5256AP, AFP-10L	70ns 85ns 100ns		100μA

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expantion by $\overline{S}$
- $\overline{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O
- Package
  M5M5256AP . . . . . 28 Pin 600mil DIP
  M5M5256AFP . . 28 Pin Small Outline Package (SOP)

APPLICATION

Small Capacity Memory Units.

PIN CONFIGURATION (TOP VIEW)



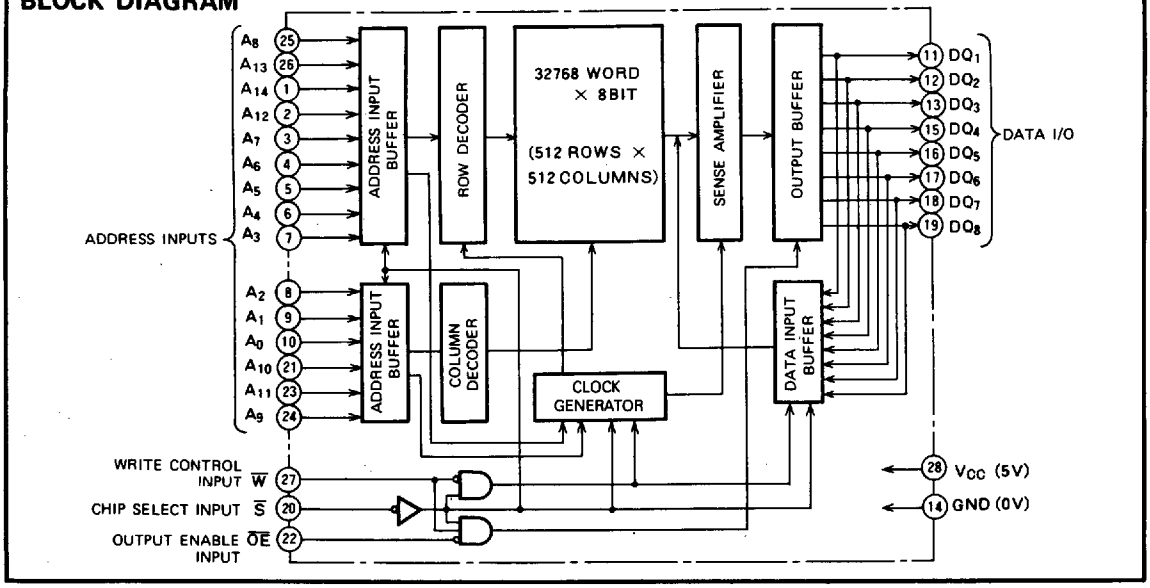
Outline 28P4 (AP)
28P2W (AFP)

FUNCTION

The operation mode of the M5M5256AP, AFP is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance

BLOCK DIAGRAM



state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expantion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		0～V_{CC}	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	−0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			−0.3		0.8	V
V_{OH}	High output voltage	I_{OH}=−1mA		2.4			V
V_{OL}	Low output voltage	I_{OL}=2mA				0.4	V
I_I	Input current	V_I=0～V_{CC}				±1	μA
I_O	Output current	$\overline{S}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=0～V_{CC}				±1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$<0.2, $\overline{W}$>V_{CC}−0.2, Output open Other input <0.2 or >V_{CC}−0.3 Min. cycle			30	65	mA
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$=V_{IL}, $\overline{W}$=V_{IH} Output open Other input =V_{IL} or V_{IH} Min. cycle			35	70	mA
I_{CC3}	Stand by supply current	$\overline{S}$≧V_{CC}−0.2V Other inputs =0～V_{CC}	AP, AFP			2	mA
			AP, AFP-L			100	μA
I_{CC4}	Stand by supply current	$\overline{S}$=V_{IH}, Other inputs=0～V_{CC}				3	mA
Ci	Input capacitance (Ta=25°C)	V_I=GND, V_i=25mVrms, f=1MHz				6	pF
Co	Output capacitance (Ta=25°C)	V_O=GND, V_O=25mVrms, f=1MHz				8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)
2 Typical value is V_{CC}=5V, Ta=25°C

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5256-70 M5M5256-70L			M5M5256-85 M5M5256-85L			M5M5256-10 M5M5256-10L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	70			85			100			ns
$t_{a(A)}$	Address access time			70			85			100	ns
$t_{a(S)}$	Chip select access time			70			85			100	ns
$t_{a(OE)}$	Output enable access time			35			45			50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			30			30			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			30			35	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5			5			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			10			ns
$t_{v(A)}$	Data valid time after address change	20			20			20			ns

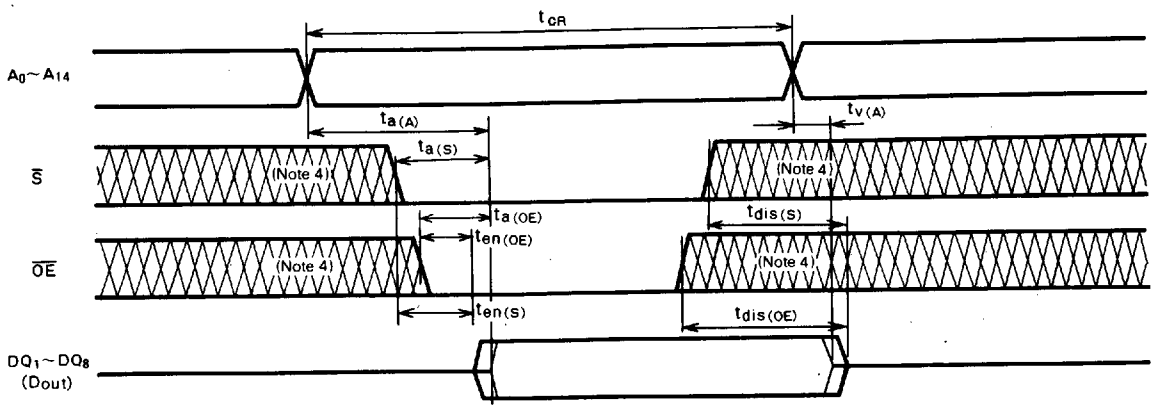
TIMING REQUIREMENTS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits									Unit
		M5M5256-70 M5M5256-70L			M5M5256-85 M5M5256-85L			M5M5256-10 M5M5256-10L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	70			85			100			ns
$t_{w(W)}$	Write pulse width	55			60			60			ns
$t_{su(A)}$	Address set up time	0			0			0			ns
$t_{su(A-\overline{WH})}$	Address set up time with respect to $\overline{W}$ high	65			75			80			ns
$t_{su(S)}$	Chip select set up time	65			75			80			ns
$t_{su(D)}$	Data set up time	30			35			35			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			25			30			35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			25			30			35	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			10			ns

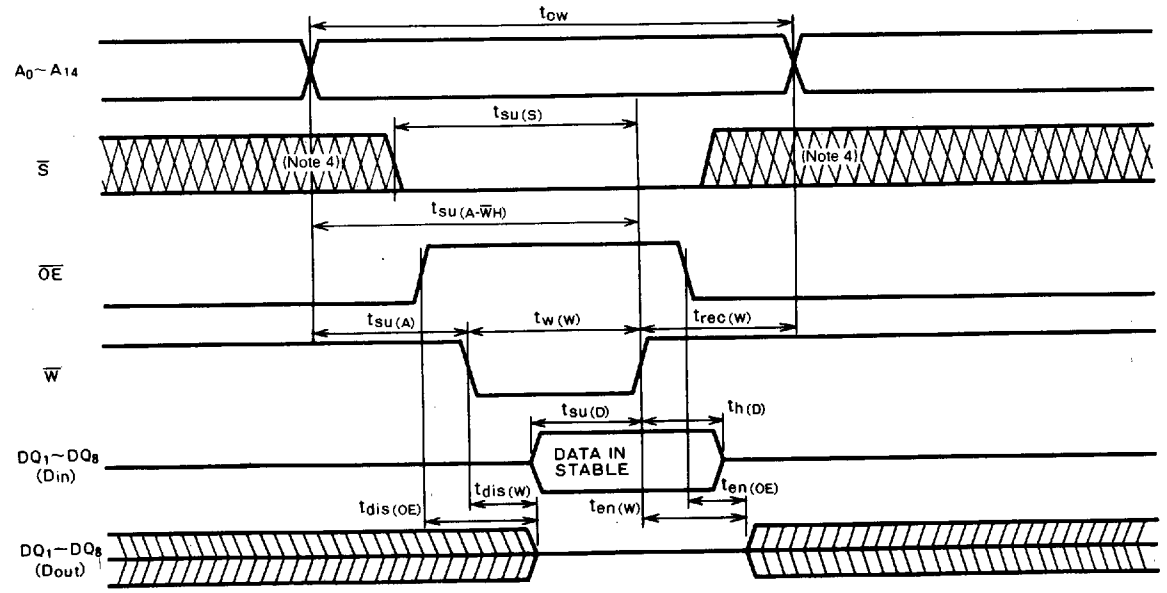
TIMING DIAGRAM

Read cycle

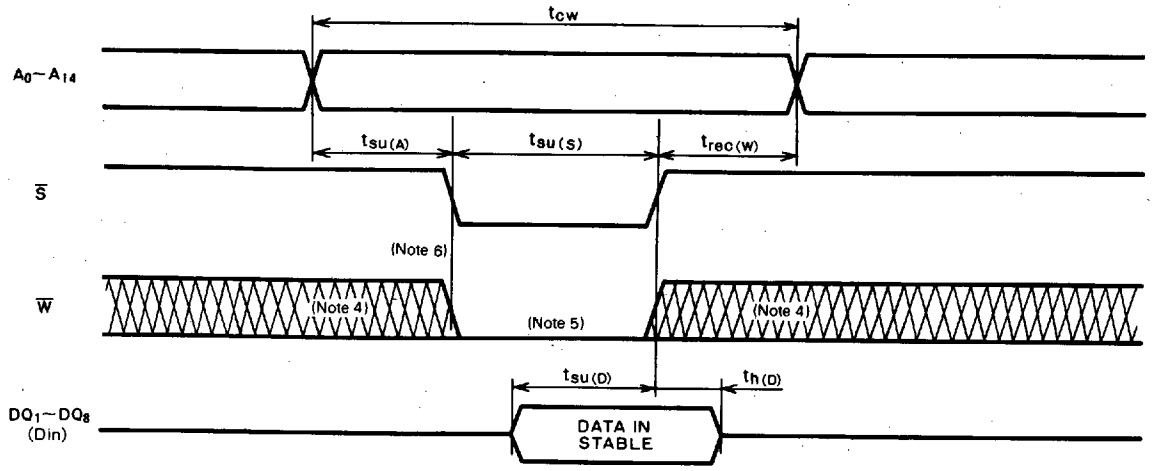


W = "H" level

Write cycle (W control)



Write cycle ($\overline{S}$ control)



Note 3: Test condition
Input pulse level: 0.6 ~ 2.4V
Input pulse rise, fall time, 10ns
Load: 1 TTL. C_L = 30pF for -70, -70L, 100pF for -85, -10, -85L, -10L.
Conditions of assessment: 1.5V
4: Hatching indicates the state is don't care.
5: Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, Other inputs =3V	AP, AFP			2	mA
			AP, AFP-L			50	μA

TIMING REQUIREMENTS (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS