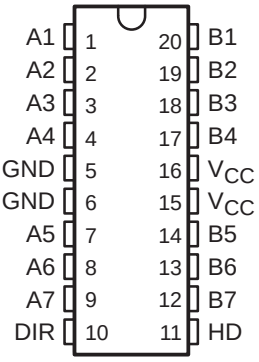
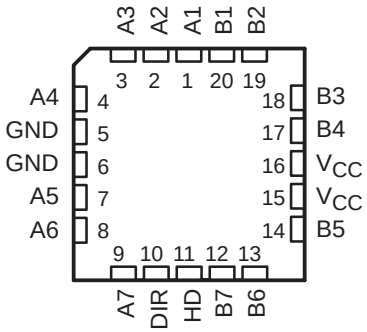
- **3-State Outputs Directly Drive Bus Lines**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Designed for the IEEE 1284-I (Level 1 Type) and IEEE 1284-II (Level 2 Type) Electrical Specifications**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and DIP (N) Packages, Ceramic Chip Carriers (FK), Flat (W), and DIP (J) Packages**

SN54ACT1284 . . . J OR W PACKAGE
SN74ACT1284 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The ’ACT1284 are designed for asynchronous two-way communication between data buses. The control function minimizes external timing requirements.

The devices allow data transmission in either the A-to-B or the B-to-A direction for bits 1, 2, 3, and 4, depending on the logic level at the direction-control (DIR) input. Bits 5, 6, and 7, however, always transmit in the A-to-B direction.

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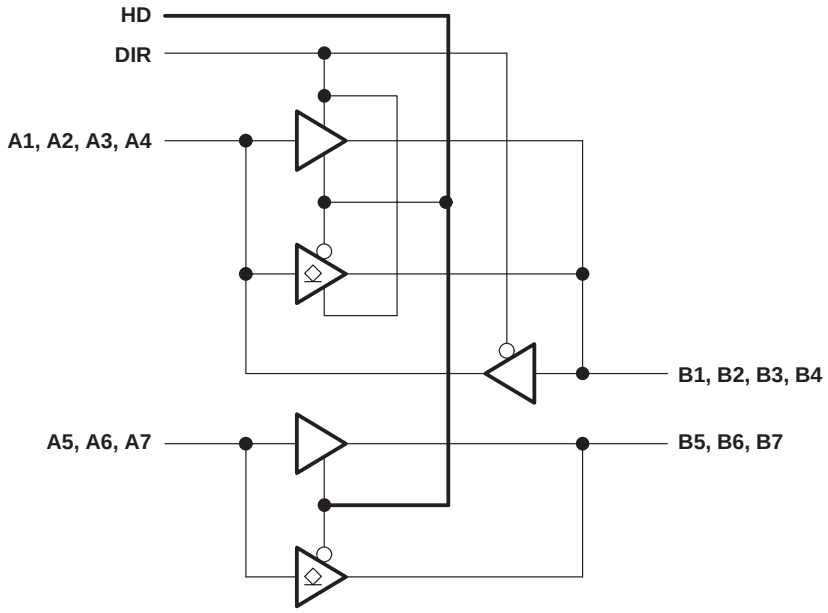
The SN54ACT1284 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT1284 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A to B: Bits 5, 6, 7
		Totem pole	B to A: Bits 1, 2, 3, 4
L	H	Totem pole	B to A: Bits 1, 2, 3, 4 and A to B: Bits 5, 6, 7
H	L	Open drain	A to B: Bits 1, 2, 3, 4, 5, 6, 7
H	H	Totem pole	A to B: Bits 1, 2, 3, 4, 5, 6, 7

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
B-port input and output voltage range, V_I and V_O (see Notes 1 and 2) . . . . . –2 V to 7 V
A-port input and output voltage range, V_I and V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The ac input voltage pulsewidth is limited to 20 ns if the input voltage goes more negative than –0.5 V.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54ACT1284		SN74ACT1284		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.7	5.5	4.7	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Open drain output voltage	HD low	0	5.5	0	5.5	V
I_{OH}	High-level output current	B port, HD high		–14		–14	mA
		A port		–4		–4	
I_{OL}	Low-level output current	B port		14		14	mA
		A port		4		4	
T_A	Operating free-air temperature		–55	125	0	70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

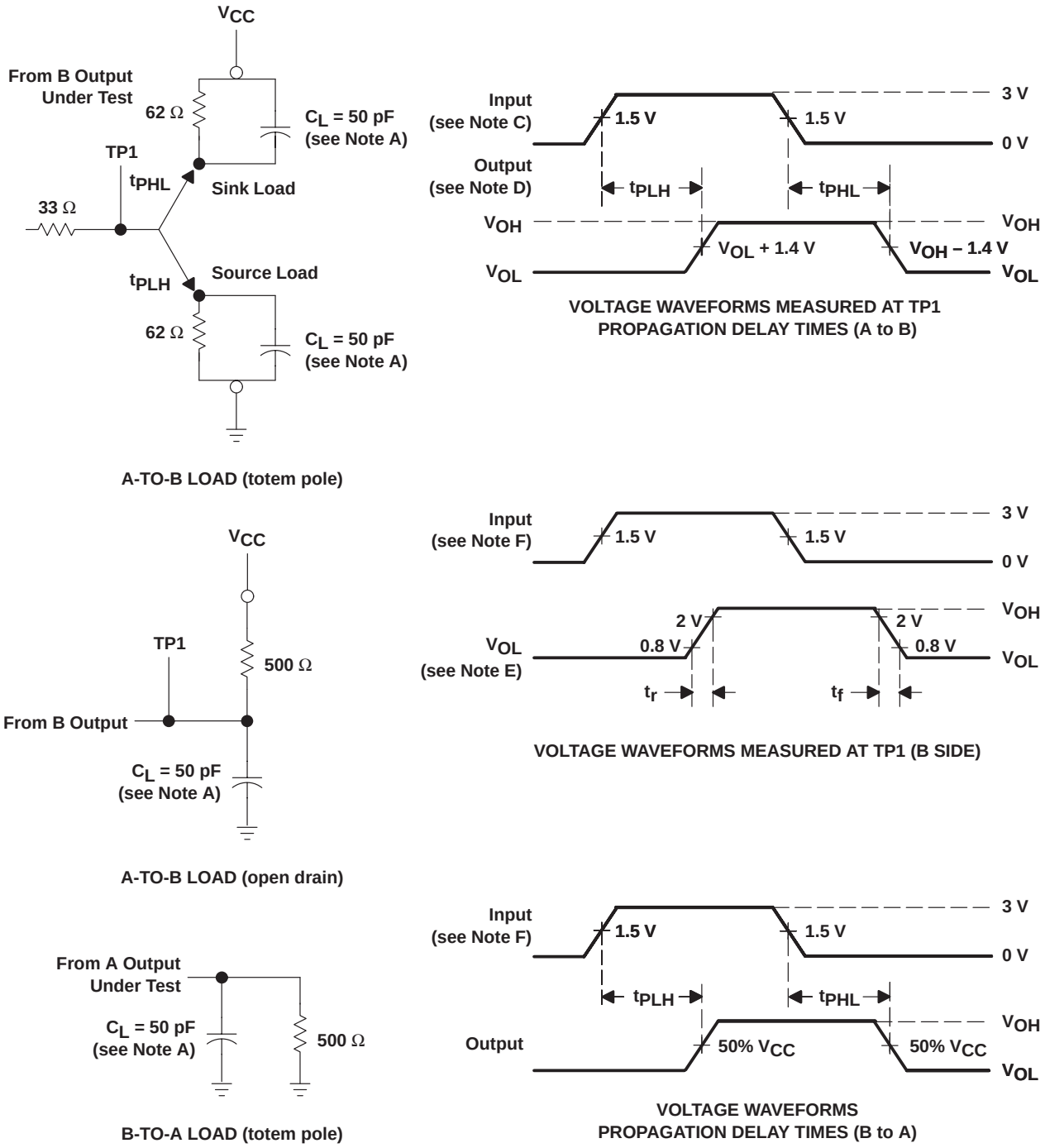
PARAMETER		TEST CONDITIONS	V_{CC}†	SN54ACT1284			SN74ACT1284			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{hys}	Input hysteresis	$V_{IT+} – V_{IT–}$ for all inputs	5 V	0.4			0.4			V
			4.7 V	0.2			0.2			
V_{OH}	B port	I_{OH} = –14 mA	4.7 V	2.4			2.4			V
	A port	I_{OH} = –50 µA	MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			
		I_{OH} = –4 mA	4.7 V	3.7			3.7			
V_{OL}	B port	I_{OL} = 14 mA	4.7 V			0.4			0.4	V
	A port	I_{OL} = 50 µA	4.7 V			0.2			0.2	
		I_{OL} = 4 mA				0.4			0.4	
I_I		$V_I = V_{CC}$ or GND	5.5 V			±1			±1	µA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±20			±20	µA
I_{OFF}	B port	V_I or $V_O \le 7$ V	0 V			±100			±100	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			1.5			1.5	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4			4		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12			12		pF
Z_O	B port	I_{OH} = –20 mA, I_{OH} = –50 mA	5 V	8		30	8		30	Ω

† For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.
‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	SN54ACT1284		SN74ACT1284		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Totem pole	A or B	B or A	1	20	1	20	ns
t_{PHL}				1	20	1	20	
SR	Totem pole	B output		0.05	0.4	0.05	0.4	V/ns
t_{pd}(EN)	Totem pole	HD	B	1	20	1	20	ns
t_{pd}(DIS)				1	20	1	20	
t_r, t_f	Open drain	A	B		120		120	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.
C. Input rise and fall times are 3 ns, 150 ns < pulsewidth <10 μs for both low-to-high and high-to-low transitions.
D. Slew rate is defined as 10% and 90% of the transition times.
E. Rise and fall times, open drain, are <120 ns.
F. Input rise and fall times are 3 ns.

Figure 1. Load Circuits and Voltage Waveforms

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SN74ACT1284, 7-Bit Bus Interfaces With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74ACT1284
Voltage Nodes (V)	5
Static Current	1.5

FEATURES

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DESCRIPTION

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TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74act1284.pdf (93 KB,Rev.B) (Updated: 04/01/1996)

APPLICATION NOTES

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View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)

- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- LVT-to-LVTH Conversion (SCEA010 - Updated: 12/08/1998)
- Logic Solutions For IEEE Std 1284 (SCEA013 - Updated: 06/01/1999)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

BLOCK DIAGRAMS

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Generic Set Top Box - System Test

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ACT1284DBR	SSOP (DB)	20	0 TO 70	ACTIVE	View Product Content	Request Samples
SN74ACT1284DW	SOP (DW)	20	0 TO 70	ACTIVE	View Product Content	Request Samples
SN74ACT1284PWR	TSSOP (PW)	20	0 TO 70	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74ACT1284DBLE	OBSOLETE	SSOP (DB) | 20	0 TO 70	View Contents	1KU |		N/A*		Not Available			
SN74ACT1284DBR	ACTIVE	SSOP (DB) | 20	0 TO 70	View Contents	1KU | 0.64	2000	N/A*	484 | 25 Sep	8 WKS			
SN74ACT1284DW	ACTIVE	SOP (DW) | 20	0 TO 70	View Contents	1KU | 0.64	25	3225		8 WKS	DigiKey | AMERICA	423	BUY NOW
SN74ACT1284DWR	ACTIVE	SOP (DW) | 20	0 TO 70	View Contents	1KU | 0.64	2000	N/A*	2000 | 05 Nov	8 WKS	DigiKey | AMERICA	>1k	BUY NOW
SN74ACT1284NSR	ACTIVE	SOP (NS) | 20	0 TO 70	View Contents	1KU | 0.67	2000	N/A*		8 WKS			
SN74ACT1284PWR	ACTIVE	TSSOP (PW) | 20	0 TO 70	View Contents	1KU | 0.64	2000	N/A*	>10k | 14 Nov	8 WKS			

Table Data Updated on: 9/26/2002