

## Document Title

256Kx8 bit Low Power and Low Voltage CMOS Static RAM

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Design target	May 26, 1998	Advance
1.0	Finalize	October 8, 1998	Final
2.0	Revised - Add FBGA type package	July 21, 1999	Final

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## 256Kx8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: TFT
- Organization: 256Kx8
- Power Supply Voltage
  - K6T2008V2A Family: 3.0V~3.6V
  - K6T2008U2A Family: 2.7V~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-TSOP1-0820F, 32-TSOP1-0813.4F  
48-FBGA-6.00x7.00

### GENERAL DESCRIPTION

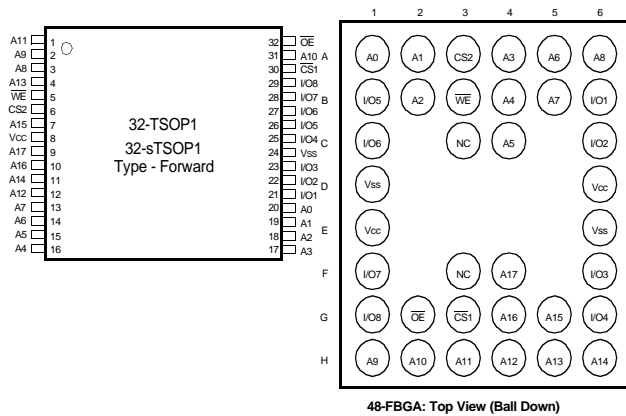
The K6T2008V2A and K6T2008U2A families are fabricated by SAMSUNG's advanced CMOS process technology. The family support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
K6T2008V2A-B K6T2008U2A-B	Commercial(0~70°C)	3.0~3.6V 2.7~3.3V	70/85ns 70 <sup>1)</sup> /85/100ns	10µA	30mA <sup>2)</sup>	32-TSOP1-0820F 32-TSOP1-0813.4F 48-FBGA-6.00x7.00
K6T2008V2A-F K6T2008U2A-F	Industrial(-40~85°C)	3.0~3.6V 2.7~3.3V	70 <sup>1)</sup> /85/100ns	15µA		

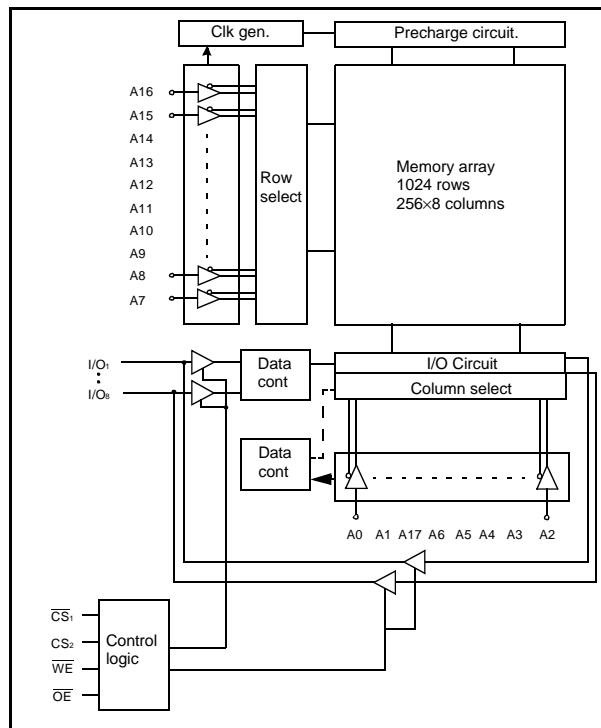
1. The parameters are tested with 30pF test load
2. K6T2008V2A Family = 35mA

### PIN DESCRIPTION



Name	Function	Name	Function
CS <sub>1</sub> , CS <sub>2</sub>	Chip Select Inputs	I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Inputs/Outputs
OE	Output Enable Input	Vcc	Power
WE	Write Enable Input	Vss	Ground
A <sub>0</sub> ~A <sub>17</sub>	Address Inputs	N.C.	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T2008V2A-TB70 K6T2008V2A-TB85	32-TSOP1 F, 70ns, 3.3V,LL 32-TSOP1 F, 85ns, 3.3V,LL	K6T2008V2A-TF70 K6T2008V2A-TF85 K6T2008V2A-TF10	32-TSOP1 F, 70ns, 3.3V, LL 32-TSOP1 F, 85ns, 3.3V, LL 32-TSOP1 F, 100ns, 3.3V, LL
K6T2008U2A-TB70 K6T2008U2A-TB85 K6T2008U2A-TB10	32-TSOP1 F, 70ns, 3.0V, LL 32-TSOP1 F, 85ns, 3.0V, LL 32-TSOP1 F, 100ns, 3.0V, LL	K6T2008U2A-TF70 K6T2008U2A-TF85 K6T2008U2A-TF10	32-TSOP1 F, 70ns, 3.0V, LL 32-TSOP1 F, 85ns, 3.0V, LL 32-TSOP1 F, 100ns, 3.0V, LL
K6T2008V2A-YB70 K6T2008V2A-YB85	32-sTSOP1 F, 70ns, 3.3V,LL 32-sTSOP1 F, 85ns, 3.3V,LL	K6T2008V2A-YF70 K6T2008V2A-YF85 K6T2008V2A-YF10	32-sTSOP1 F, 70ns, 3.3V, LL 32-sTSOP1 F, 85ns, 3.3V, LL 32-sTSOP1 F, 100ns, 3.3V, LL
K6T2008U2A-YB70 K6T2008U2A-YB85 K6T2008U2A-YB10	32-sTSOP1 F, 70ns, 3.0V, LL 32-sTSOP1 F, 85ns, 3.0V, LL 32-sTSOP1 F, 100ns, 3.0V, LL	K6T2008U2A-YF70 K6T2008U2A-YF85 K6T2008U2A-YF10	32-sTSOP1 F, 70ns, 3.0V, LL 32-sTSOP1 F, 85ns, 3.0V, LL 32-sTSOP1 F, 100ns, 3.0V, LL
		K6T2008V2A-FF70 K6T2008V2A-FF85	48-FBGA, 70ns, 3.3V, LL 48-FBGA, 85ns, 3.3V, LL
		K6T2008U2A-FF70 K6T2008U2A-FF85	48-FBGA, 70ns, 3.0V, LL 48-FBGA, 85ns, 3.0V, LL

## FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.3 to 4.6	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	K6T2008V2A-L, K6T2008U2A-L
		-40 to 85	°C	K6T2008V2A-P, K6T2008U2A-P

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	K6T2008V2A Family K6T2008U2A Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V <sub>SS</sub>	All Family	0	0	0	V
Input high voltage	V <sub>IH</sub>	K6T2008V2A, K6T2008U2A Family	2.2	-	V <sub>CC</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	K6T2008V2A, K6T2008U2A Family	-0.3 <sup>3)</sup>	-	0.6	V

Note:

- Commercial Product : T<sub>A</sub>=0 to 70°C, otherwise specified  
Industrial Product : T<sub>A</sub>=-40 to 85°C, otherwise specified
- Overshoot : V<sub>CC</sub>+2.0V in case of pulse width≤30ns
- Undershoot : -2.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

- Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

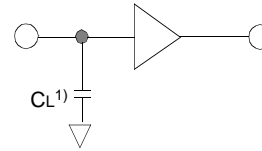
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	5	mA
Average operating current	ICC1	Cycle time=1μs, 100%duty, I <sub>IO</sub> =0mA, $\overline{CS}_1\leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V	-	-	4	mA
	ICC2	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	25	30 <sup>1)</sup>	mA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.3	mA
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS}_1\geq V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V or CS <sub>2</sub> ≤0.2V, Other inputs=0~V <sub>CC</sub>	-	0.2	10 <sup>2)</sup>	μA

- K6T2008V2A Family = 35mA
- Industrial product = 15μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 1.5V  
 Output load(see right) :  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS (K6T2008V2A Family: $V_{CC}=3.0\sim 3.6\text{V}$ , K6T2008U2A Family: $V_{CC}=2.7\sim 3.3\text{V}$ Commercial Product: $T_A=0$ to $70^\circ\text{C}$ , Industrial Product: $T_A=-40$ to $85^\circ\text{C}$ )

Parameter List	Symbol	Speed Bins						Units	
		70ns		85ns		100ns			
		Min	Max	Min	Max	Min	Max		
Read	Read cycle time	t <sub>RC</sub>	70	-	85	-	100	-	ns
	Address access time	t <sub>AA</sub>	-	70	-	85	-	100	ns
	Chip select to output	t <sub>CO1</sub> , t <sub>CO2</sub>	-	70	-	85	-	100	ns
	Output enable to valid output	t <sub>OE</sub>	-	35	-	40	-	50	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	25	0	25	0	30	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	25	0	25	0	30	ns
	Output hold from address change	t <sub>OH</sub>	10	-	15	-	15	-	ns
Write	Write cycle time	t <sub>WC</sub>	70	-	85	-	100	-	ns
	Chip select to end of write	t <sub>CW</sub>	60	-	70	-	80	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	60	-	70	-	80	-	ns
	Write pulse width	t <sub>WP</sub>	55	-	60	-	70	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	25	0	30	0	30	ns
	Data to write time overlap	t <sub>DW</sub>	30	-	35	-	40	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	5	-	ns

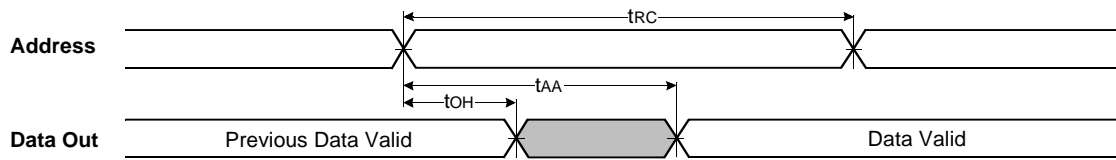
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	2.0	-	3.6	V
Data retention current	I <sub>DR</sub>	$V_{CC}=3.0\text{V}$ , $\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	-	0.2	10 <sup>(2)</sup>	μA
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

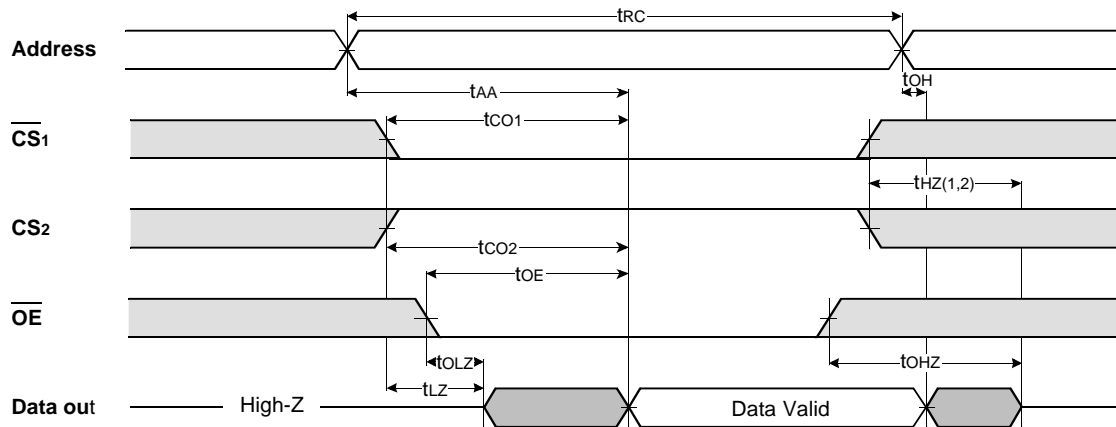
1.  $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$ ,  $CS_2 \geq V_{CC}-0.2\text{V}$  ( $\overline{CS}_1$  controlled) or  $CS_2 \leq 0.2\text{V}$  ( $CS_2$  controlled)  
 2. Industrial Products = 15μA

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}_1 = \overline{OE} = V_{IL}$ ,  $CS_2 = \overline{WE} = V_{IH}$ )



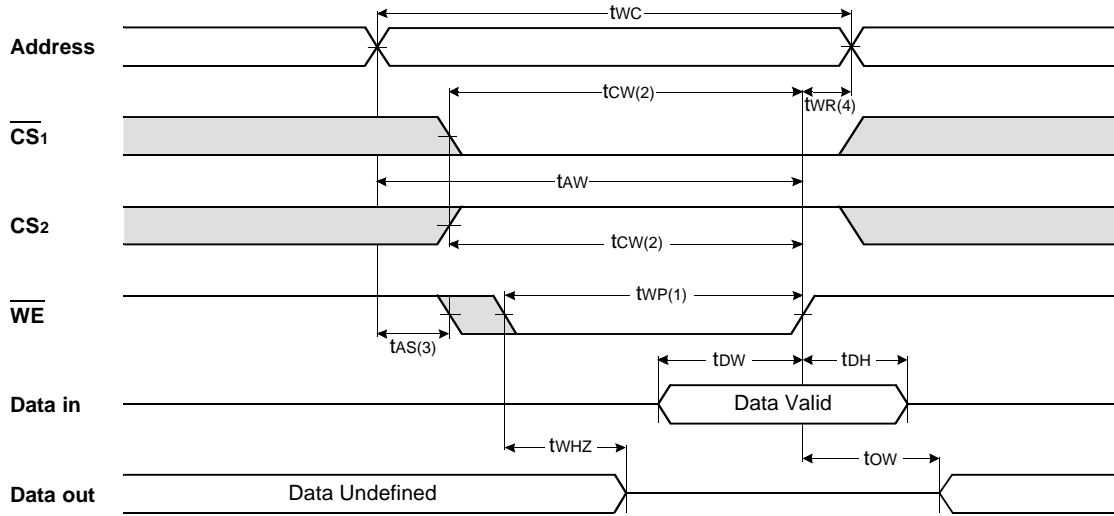
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE} = V_{IH}$ )



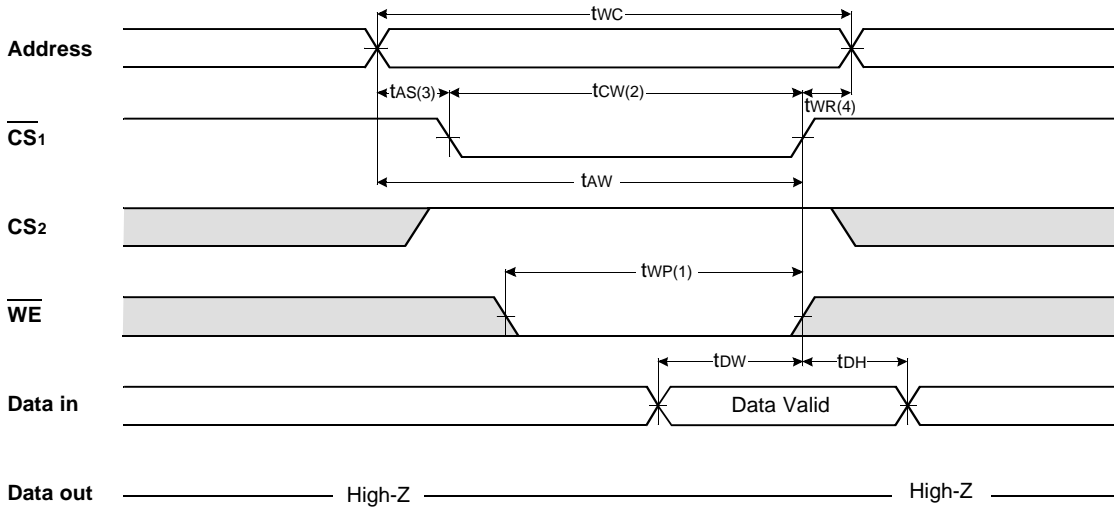
**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

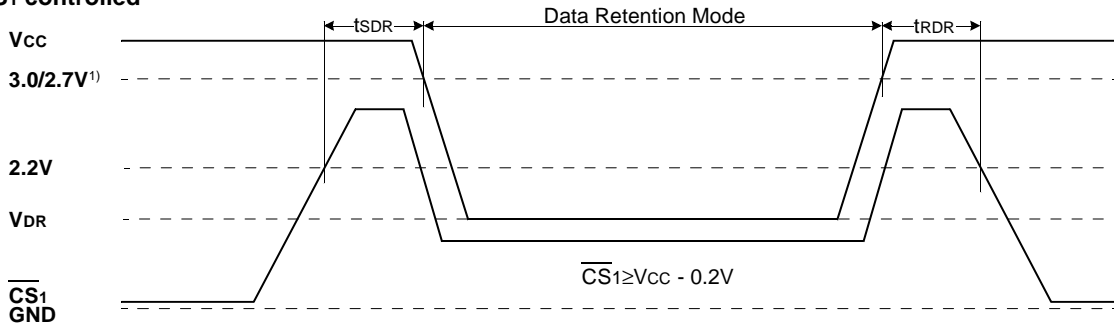


### NOTES (WRITE CYCLE)

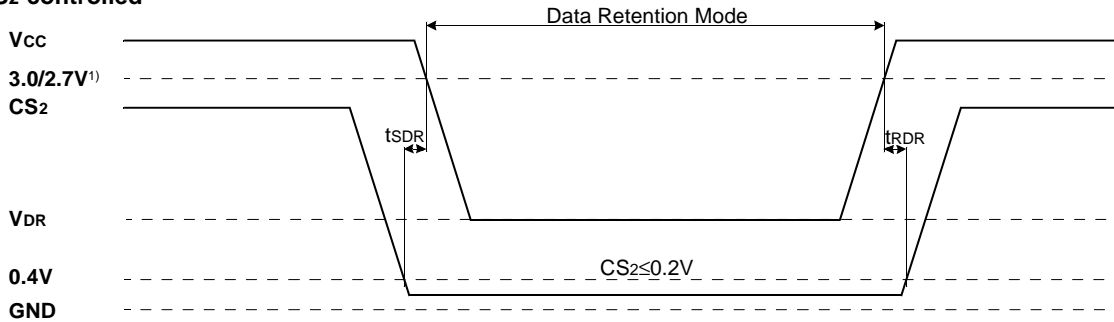
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low : A write ends at the earliest transition among  $CS_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR2}$  applied in case a write ends as  $CS_2$  going to low.

## DATA RETENTION WAVE FORM

### $\overline{CS}_1$ controlled



### $CS_2$ controlled



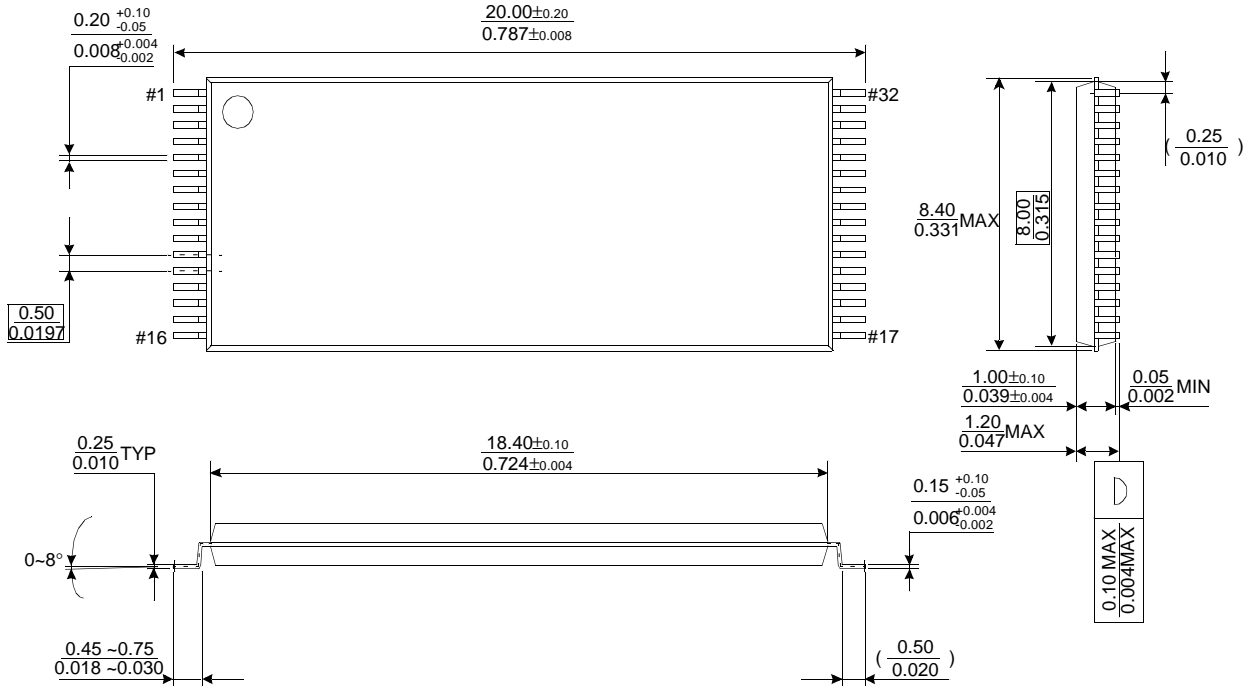
1. 3.0V for K6T2008V2A Family, 2.7V for K6T2008U2A Family



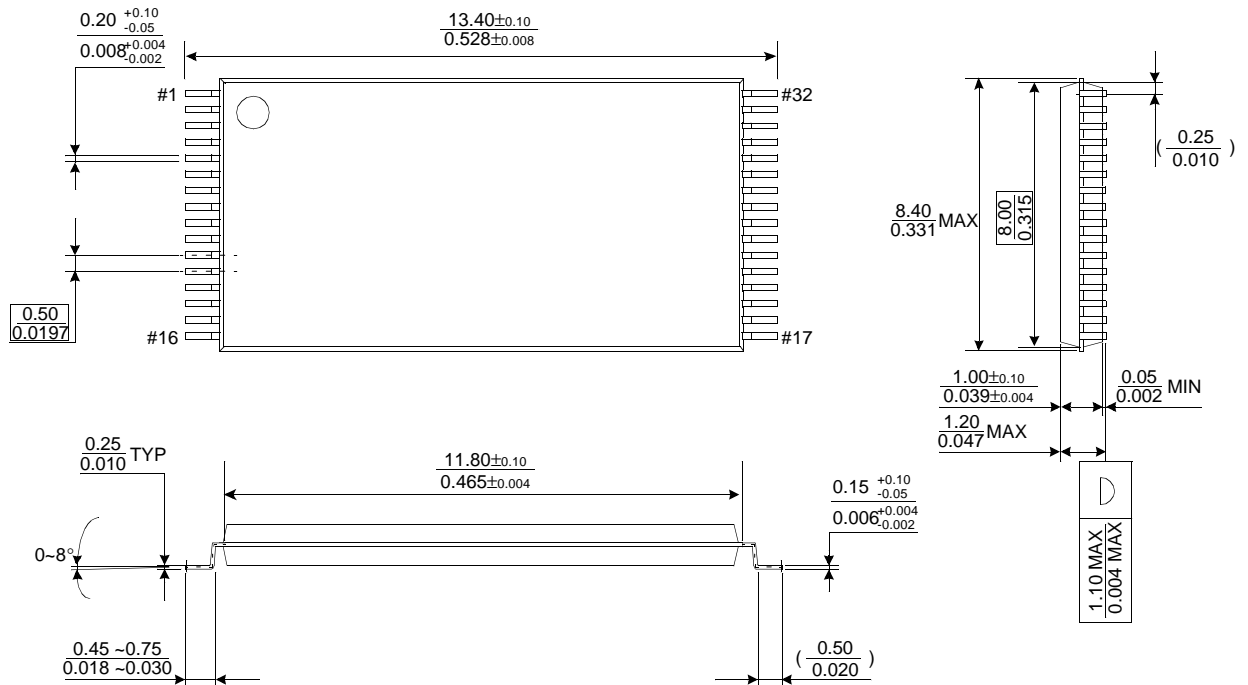
## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



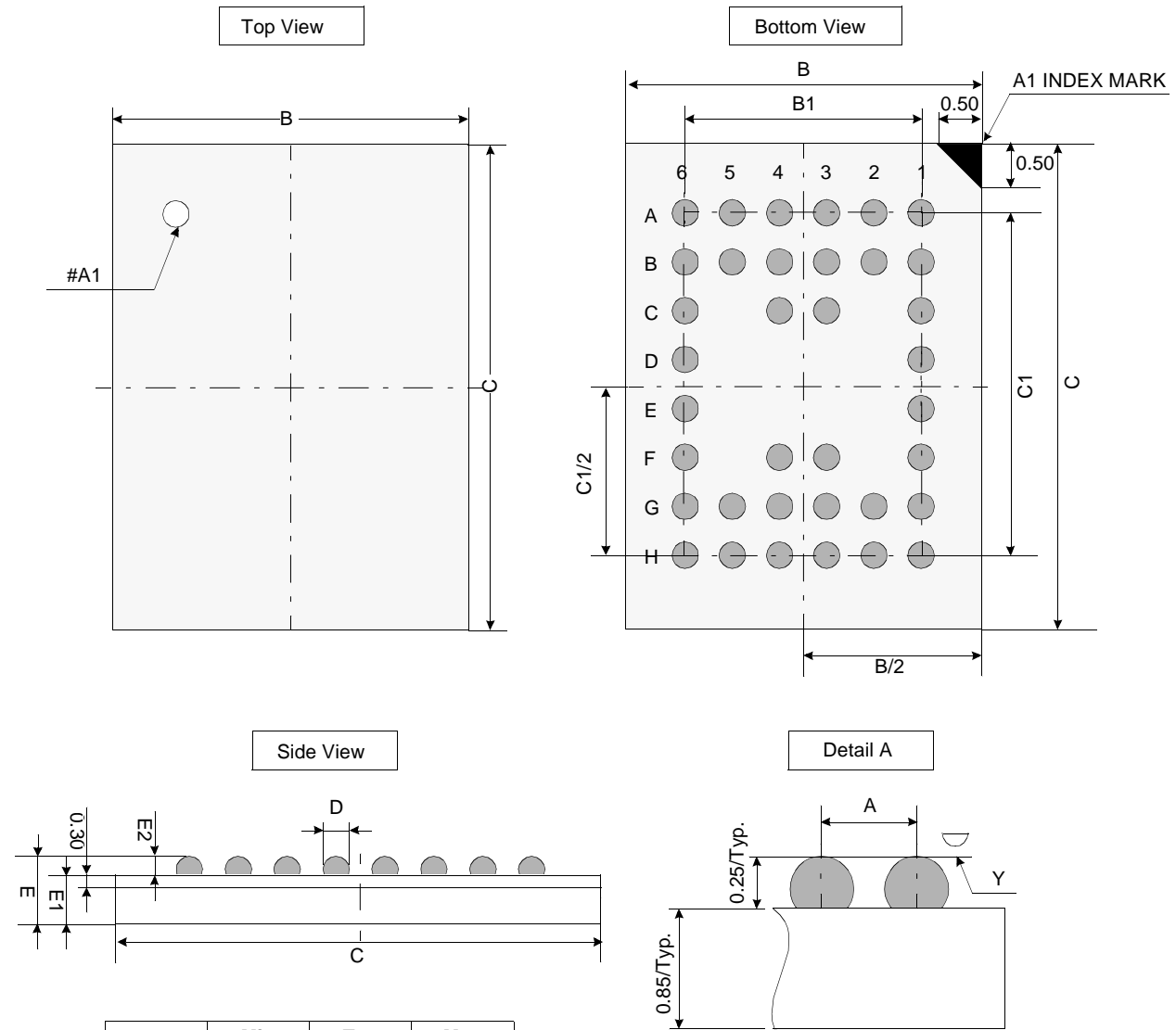
### 32 PIN SMALLER THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



## PACKAGE DIMENSIONS

Units: millimeters

### 48 BALL FINE PITCH BALL GRID ARRAY(6.00X7.00)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	6.90	7.00	7.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.10	1.20
E1	-	0.85	-
E2	0.20	0.25	0.30
Y	-	-	0.08

#### Notes.

1. Bump counts: 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)