



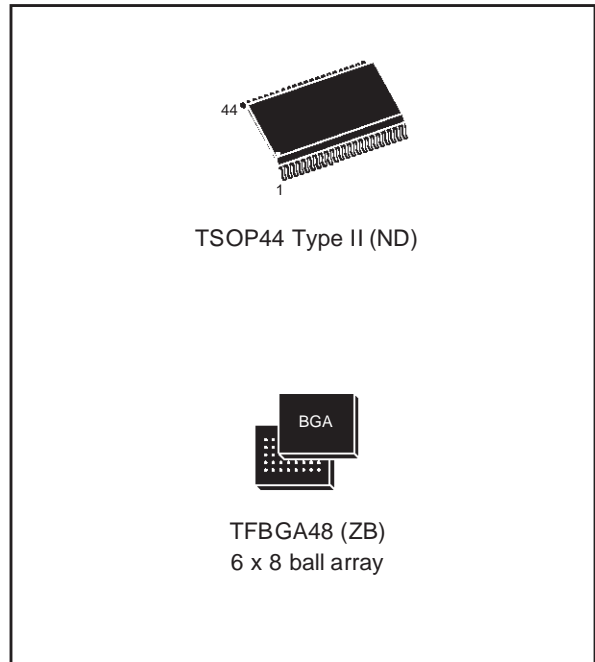
# M68AW256M M68AW256ML

4 Mbit (256K x16) 3.0V Asynchronous SRAM

## FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.6V
- 256K x 16 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIME: 55ns
- LOW STANDBY CURRENT
- LOW  $V_{CC}$  DATA RETENTION: 1.0V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN

Figure 1. Packages



**TABLE OF CONTENTS**

**SUMMARY DESCRIPTION** ..... **3**

    Figure 2. Logic Diagram ..... 3

    Table 1. Signal Names ..... 3

    Figure 3. TSOP Connections. .... 4

    Figure 4. TFBGA Connections (Top view through package). .... 5

    Figure 5. Block Diagram ..... 6

**MAXIMUM RATING** ..... **6**

    Table 2. Absolute Maximum Ratings. .... 6

**DC AND AC PARAMETERS** ..... **7**

    Table 3. Operating and AC Measurement Conditions. .... 7

    Figure 6. AC Measurement I/O Waveform ..... 7

    Figure 7. AC Measurement Load Circuit. .... 7

    Table 4. Capacitance. .... 8

    Table 5. DC Characteristics. .... 8

**OPERATION** ..... **9**

    Table 6. Operating Modes ..... 9

    Read Mode ..... 9

    Figure 8. Address Controlled, Read Mode AC Waveforms. .... 9

    Figure 9. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms. .... 10

    Figure 10. Chip Enable or UB/LB Controlled, Standby Mode AC Waveforms ..... 10

    Table 7. Read and Standby Mode AC Characteristics ..... 11

    Write Mode ..... 12

    Figure 11. Write Enable Controlled, Write AC Waveforms ..... 12

    Figure 12. Chip Enable Controlled, Write AC Waveforms. .... 13

    Figure 13. UB/LB Controlled, Write AC Waveforms ..... 13

    Table 8. Write Mode AC Characteristics ..... 14

    Figure 14. Low  $V_{CC}$  Data Retention AC Waveforms ..... 15

    Table 9. Low  $V_{CC}$  Data Retention Characteristics. .... 15

**PACKAGE MECHANICAL** ..... **16**

    TSOP44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Outline ..... 16

    TSOP 44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Mechanical Data ..... 16

    TFBGA48 - 6 x 8 ball array, 0.75 mm pitch, Bottom View Package Outline ..... 17

    TFBGA48 - 6 x 8 ball array, 0.75 mm pitch, Package Mechanical Data ..... 17

**PART NUMBERING** ..... **18**

    Table 12. Ordering Information Scheme ..... 18

**REVISION HISTORY** ..... **18**

    Table 13. Document Revision History ..... 18

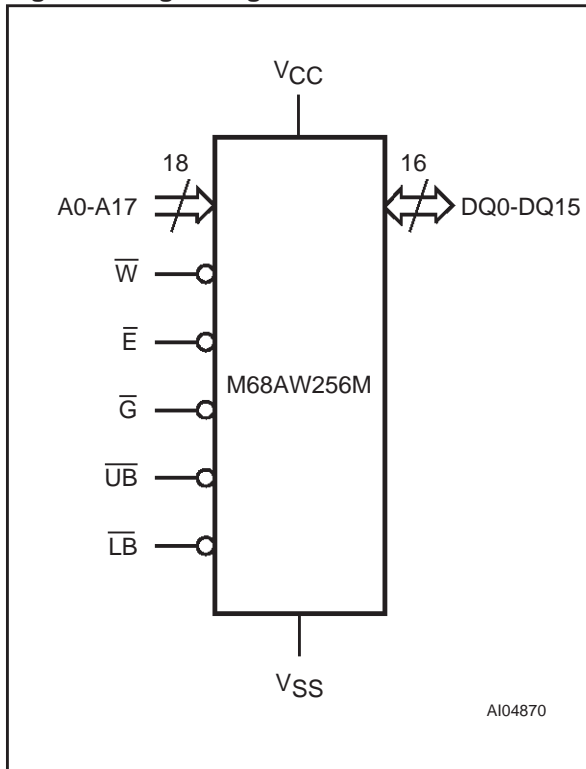
**SUMMARY DESCRIPTION**

The M68AW256M is a 4 Mbit (4,194,304 bit) CMOS SRAM, organized as 262,144 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.7 to 3.6V supply. This device has an au-

tomatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AW256 is available in TFBGA48 (0.75 mm pitch) and in TSOP44 Type II packages.

**Figure 2. Logic Diagram**



**Table 1. Signal Names**

A0-A17	Address Inputs
DQ0-DQ15	Data Input/Output
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{W}$	Write Enable
$\bar{UB}$	Upper Byte Enable Input
$\bar{LB}$	Lower Byte Enable Input
Vcc	Supply Voltage
Vss	Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Figure 3. TSOP Connections

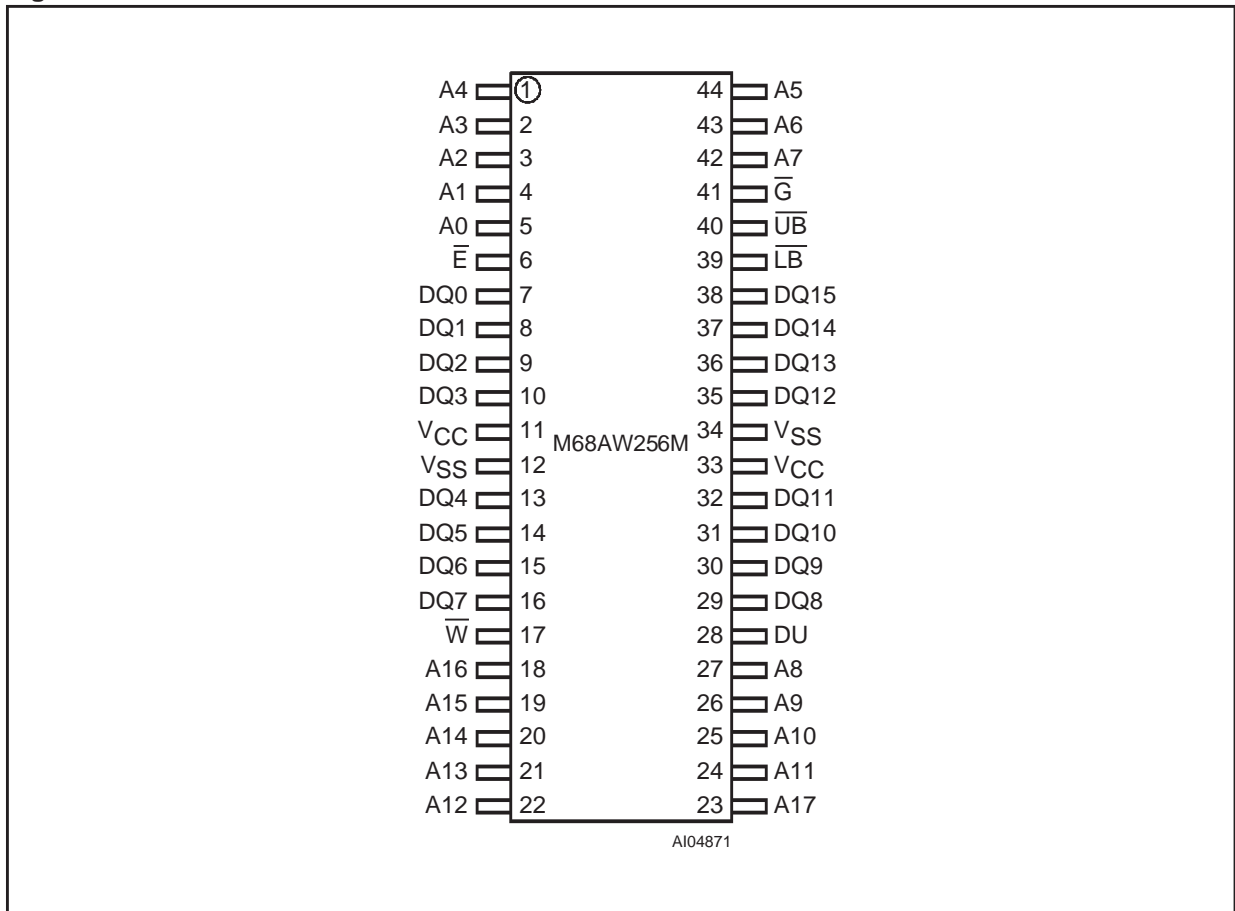


Figure 4. TFBGA Connections (Top view through package)

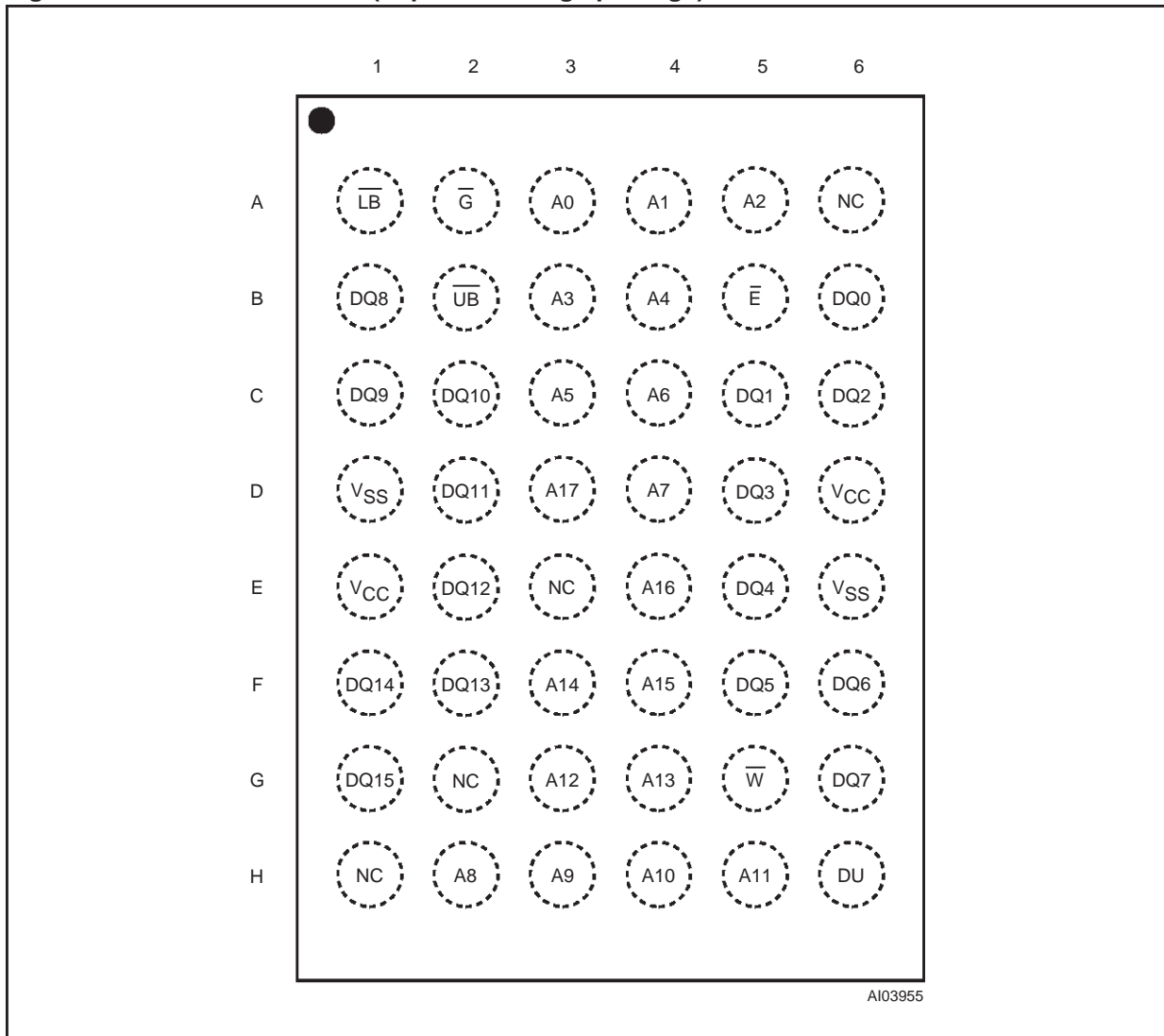
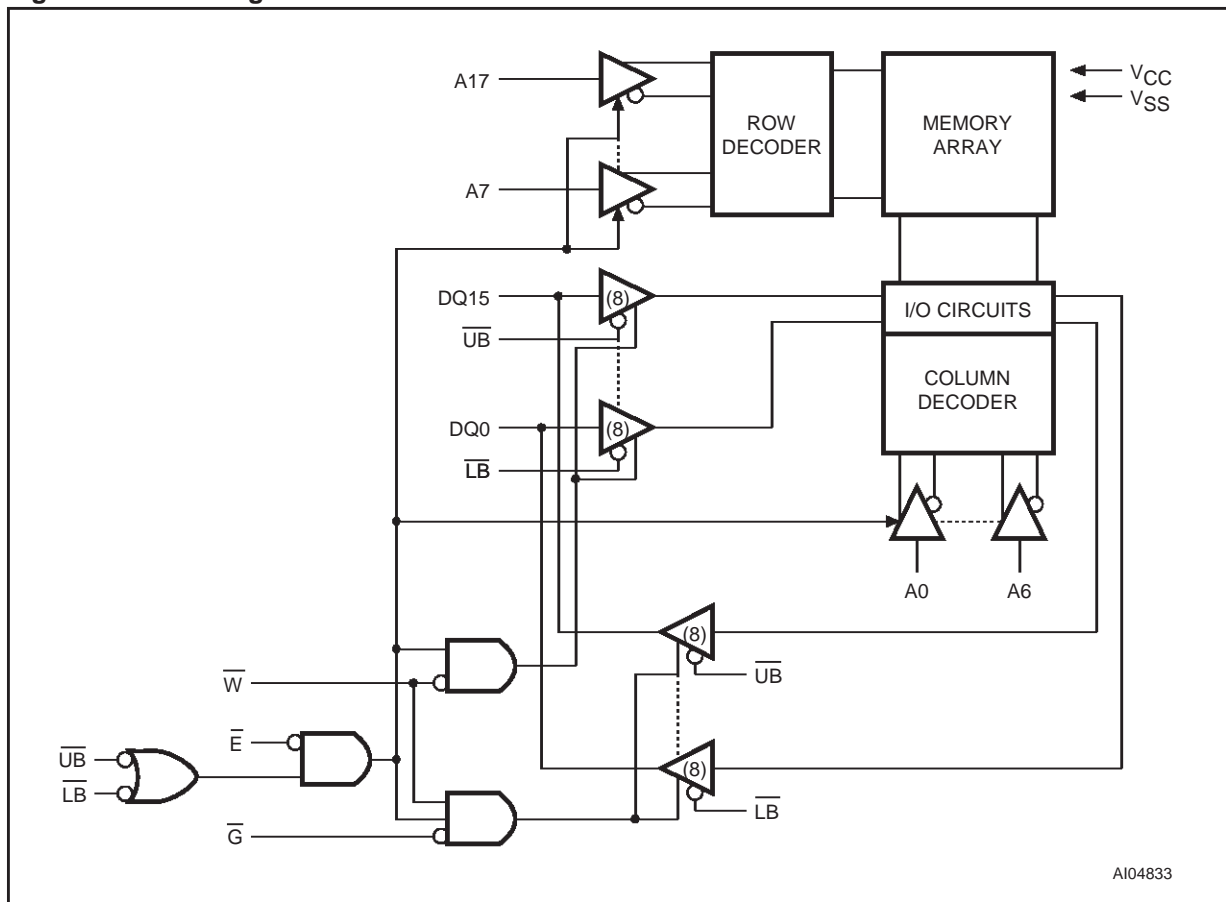


Figure 5. Block Diagram



**MAXIMUM RATING**

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$I_O^{(1)}$	Output Current	20	mA
$T_A$	Ambient Operating Temperature	-55 to 125	°C
$T_{STG}$	Storage Temperature	-65 to 150	°C
$V_{CC}$	Supply Voltage	-0.5 to 4.6	V
$V_{IO}^{(2)}$	Input or Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$P_D$	Power Dissipation	1	W

Note: 1. One output at a time, not to exceed 1 second duration.  
 2. Up to a maximum operating  $V_{CC}$  of 3.6V only.

**DC AND AC PARAMETERS**

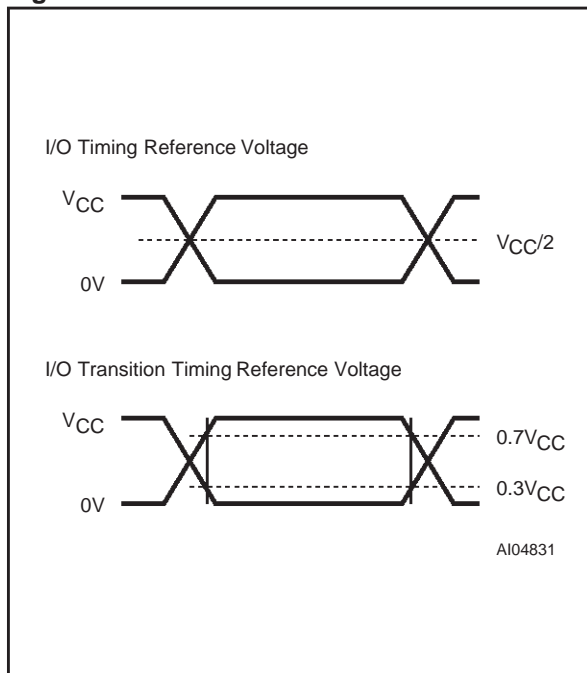
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

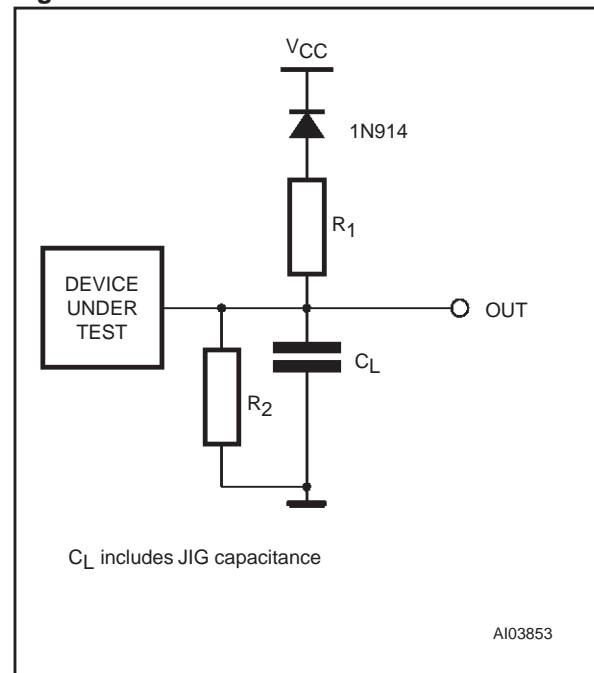
**Table 3. Operating and AC Measurement Conditions**

Parameter	M68AW256M
V <sub>CC</sub> Supply Voltage	2.7 to 3.6V
Ambient Operating Temperature	-40 to 85°C
Load Capacitance (C <sub>L</sub> )	30 or 5pF
Output Circuit Protection Resistance (R <sub>1</sub> )	1.10kΩ
Load Resistance (R <sub>2</sub> )	1.55kΩ
Input Rise and Fall Times	≤ 4ns
Input Pulse Voltages	0 to V <sub>CC</sub>
Input and Output Timing Ref. Voltages	V <sub>CC</sub> /2
Input and Output Transition Timing Ref. Voltages	V <sub>OL</sub> = 0.3V <sub>CC</sub> ; V <sub>OH</sub> = 0.7V <sub>CC</sub>

**Figure 6. AC Measurement I/O Waveform**



**Figure 7. AC Measurement Load Circuit**



## M68AW256M, M68AW256ML

**Table 4. Capacitance**

Symbol	Parameter <sup>(1,2)</sup>	Test Condition	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance on all pins (except DQ)	V <sub>IN</sub> = 0V		6	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance	V <sub>OUT</sub> = 0V		8	pF

Note: 1. Sampled only, not 100% tested.  
 2. At T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 3.0V.  
 3. Outputs deselected.

**Table 5. DC Characteristics**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I <sub>CC1</sub> <sup>(1)</sup>	Operating Supply Current	V <sub>CC</sub> = 3.6V, f = 1/t <sub>AVAV</sub> , I <sub>OUT</sub> = 0mA		7	15	mA
I <sub>CC2</sub>	Operating Supply Current	V <sub>CC</sub> = 3.6V, f = 1MHz, I <sub>OUT</sub> = 0mA		1	2	mA
I <sub>SB</sub> <sup>(2)</sup>	Standby Supply Current CMOS (M68AW256M)	V <sub>CC</sub> = 3.6V, Ē ≥ V <sub>CC</sub> - 0.15V, f = 0		20		μA
	Standby Supply Current CMOS (M68AW256ML)			2		μA
I <sub>LI</sub>	Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1		1	μA
I <sub>LO</sub>	Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> <sup>(3)</sup>	-1		1	μA
V <sub>IH</sub>	Input High Voltage	V <sub>CC</sub> = 2.7V	2.2		V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input Low Voltage	V <sub>CC</sub> = 2.7V	-0.5		0.8	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = 2.7V, I <sub>OH</sub> = -100μA	2.4			V
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = 2.7V, I <sub>OL</sub> = 2.1mA			0.4	V

Note: 1. Average AC current, cycling at t<sub>AVAV</sub> minimum.  
 2. All other Inputs at V<sub>IL</sub> ≤ 0.15V or V<sub>IH</sub> ≥ V<sub>CC</sub> - 0.15V.  
 3. Output disabled.



**OPERATION**

The M68AW256M has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ( $\overline{E}$  = High) or LB and UB are de-asserted (LB and UB = High). An Output Enable ( $\overline{G}$ ) signal provides

a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs  $\overline{W}$ ,  $\overline{E}$ ,  $\overline{LB}$  and  $\overline{UB}$  as summarized in the Operating Modes table (see Table 6).

**Table 6. Operating Modes**

Operation	$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Deselected/Power-down	$V_{IH}$	X	X	X	X	Hi-Z	Hi-Z	Standby ( $I_{SB}$ )
Deselected/Power-down	X	X	X	$V_{IH}$	$V_{IH}$	Hi-Z	Hi-Z	Standby ( $I_{SB}$ )
Lower Byte Read	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	Data Output	Hi-Z	Active ( $I_{CC}$ )
Lower Byte Write	$V_{IL}$	$V_{IL}$	X	$V_{IL}$	$V_{IH}$	Data Input	Hi-Z	Active ( $I_{CC}$ )
Output Disabled	$V_{IL}$	X	$V_{IH}$	$V_{IL}$	X	Hi-Z	Hi-Z	Active ( $I_{CC}$ )
Output Disabled	$V_{IL}$	X	$V_{IH}$	X	$V_{IL}$	Hi-Z	Hi-Z	Active ( $I_{CC}$ )
Upper Byte Read	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	Hi-Z	Data Output	Active ( $I_{CC}$ )
Upper Byte Write	$V_{IL}$	$V_{IL}$	X	$V_{IH}$	$V_{IL}$	Hi-Z	Data Input	Active ( $I_{CC}$ )
Word Read	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IL}$	Data Output	Data Output	Active ( $I_{CC}$ )
Word Write	$V_{IL}$	$V_{IL}$	X	$V_{IL}$	$V_{IL}$	Data Input	Data Input	Active ( $I_{CC}$ )

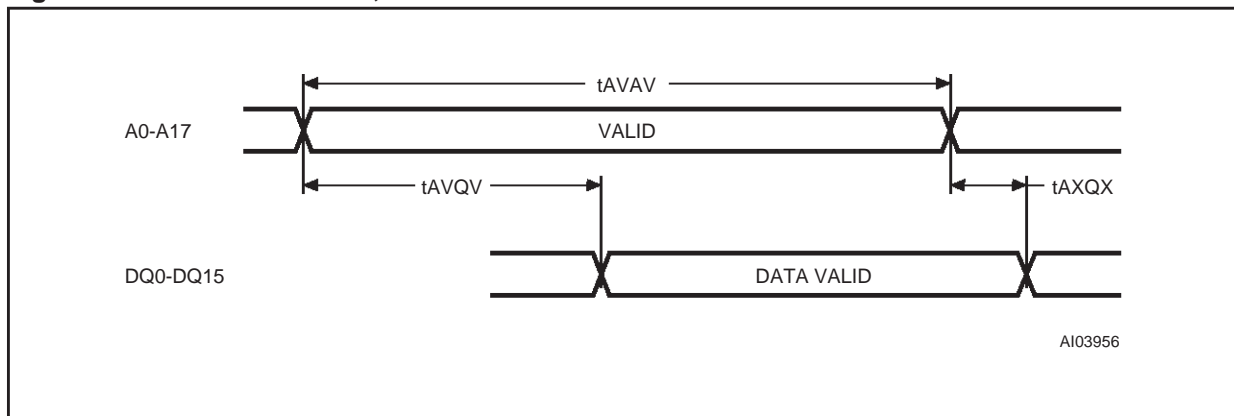
Note: 1. X =  $V_{IH}$  or  $V_{IL}$ .

**Read Mode**

The M68AW256M is in the Read mode whenever Write Enable ( $\overline{W}$ ) is High with Output Enable ( $\overline{G}$ ) Low, and Chip Enable ( $\overline{E}$ ) is asserted. This provides access to data from eight or sixteen, depending on the status of the signal UB and LB, of the 4,194,304 locations in the static memory array, specified by the 18 address inputs. Valid data will be available at the eight or sixteen output pins

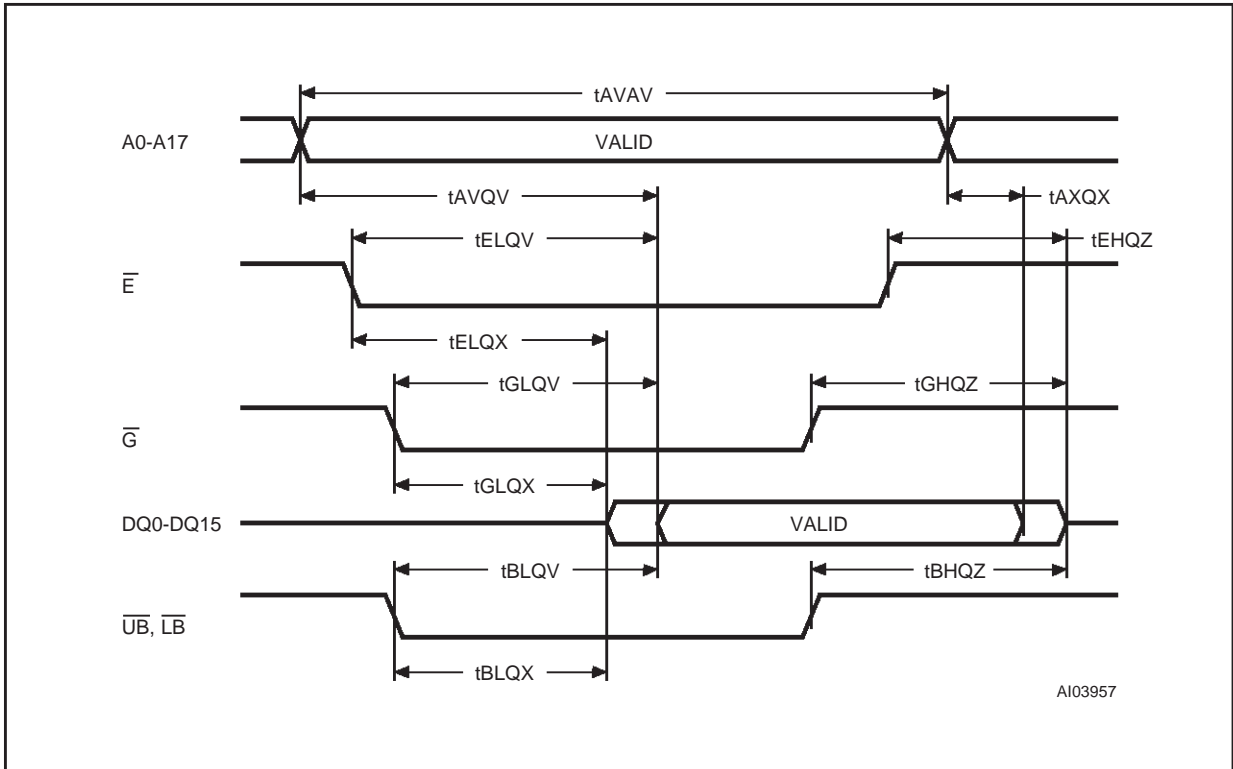
within  $t_{AVQV}$  after the last stable address, providing  $\overline{G}$  is Low and  $\overline{E}$  is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter ( $t_{ELQV}$ ,  $t_{GLQV}$  or  $t_{BLQV}$ ) rather than the address. Data out may be indeterminate at  $t_{ELQX}$ ,  $t_{GLQX}$  and  $t_{BLQX}$  but data lines will always be valid at  $t_{AVQV}$ .

**Figure 8. Address Controlled, Read Mode AC Waveforms**



Note:  $\overline{E}$  = Low,  $\overline{G}$  = Low,  $\overline{W}$  = High,  $\overline{UB}$  = Low and/or  $\overline{LB}$  = Low.

Figure 9. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.



Note: Write Enable ( $\bar{W}$ ) = High.

Figure 10. Chip Enable or  $\bar{UB}/\bar{LB}$  Controlled, Standby Mode AC Waveforms

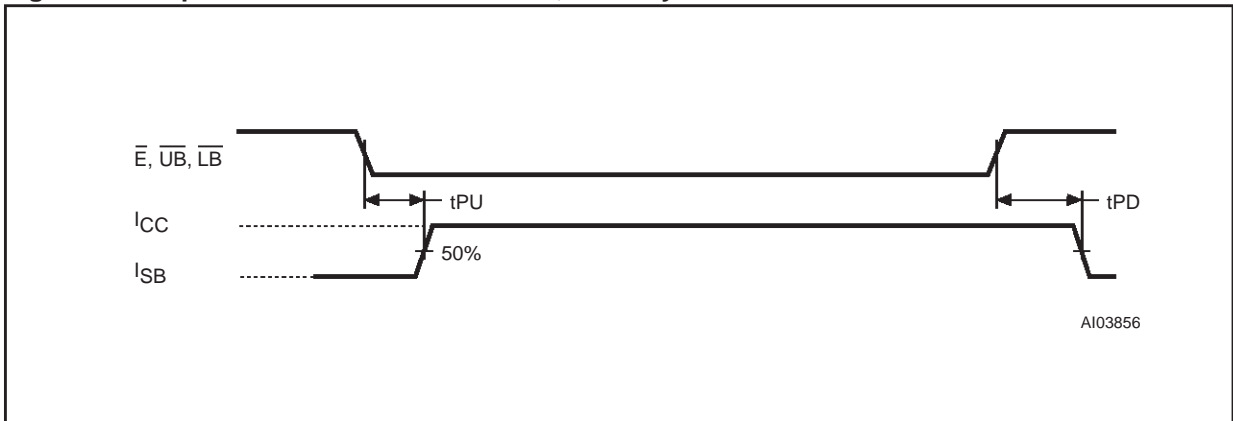


Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter		M68AW256M		Unit
			55	70	
t <sub>AVAV</sub>	Read Cycle Time	Min	55	70	ns
t <sub>AVQV</sub>	Address Valid to Output Valid	Max	55	70	ns
t <sub>AXQX</sub>	Data hold from address change	Min	10	10	ns
t <sub>BHQZ</sub> <sup>(1, 2)</sup>	Upper/Lower Byte Enable High to Output Hi-Z	Max	20	20	ns
t <sub>BLQV</sub>	Upper/Lower Byte Enable Low to Output Valid	Max	55	70	ns
t <sub>BLQX</sub>	Upper/Lower Byte Enable Low to Output Transition	Min	5	10	ns
t <sub>EHQZ</sub> <sup>(1, 2)</sup>	Chip Enable High to Output Hi-Z	Max	20	25	ns
t <sub>ELQV</sub>	Chip Enable Low to Output Valid	Max	55	70	ns
t <sub>ELQX</sub>	Chip Enable Low to Output Transition	Min	10	10	ns
t <sub>GHQZ</sub> <sup>(1, 2)</sup>	Output Enable High to Output Hi-Z	Max	20	25	ns
t <sub>GLQV</sub>	Output Enable Low to Output Valid	Max	20	35	ns
t <sub>GLQX</sub>	Output Enable Low to Output Transition	Min	5	5	ns
t <sub>PD</sub>	Chip Enable or $\overline{UB}/\overline{LB}$ High to Power Down	Max	55	70	ns
t <sub>PU</sub>	Chip Enable or $\overline{UB}/\overline{LB}$ Low to Power Up	Min	0	0	ns

Note: 1. At any given temperature and voltage condition, t<sub>GHQZ</sub> is less than t<sub>GLQX</sub>, t<sub>BHQZ</sub> is less than t<sub>BLQX</sub> and t<sub>EHQZ</sub> is less than t<sub>ELQX</sub> for any given device.

2. C<sub>L</sub> = 5pF.

**Write Mode**

The M68AW256M is in the Write mode whenever the  $\overline{W}$  and  $\overline{E}$  are Low. Either the Chip Enable input ( $\overline{E}$ ) or the Write Enable input ( $\overline{W}$ ) must be deasserted during Address transitions for subsequent write cycles. When  $\overline{E}$  ( $\overline{W}$ ) is Low, and  $\overline{UB}$  or  $\overline{LB}$  is Low, write cycle begins on the  $\overline{W}$  ( $\overline{E}$ )'s falling edge. When  $\overline{E}$  and  $\overline{W}$  are Low, and  $\overline{UB} = \overline{LB} = \text{High}$ , write cycle begins on the first falling edge of  $\overline{UB}$  or  $\overline{LB}$ . Therefore, address setup time is referenced to Write Enable, Chip Enable or  $\overline{UB}/\overline{LB}$  as  $t_{AVWL}$ ,  $t_{AVEL}$  and  $t_{AVBL}$  respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of  $\overline{E}$ ,  $\overline{W}$  or  $\overline{UB}/\overline{LB}$ .

If the Output is enabled ( $\overline{E} = \text{Low}$ ,  $\overline{G} = \text{Low}$ ,  $\overline{LB}$  or  $\overline{UB} = \text{Low}$ ), then  $\overline{W}$  will return the outputs to high impedance within  $t_{WLQZ}$  of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for  $t_{DVWH}$  before the rising edge of Write Enable, or for  $t_{WDHX}$  before the rising edge of  $\overline{E}$ , or for  $t_{DVBH}$  before the rising edge of  $\overline{UB}/\overline{LB}$  whichever occurs first, and remain valid for  $t_{WHDX}$ ,  $t_{EHDX}$  and  $t_{BHDX}$  respectively.

**Figure 11. Write Enable Controlled, Write AC Waveforms**

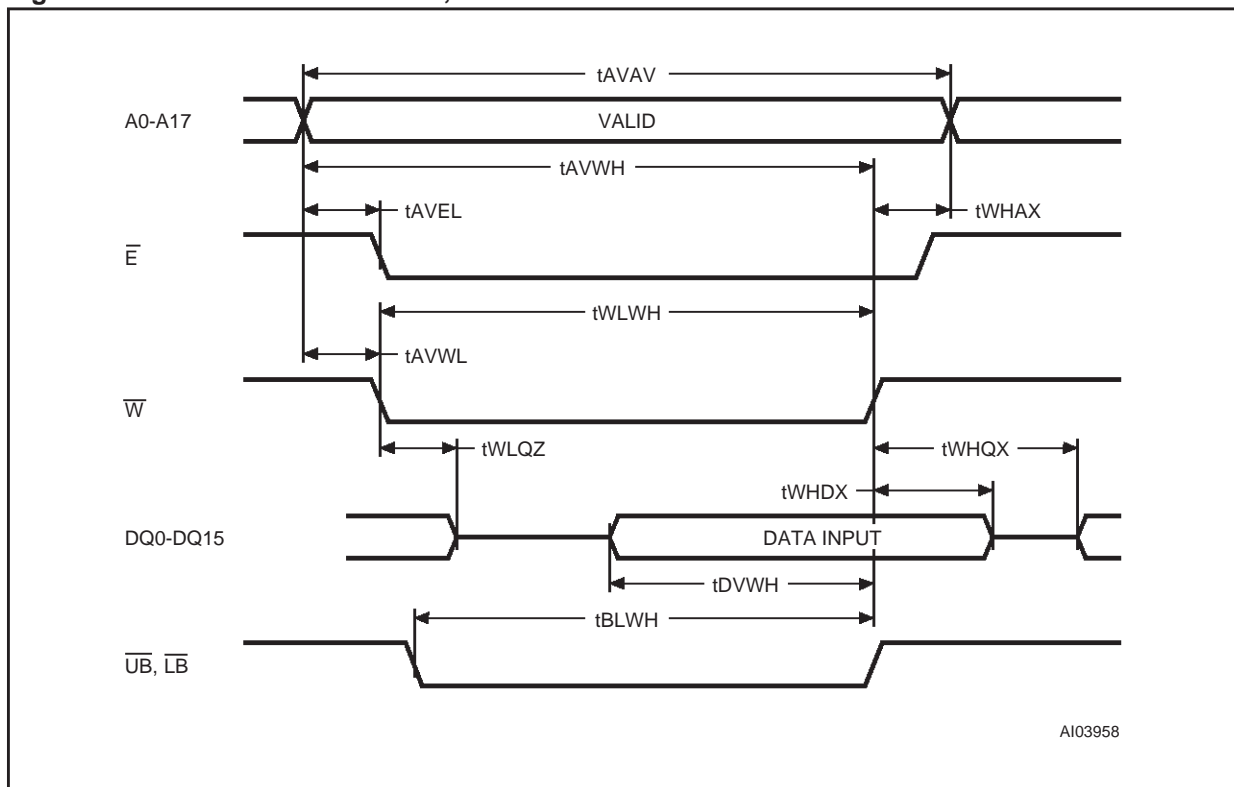


Figure 12. Chip Enable Controlled, Write AC Waveforms

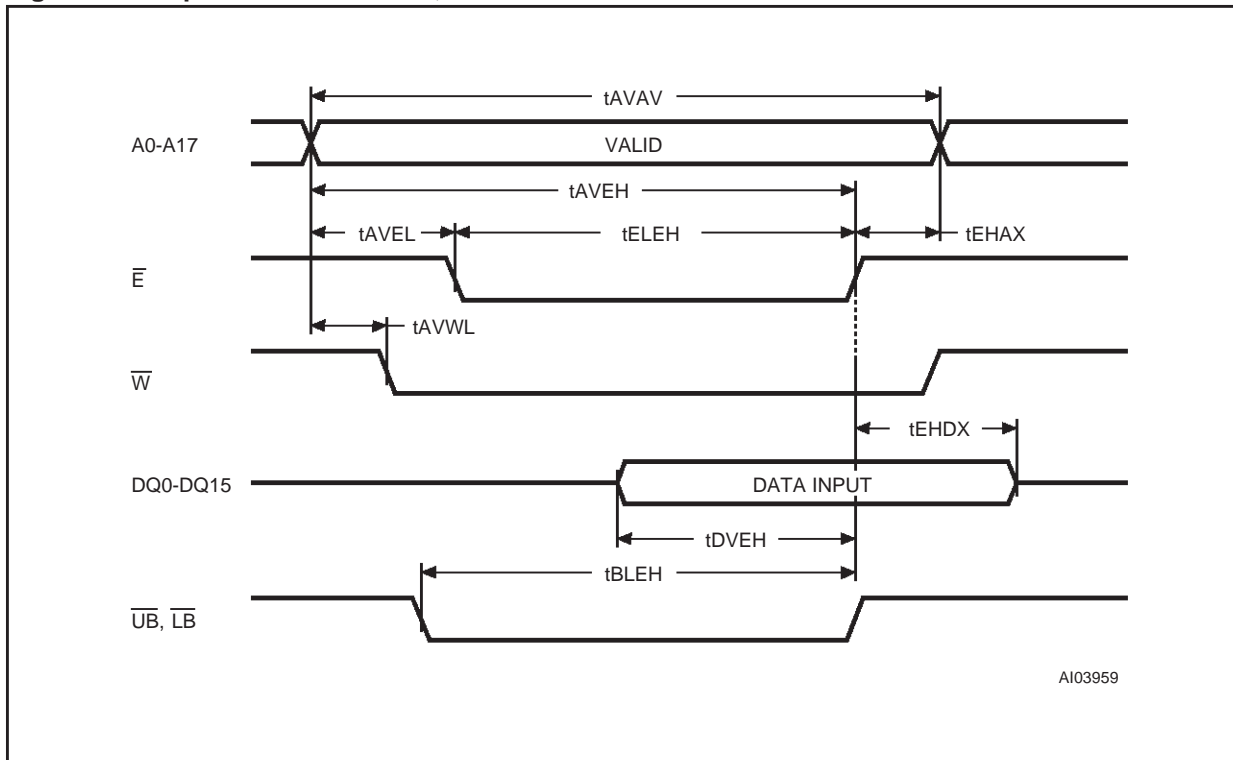
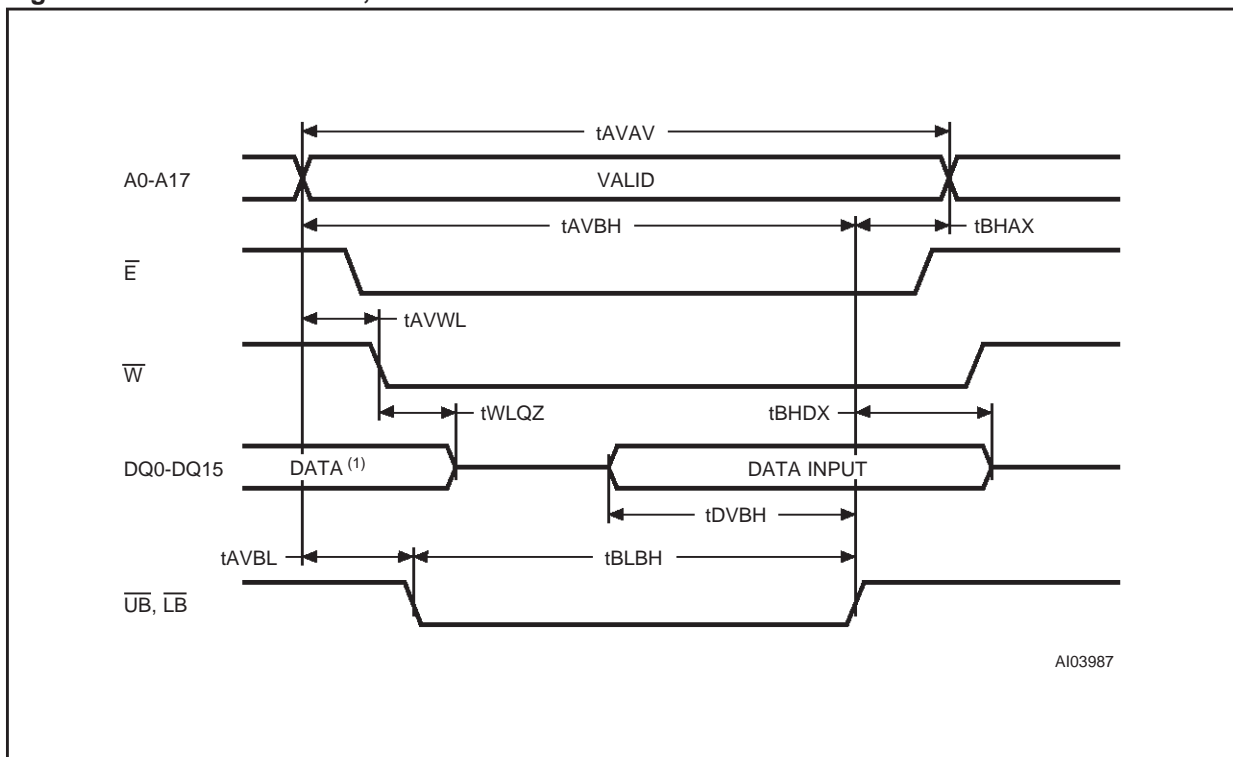


Figure 13.  $\bar{UB}/\bar{LB}$  Controlled, Write AC Waveforms



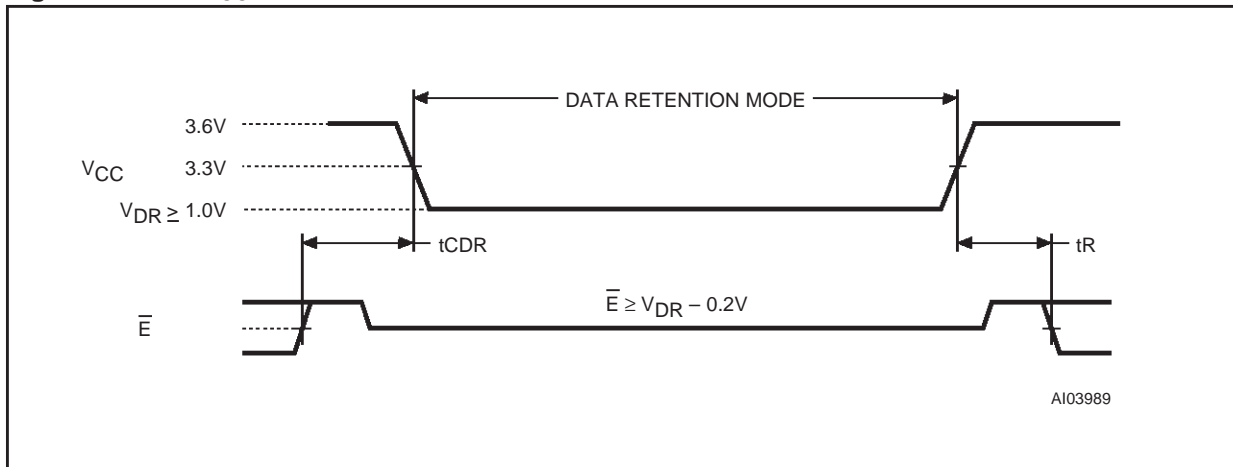
Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

**Table 8. Write Mode AC Characteristics**

Symbol	Parameter		M68AW256M		Unit
			55	70	
t <sub>AVAV</sub>	Write Cycle Time	Min	55	70	ns
t <sub>AVBH</sub>	Address Valid to $\overline{LB}$ , $\overline{UB}$ High	Min	40	60	ns
t <sub>AVBL</sub>	Address Valid to $\overline{LB}$ , $\overline{UB}$ Low	Min	0	0	ns
t <sub>AVEH</sub>	Address Valid to Chip Enable High	Min	40	60	ns
t <sub>AVEL</sub>	Address valid to Chip Enable Low	Min	0	0	ns
t <sub>AVWH</sub>	Address Valid to Write Enable High	Min	40	60	ns
t <sub>AVWL</sub>	Address Valid to Write Enable Low	Min	0	0	ns
t <sub>BHAX</sub>	$\overline{LB}$ , $\overline{UB}$ High to Address Transition	Min	0	0	ns
t <sub>BHDX</sub>	$\overline{LB}$ , $\overline{UB}$ High to Input Transition	Min	0	0	ns
t <sub>BLBH</sub>	$\overline{LB}$ , $\overline{UB}$ Low to $\overline{LB}$ , $\overline{UB}$ High	Min	40	60	ns
t <sub>BLEH</sub>	$\overline{LB}$ , $\overline{UB}$ Low to Chip Enable High	Min	40	60	ns
t <sub>BLWH</sub>	$\overline{LB}$ , $\overline{UB}$ Low to Write Enable High	Min	40	60	ns
t <sub>DVBH</sub>	Input Valid to $\overline{LB}$ , $\overline{UB}$ High	Min	20	25	ns
t <sub>DVEH</sub>	Input Valid to Chip Enable High	Min	20	25	ns
t <sub>DVWH</sub>	Input Valid to Write Enable High	Min	20	25	ns
t <sub>EHAX</sub>	Chip Enable High to Address Transition	Min	0	0	ns
t <sub>EHDX</sub>	Chip enable High to Input Transition	Min	0	0	ns
t <sub>ELEH</sub>	Chip Enable Low to Chip Enable High	Min	40	60	ns
t <sub>WHAX</sub>	Write Enable High to Address Transition	Min	0	0	ns
t <sub>WHDX</sub>	Write Enable High to Input Transition	Min	0	0	ns
t <sub>WHQX</sub> <sup>(1)</sup>	Write Enable High to Output Transition	Min	5	5	ns
t <sub>WLQZ</sub> <sup>(1,2)</sup>	Write Enable Low to Output Hi-Z	Max	20	20	ns
t <sub>WLWH</sub>	Write Enable Low to Write Enable High	Min	40	50	ns

Note: 1. At any given temperature and voltage condition, t<sub>WLQZ</sub> is less than t<sub>WHQX</sub> for any given device.

2. C<sub>L</sub> = 5pF.

Figure 14. Low  $V_{CC}$  Data Retention AC WaveformsTable 9. Low  $V_{CC}$  Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$I_{CCDR}^{(1)}$	Supply Current (Data Retention) (M68AW256M)	$V_{CC} = 1.0V, \bar{E} \geq V_{CC} - 0.3V, f = 0^{(3)}$		10	20	$\mu A$
	Supply Current (Data Retention) (M68AW256ML)	$V_{CC} = 1.0V, \bar{E} \geq V_{CC} - 0.3V, f = 0^{(3)}$		0.1	1	$\mu A$
$t_{CDR}^{(1,2)}$	Chip Deselected to Data Retention Time	$\bar{E} \geq V_{CC} - 0.3V, f = 0$	0			ns
$t_R^{(2)}$	Operation Recovery Time		$t_{AVAV}$			ns
$V_{DR}^{(1)}$	Supply Voltage (Data Retention)	$\bar{E} \geq V_{CC} - 0.3V, f = 0$	1.0		3.6	V

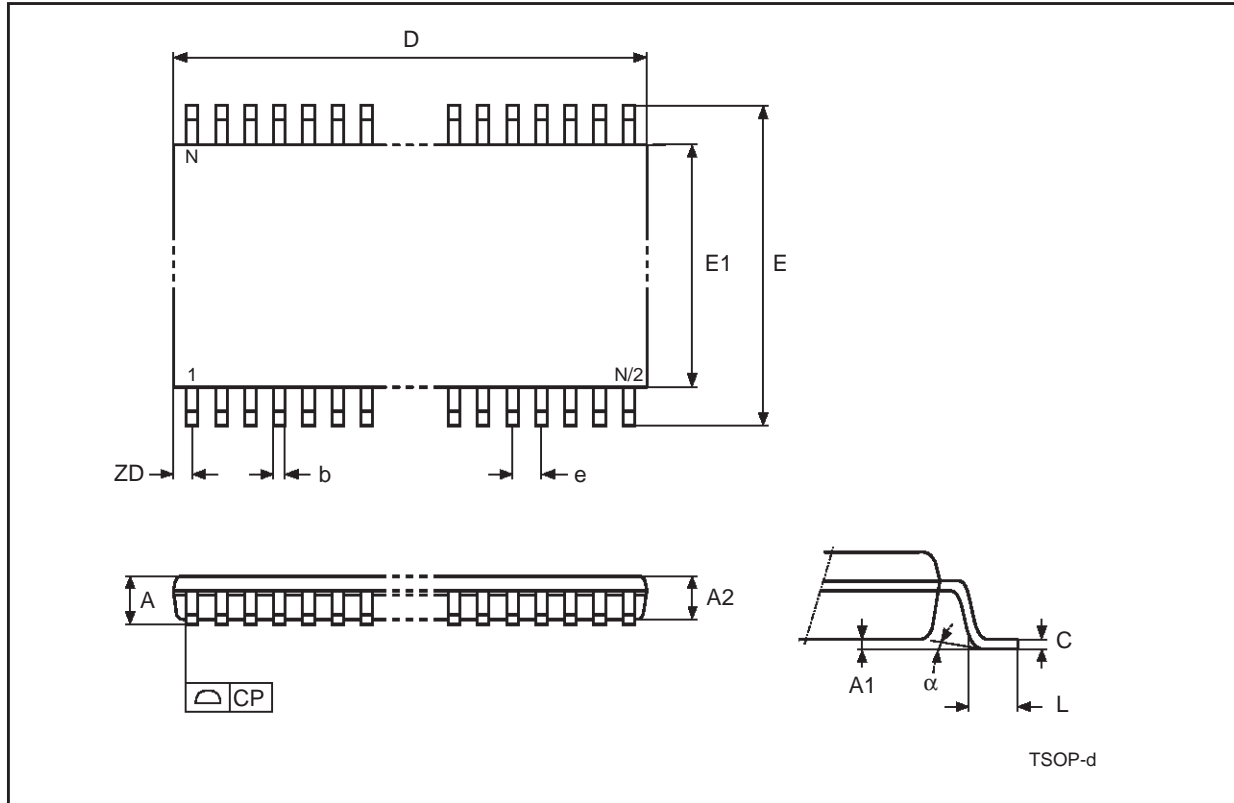
Note: 1. All other Inputs at  $V_{IH} \geq V_{CC} - 0.2V$  or  $V_{IL} \leq 0.2V$ .

2. See Figure 14 for measurement points. Guaranteed but not tested.  $t_{AVAV}$  is Read cycle time.

3. No input may exceed  $V_{CC} + 0.3V$ .

PACKAGE MECHANICAL

Figure 15. TSOP44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Outline



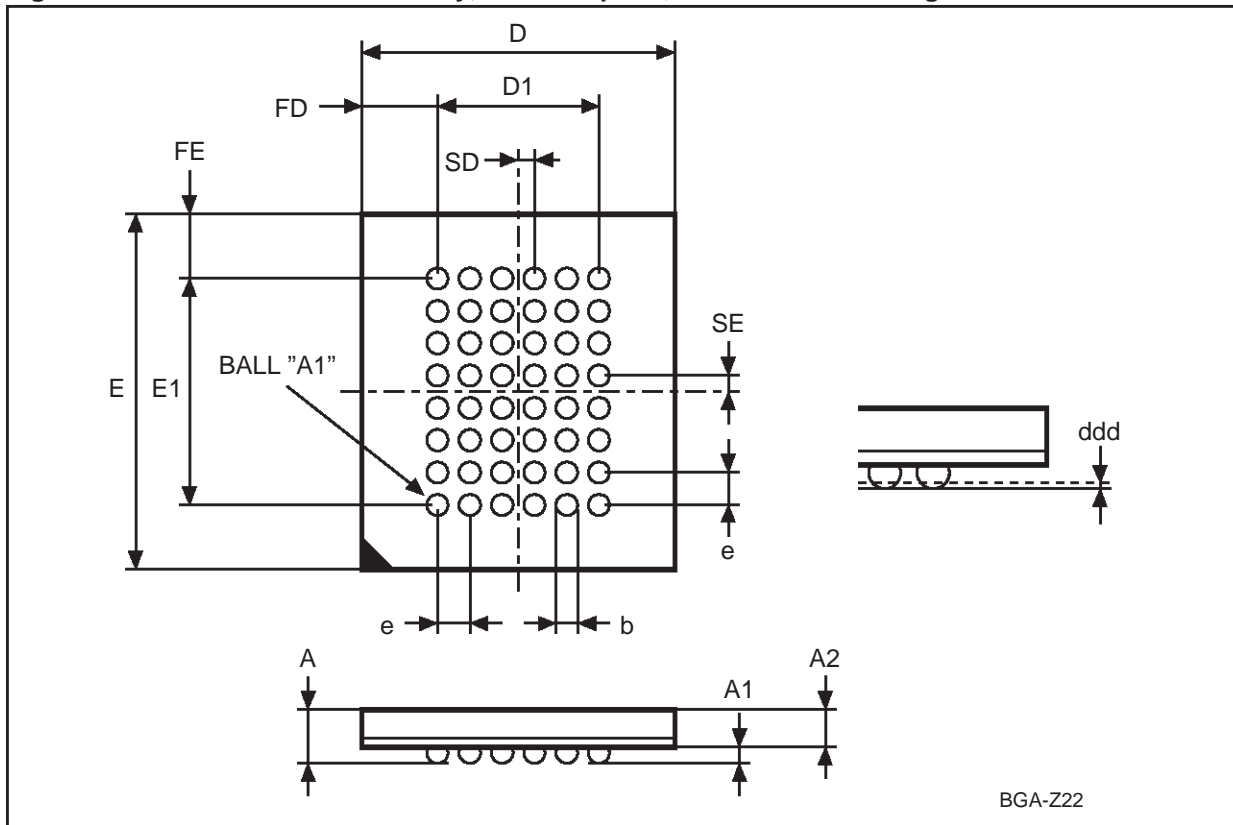
Note: Drawing is not to scale.

Table 10. TSOP 44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
b	0.350			0.0138		
c		0.120	0.210		0.0047	0.0083
D	18.410	–	–	0.7248	–	–
E	11.760	–	–	0.4630	–	–
E1	10.160	–	–	0.4000	–	–
e	0.800	–	–	0.0315	–	–
L	0.500	0.400	0.600	0.0197	0.0157	0.0236
ZD	0.805	–	–	0.0317	–	–
alfa		0	5		0	5
CP			0.100			0.0039
N	44			44		



Figure 16. TFBGA48 - 6 x 8 ball array, 0.75 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 11. TFBGA48 - 6 x 8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.010	1.200		0.0398	0.0472
A1		0.260			0.0102	
A2			0.950			0.0374
b	0.400	0.300	0.500	0.0157	0.0118	0.0197
D	7.000	6.900	7.100	0.2756	0.2717	0.2795
D1	3.750	-	-	0.1476	-	-
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	-	-	0.2067	-	-
e	0.750	-	-	0.0295	-	-
FD	1.625	-	-	0.0640	-	-
FE	1.375	-	-	0.0541	-	-
SD	0.375	-	-	0.0148	-	-
SE	0.375	-	-	0.0148	-	-



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