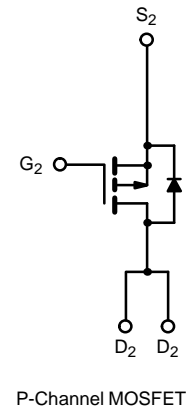
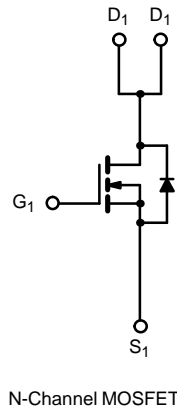
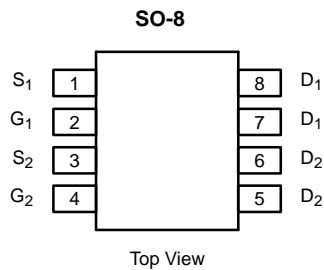




Complementary 20-V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.10 @ $V_{GS} = 10$ V	± 3.5
		0.12 @ $V_{GS} = 6$ V	± 3
		0.15 @ $V_{GS} = 4.5$ V	± 2.5
P-Channel	-20	0.10 @ $V_{GS} = -10$ V	± 3.5
		0.12 @ $V_{GS} = -6$ V	± 3
		0.19 @ $V_{GS} = -4.5$ V	± 2.5



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 20	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 3.5	A
		$T_A = 70^\circ\text{C}$	± 2.8	
Pulsed Drain Current	I_{DM}	± 14	± 14	
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	-1.7	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.0	W
		$T_A = 70^\circ\text{C}$	1.3	
Operating Junction and Storage Temperature Range	T_J, T_{Stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit		
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0			V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.0				
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = -16 V, V _{GS} = 0 V	P-Ch			-1		
		V _{DS} = 10 V, V _{GS} = 0 V, T _J = 70°C	N-Ch					5
		V _{DS} = -10 V, V _{GS} = 0 V, T _J = 70°C	P-Ch					-5
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	14			A	
		V _{DS} ≤ -5 V, V _{GS} = -10 V	P-Ch	-14				
		V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	3.5				
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	-2.5				
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 3.5 A	N-Ch			0.10	Ω	
		V _{GS} = -10 V, I _D = 3.5 A	P-Ch			0.10		
		V _{GS} = 6 V, I _D = 3 A	N-Ch			0.12		
		V _{GS} = -6 V, I _D = 3 A	P-Ch			0.12		
		V _{GS} = 4.5 V, I _D = 2 A	N-Ch			0.15		
		V _{GS} = -4.5 V, I _D = 2 A	P-Ch			0.19		
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3.5 A	N-Ch		5.6		S	
		V _{DS} = -15 V, I _D = -3.5 A	P-Ch		4.0			
Diode Forward Voltage ^b	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch		0.9	1.2	V	
		I _S = -1.7 A, V _{GS} = 0 V	P-Ch		-0.9	-1.2		
Dynamic^a								
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 3.5 A P-Channel V _{DS} = -10 V, V _{GS} = -10 V, I _D = -3.5 A	N-Ch		9	30	nC	
Gate-Source Charge	Q _{gs}		N-Ch		1.0			
Gate-Drain Charge	Q _{gd}		N-Ch		3.1			
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	N-Ch		5	10	ns	
Rise Time	t _r		N-Ch		12	25		
			P-Ch		12	25		
Turn-Off Delay Time	t _{d(off)}		N-Ch		17	30		
			P-Ch		12	30		
Fall Time	t _f		N-Ch		9	20		
			P-Ch		11	20		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3.5 A, di/dt = 100 A/μs	N-Ch		60	100		
			P-Ch		50	100		

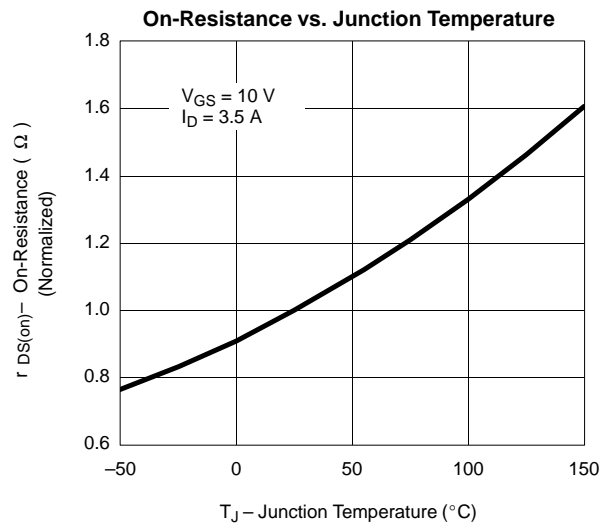
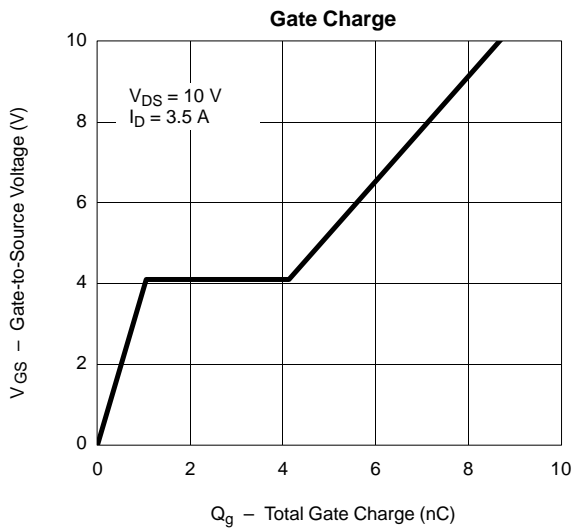
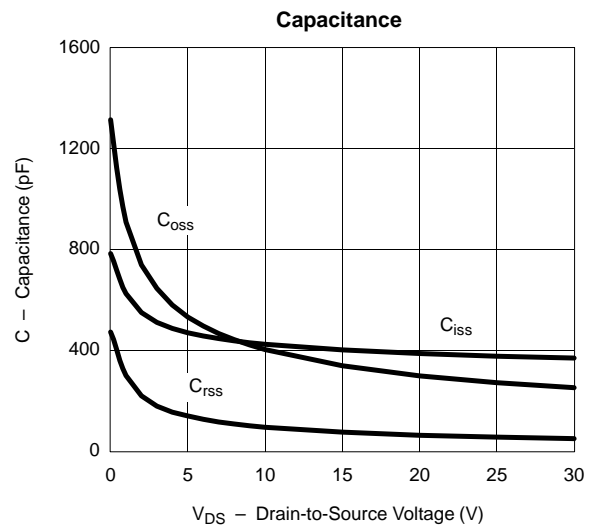
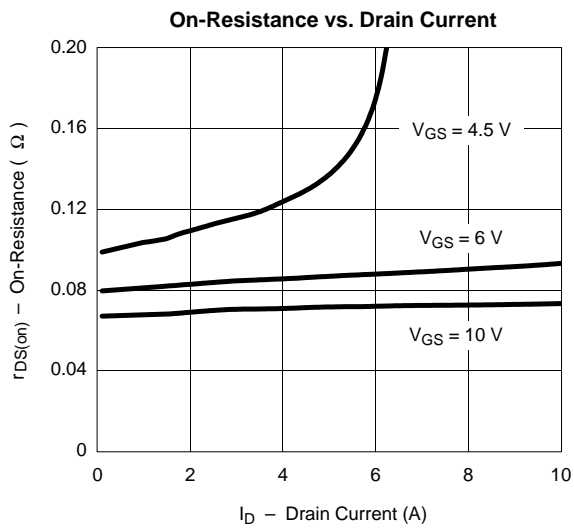
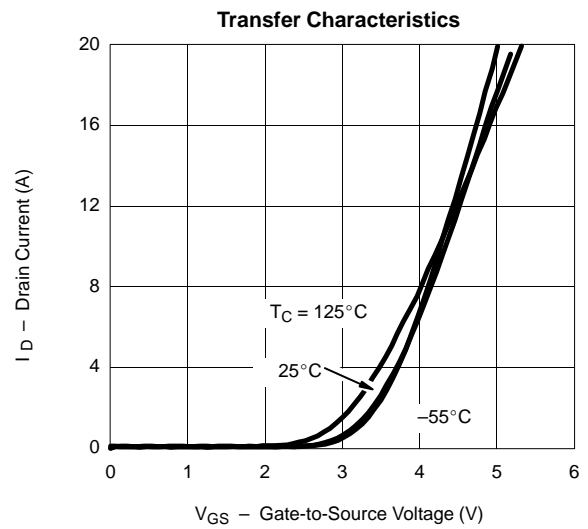
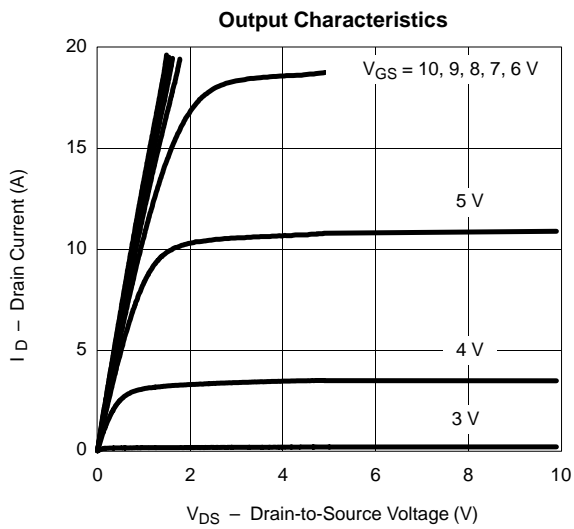
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

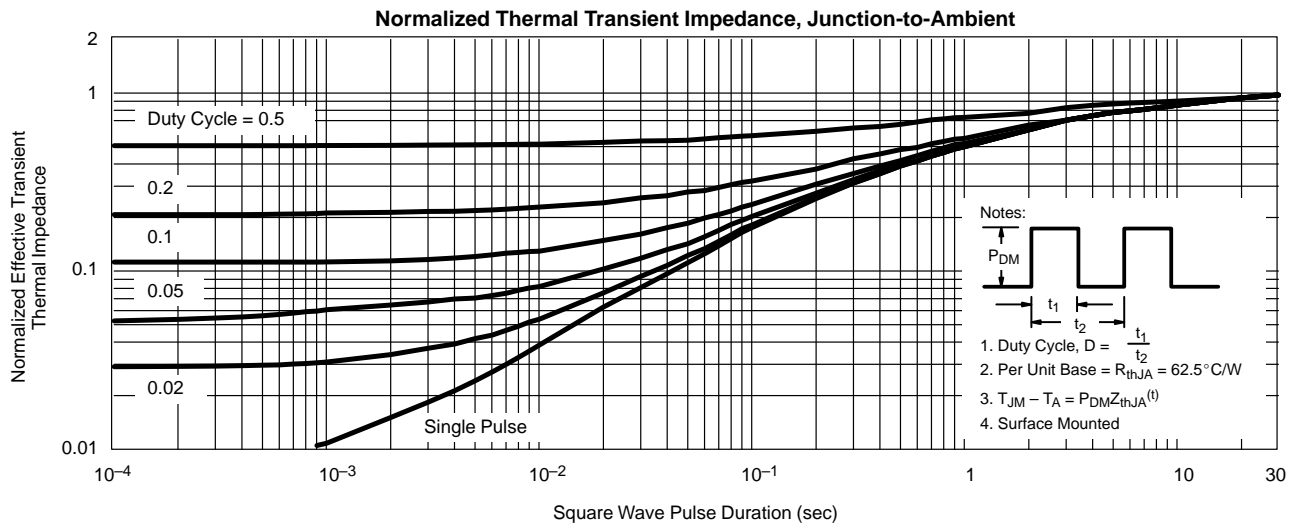
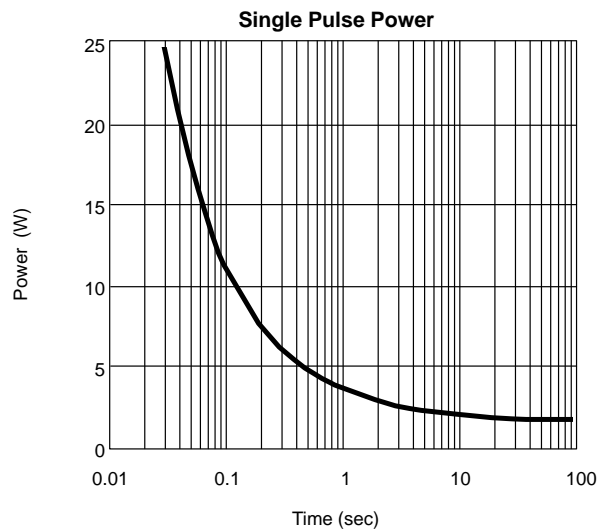
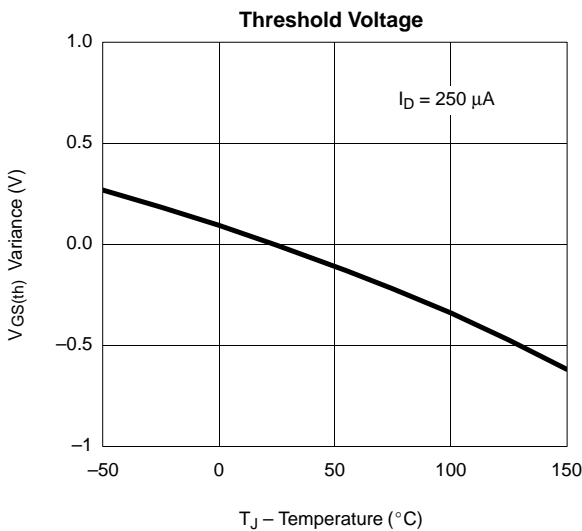
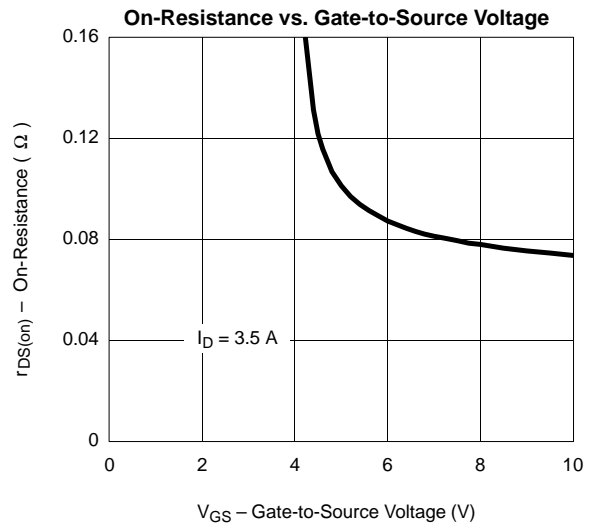
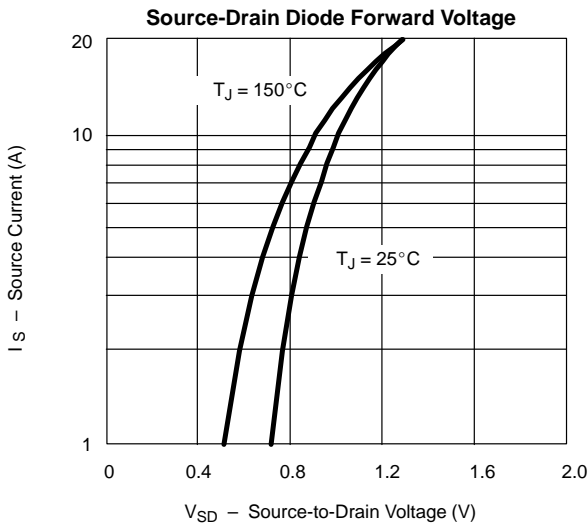


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



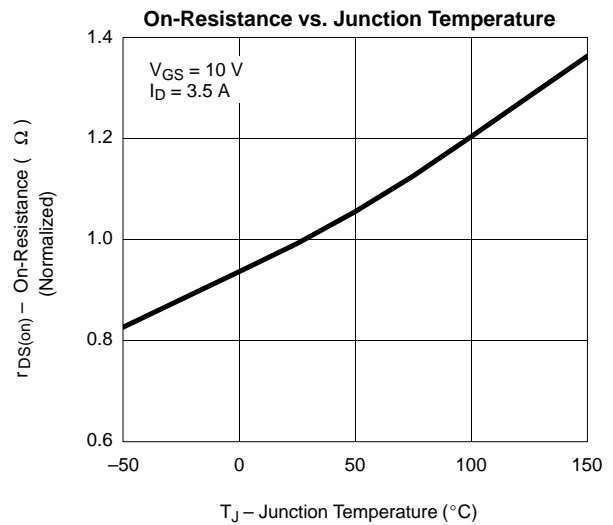
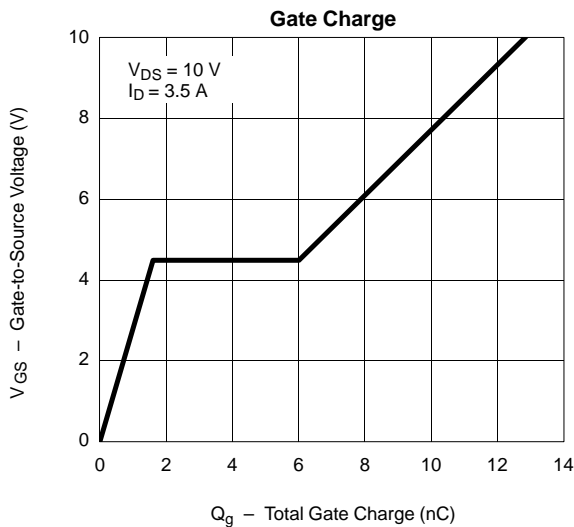
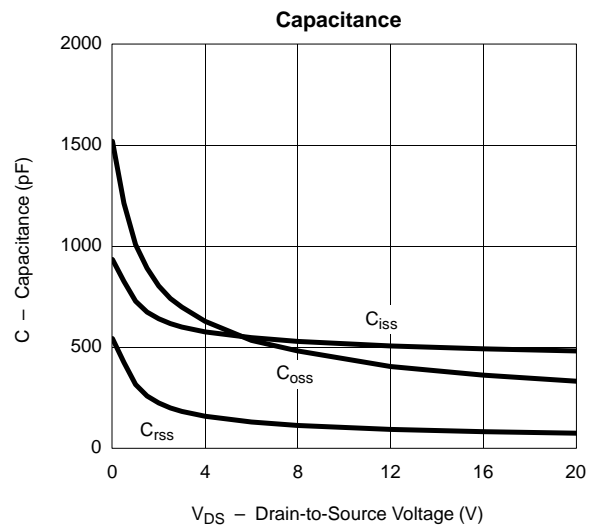
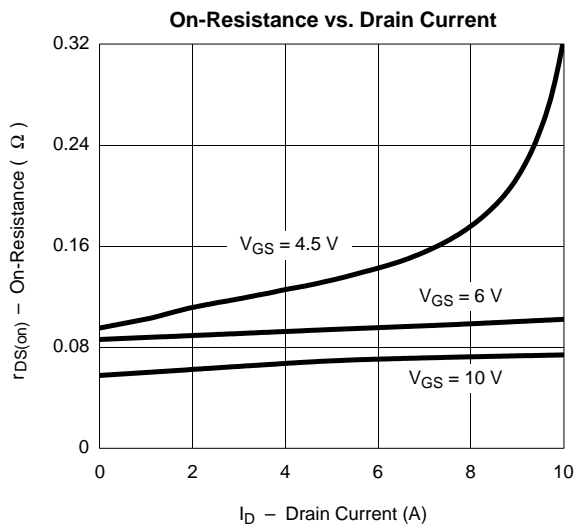
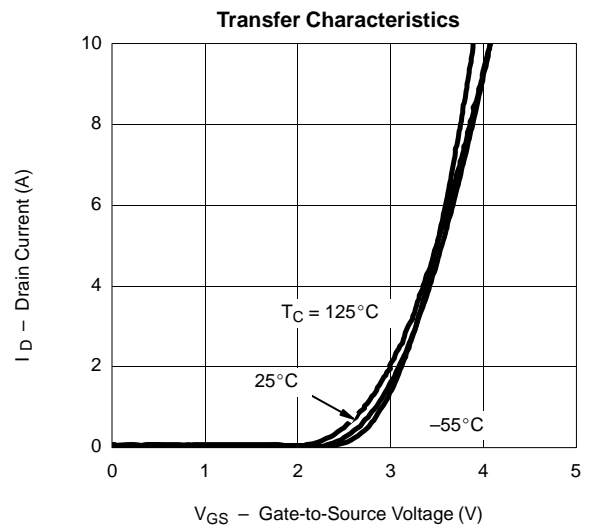
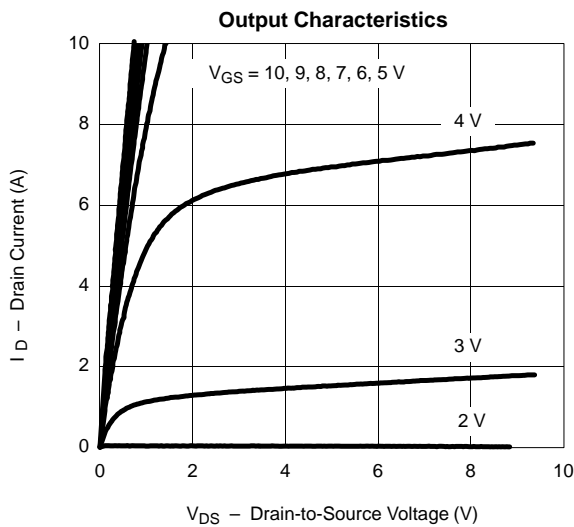
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL



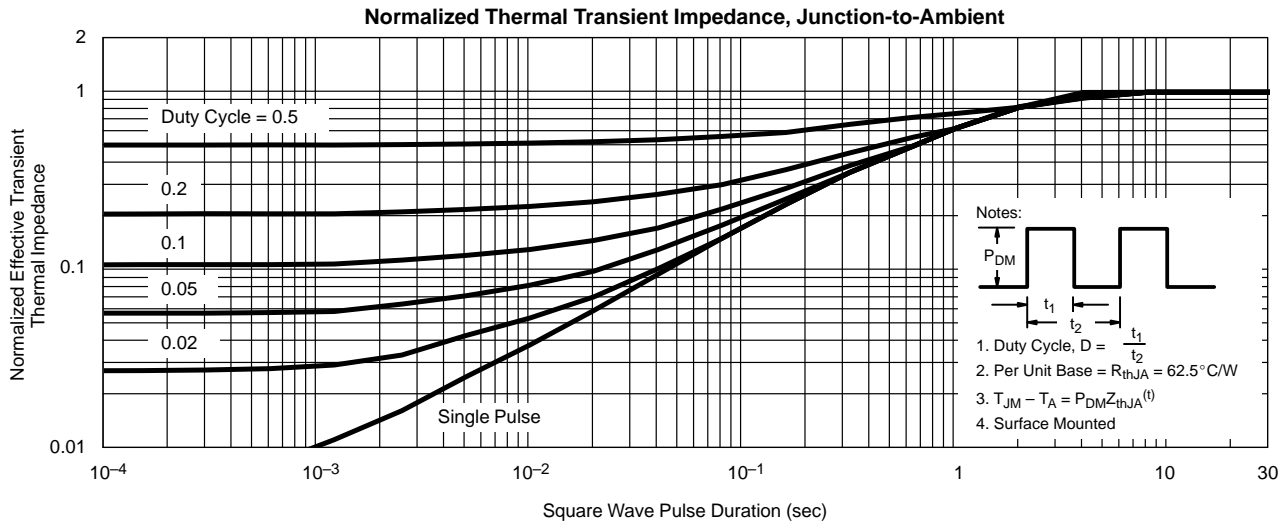
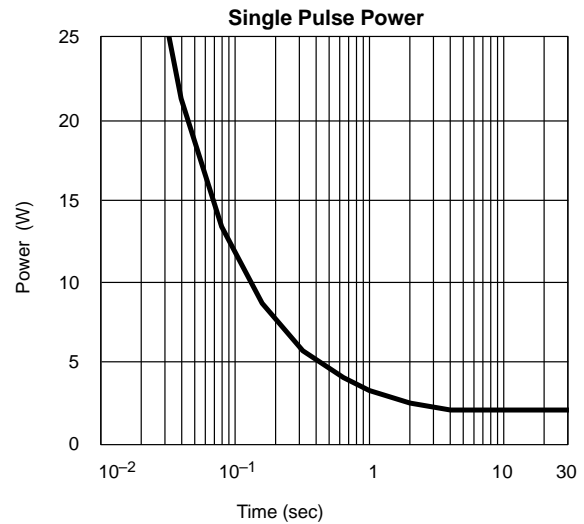
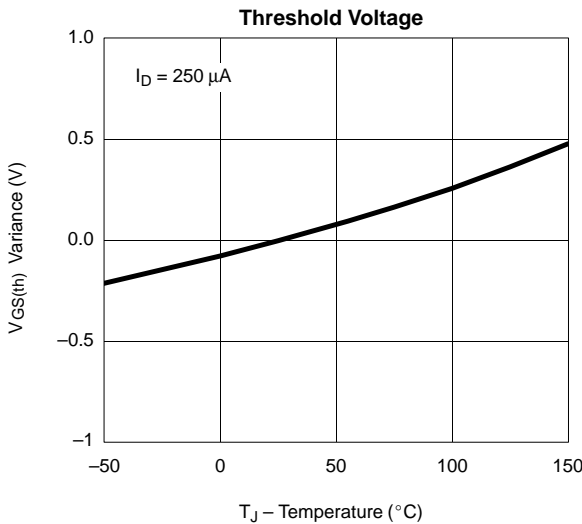
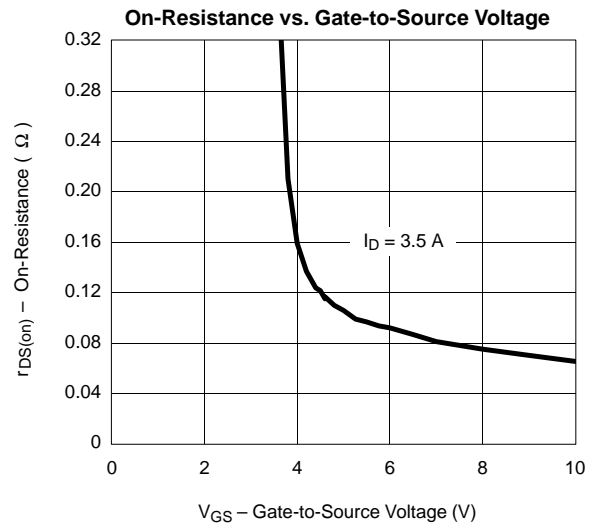
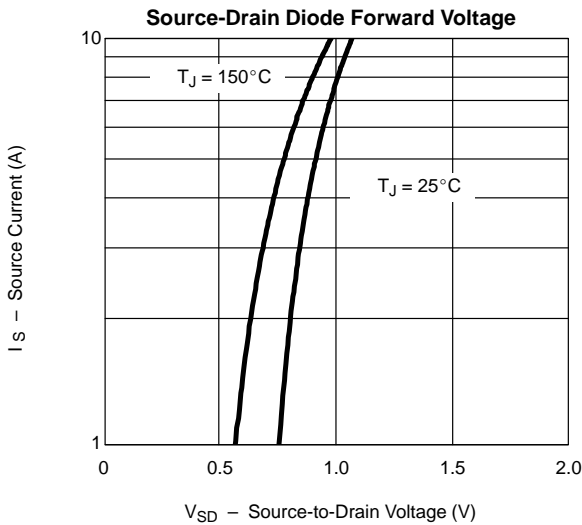


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL





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