CAT71C256L/71C256LI - Low Power
32K x 8-BIT CMOS STATIC RAM

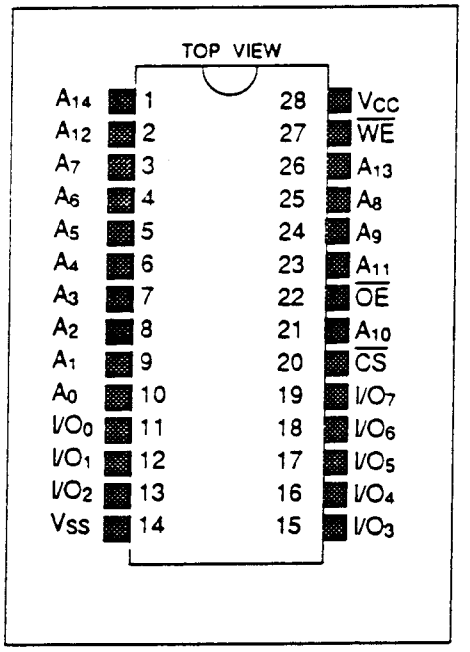
DESCRIPTION

The CAT71C256L/71C256LI is a low power, high performance 262,144 bit CMOS static RAM organized as a 32,768 X 8 bit array. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary. The CAT71C256L/71C256LI is a CMOS device requiring extremely low power during standby (100µA). The $\overline{CS}$ and $\overline{OE}$ control signals facilitate OR-tying of the output lines, simplifying memory expansion.

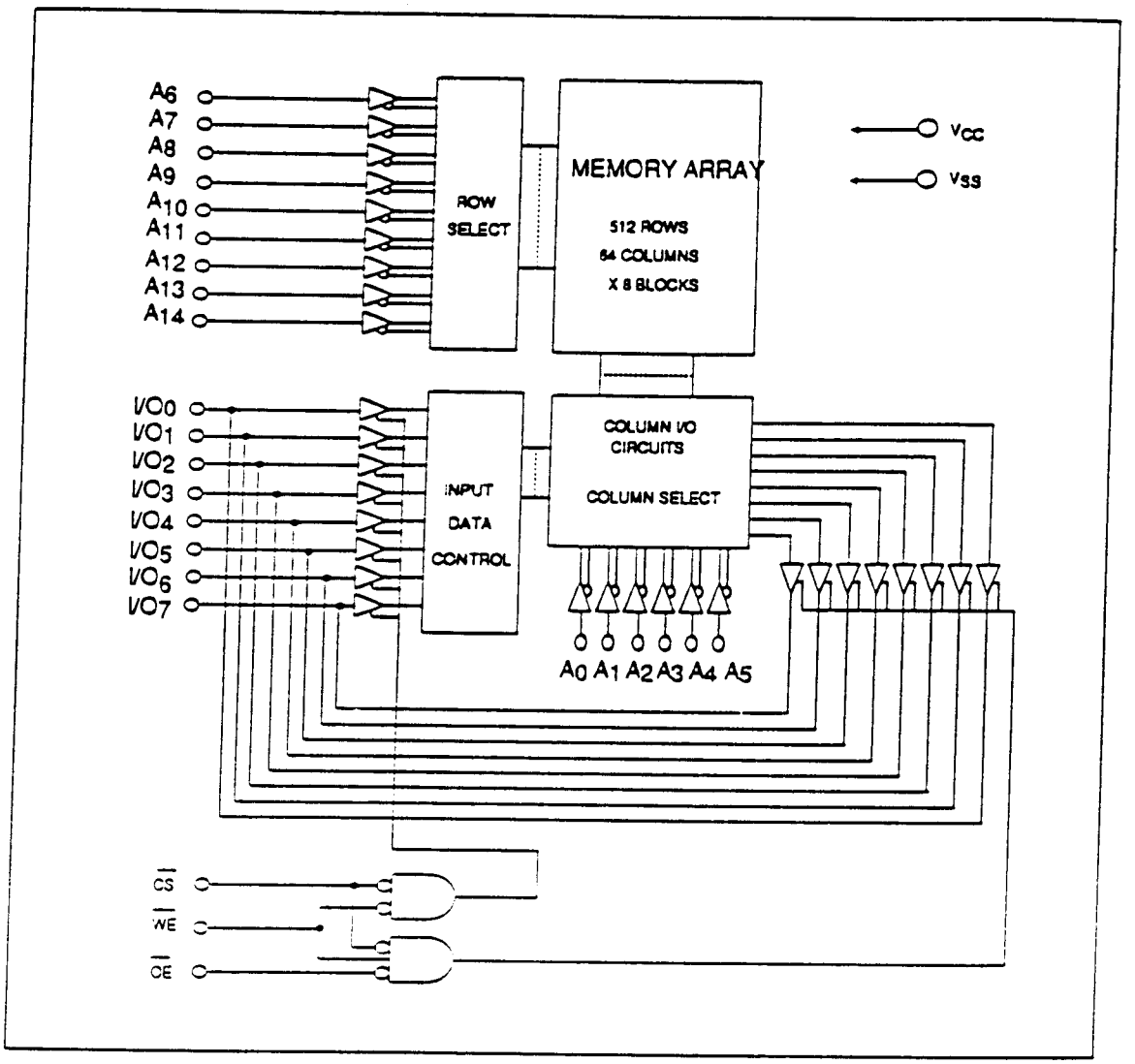
FEATURES

- Single 5V supply (±10%)
- Low power consumption:
  - Active: 80mA max
  - Standby: 100uA max
- 32,768 X 8 configuration
- Static operation
- Access / Cycle time: 85ns max
- TTL compatible INPUT/OUTPUT
- Three state outputs
- 28-pin DIP and 28-pin SO packages
- Temperature Range:
  - CAT71C256L (0° to +70°C)
  - CAT71C256LI (-40° to +85°C)

PIN CONFIGURATION
28-Pin DIP and SO



BLOCK DIAGRAM



Pin Assignment

A_0 - A_{14}	:ADDRESS INPUTS
$\overline{I/O_0}$ - I/O_7	:DATA INPUT/OUTPUT
$\overline{CS}$	:CHIP SELECT
$\overline{WE}$	:WRITE ENABLE
$\overline{OE}$	:OUTPUT ENABLE

MODES OF OPERATION

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High-Z
Read	L	H	H	High-Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

Note: X = H or L

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Conditions	Value	Unit
V_{CC}	Supply voltage	T_A = 25°C, with respect to V_{SS}	-0.3 to 7.0	V
V_{IN}	Input voltage		-0.3 to V_{CC} +0.3	V
P_D	Power dissipation	T_A = 25°C	1.0	W
T_{STG}	Storage temperature	-	-55 to +150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	V_{CC} = 5V ± 10%	4.5	5	5.5	V
V_{SS}				0		V
V_{CCH}	Data retention voltage		2	5	5.5	V
V_{IH}	"H" Input voltage	5V ± 10%	2.2	-	VCC +0.3	V
V_{IL}	"L" Input voltage		-0.3	-	0.8	V
T_{OPR}	Operating temperature	CAT71C256L	0	-	+70	°C
		CAT71C256LI	-40	-	+85	°C
CL	Output load		-	-	100	pF
TTL			-	-	1	-

DC CHARACTERISTICS

(V_{CC} = +5V ±10%), T_A (71C256L= 0°C to +70°C ,71C256LI = -40°C to 85°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{LI}	Input leakage current	V_{IN} = 0 to V_{CC}	-1		1	µA
I_{LO}	Output leakage current	$\overline{CS}$ or $\overline{OE}$ = V_{IH} VI/O = 0 to V_{CC}	-1		1	µA
V_{OH}	"H" output voltage	I_{OH} = -1mA	2.4		-	V
V_{OL}	"L" output voltage	I_{OL} = 2.1mA			0.4	V
I_{CCS}	Standby supply current (CMOS)	$\overline{CS}$ ≥V_{CC} -0.2V V_{IN} =0 to V_{CC}		0.2	100	µA
I_{CCS1}	Standby supply current (TTL)	$\overline{CS}$ = V_{IH} T_{CYC} = min. cycle			3	mA
I_{CCA}	Operating supply current	Min. cycle			80	mA

AC CHARACTERISTICS - TEST CONDITIONS

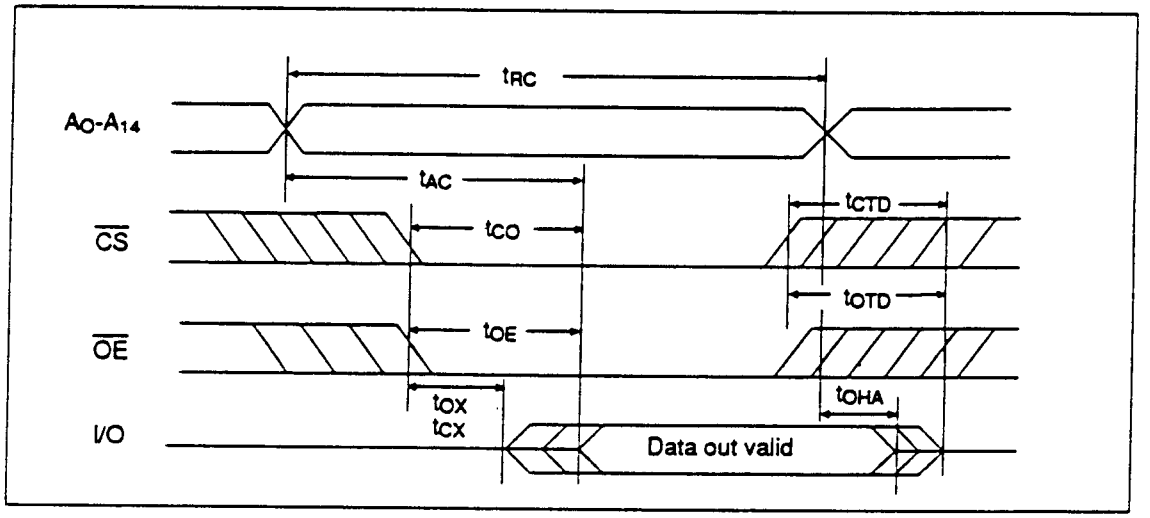
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5 ns
Input/Output Timing Reference Level	1.5V
Output Load	C_L = 100pF, 1 TTL gate

READ CYCLE

(V_{CC} = 5V ± 10%), T_A (71C256L= 0°C to +70°C, 71C256LI = -40° to +85°C)

Symbol	Parameter	71C256LPI-85 Min.	Max.	Units
t_{RC}	Read Cycle Time	85		ns
t_{AC}	Address Access Time		85	ns
t_{CO}	Chip Select Access Time		85	ns
t_{OE}	Ouput Enable to Output Valid		45	ns
t_{CX}	Chip Selection to Output Active	10		ns
t_{OHA}	Output Hold Time from Address Change	5		ns
t_{OTD}	Output 3-state from Output Disable	0	30	ns
t_{CTD}	Output 3-state from Chip Deselection		30	ns
t_{OX}	Output Enable to Output Active	5		ns

READ CYCLE TIMING



NOTES:

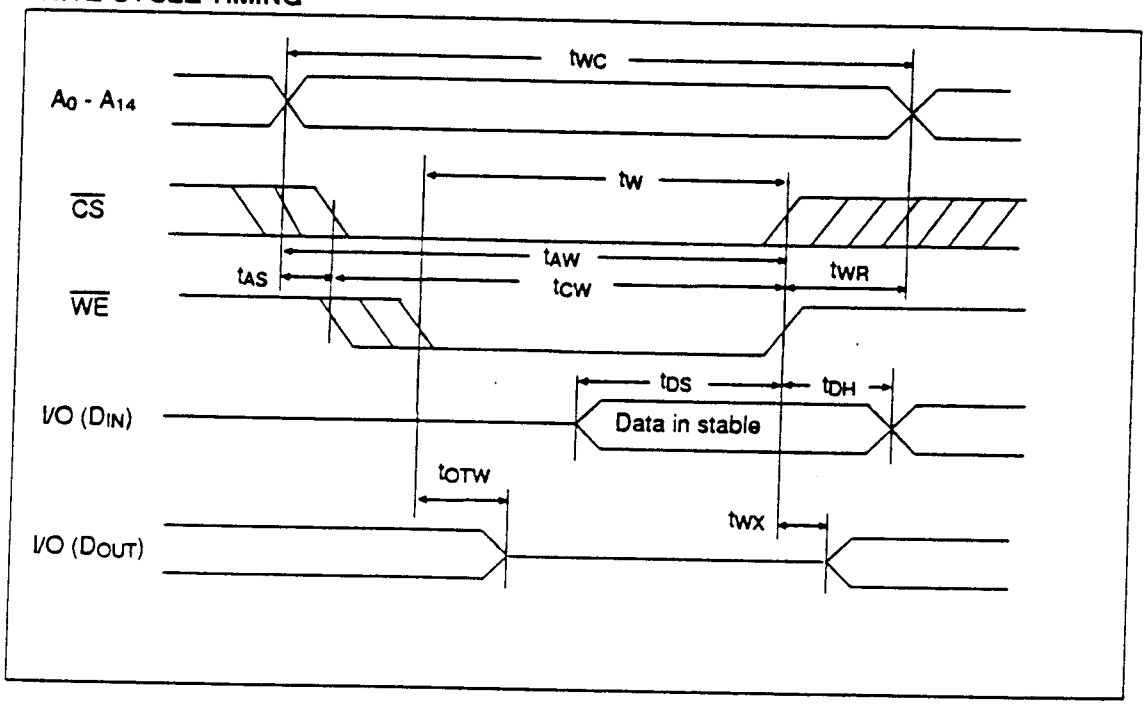
1. A READ occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time to DATA OUT high impedance.

WRITE CYCLE

(V_{CC} = 5V ± 10%), TA (71C256L =0° C to +70°C, 71C256LI = -40°C to +85°C)

Symbol	Parameter	71C256L/LI-85 Min.	Max.	Units
t_{WC}	Write Cycle Time	85		ns
t_{CW}	Chip Selection to End of Write	75		ns
t_{AW}	Address Valid to End of Write	75		ns
t_{AS}	Address to Write Set-up Time	0		ns
t_W	Write Time	70		ns
t_{WR}	Write Recovery Time	5		ns
t_{DS}	Data Set-up Time	40		ns
t_{DH}	Data Hold from Write Time	0		ns
t_{OTW}	Output 3-state from Write	0	30	ns
t_{WX}	Output Active from End of Write	5		ns

WRITE CYCLE TIMING



NOTES:

1. Write condition: during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ can be both high and low during a Write cycle.
3. t_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
4. t_W is the overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time to DATA OUT high impedance, not by output level.
7. When I/O pins are in data output mode, do not force inverse input signals to those pins.

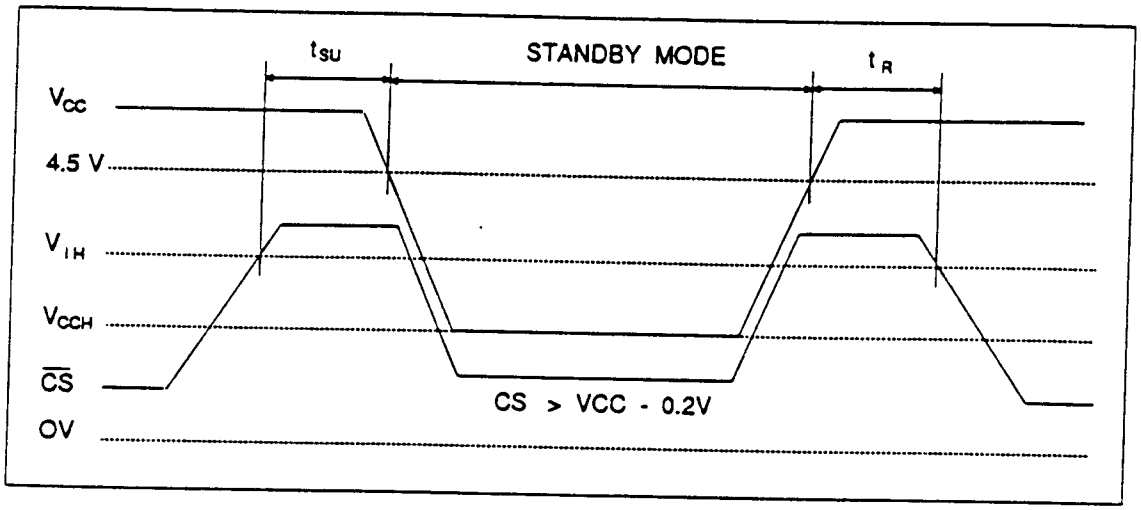
CAPACITANCE

(T_A = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	10	pF

Note: These parameters are periodically sampled and are not 100% tested.

$\overline{CS}$ CONTROL TIMING



LOW Vcc DATA RETENTION CHARACTERISTICS

T_A = -40°C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CCH}	Vcc for data retention	$\overline{CS} \geq V_{CC}$ -0.2V	2			V
I_{CCH}	Data retention current	$\overline{CS} \geq V_{CC}$ -0.2V, Vcc = 3V		1	50	µA
t_{SU}	$\overline{CS}$ to Data retention time		0			ns
t_R	Operation recovery time		t_{RC}			ns