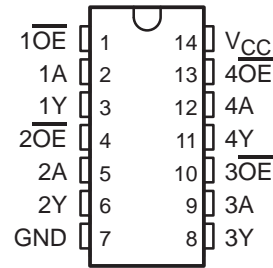


SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

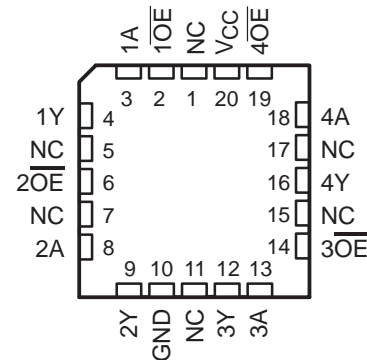
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVTH125 . . . J PACKAGE
SN74LVTH125 . . . D, DB, DGV, OR PW PACKAGE
(TOP VIEW)



SN54LVTH125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH125 devices feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (\overline{OE}) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH125 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH125 is characterized for operation from -40°C to 85°C .



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 **TEXAS
INSTRUMENTS**

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SN54LVTH125, SN74LVTH125

3.3-V ABT QUADRUPLE BUS BUFFERS

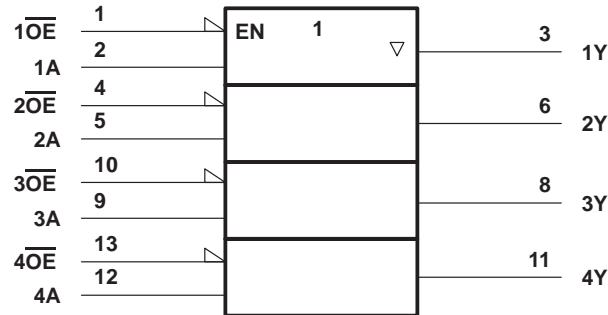
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

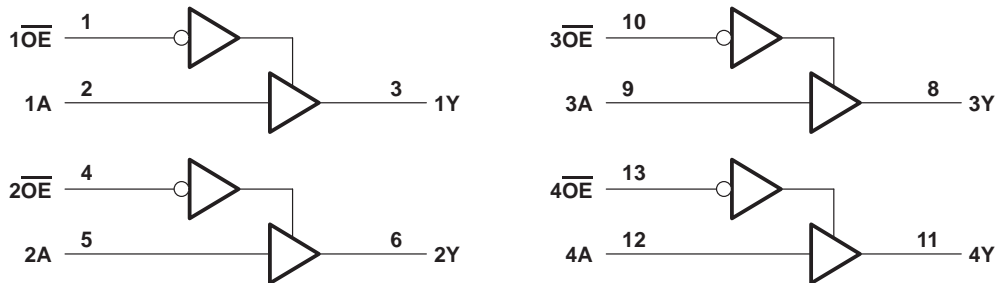
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, and PW packages.

SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS703F – AUGUST 1997 – REVISED JUNE 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH125	96 mA
SN74LVTH125	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH125	48 mA
SN74LVTH125	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
DB package	96°C/W
DGV package	127°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH125		SN74LVTH125		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVTH125, SN74LVTH125

3.3-V ABT QUADRUPLE BUS BUFFERS

WITH 3-STATE OUTPUTS

SCBS703F – AUGUST 1997 – REVISED JUNE 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH125			SN74LVTH125			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 2.7 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2			V _{CC} -0.2			V
	V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4			2.4			
	V _{CC} = 3 V		2			2			
V _{OL}	V _{CC} = 2.7 V		0.2			0.2			V
			0.5			0.5			
	V _{CC} = 3 V		0.4			0.4			
			0.5			0.5			
			0.55			0.55			
			0.55			0.55			
I _I	V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10			10			μA
	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND	±1			±1			
	Data inputs	V _{CC} = 3.6 V	1			1			
		V _I = 0	-5			-5			
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA
I _I (hold)	Data inputs	V _{CC} = 3 V	75			75			μA
			-75			-75			
		V _{CC} = 3.6 V‡, V _I = 0 to 3.6 V				±500			
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V		5			5			μA
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V		-5			-5			μA
I _{OZPU}	V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±50*			±50			μA
I _{OZPD}	V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±50*			±50			μA
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.12 0.19		0.12 0.19		mA
			Outputs low		4.5 7		4.5 7		
			Outputs disabled		0.12 0.19		0.12 0.19		
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.3			0.2			mA
C _i	V _I = 3 V or 0		4			4			pF
C _o	V _O = 3 V or 0		6.5			6.5			pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVTH125, SN74LVTH125
3.3-V ABT QUADRUPLE BUS BUFFERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH125				SN74LVTH125				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t_{PLH}	A	Y	1	4.2		4.7	1	2	3.5		4.5	ns
t_{PHL}			1	4.1		5.1	1	2.1	3.9		4.9	
t_{PZH}	\overline{OE}	Y	1	4.9		5.6	1	2	4		5.5	ns
t_{PZL}			1.1	4.9		5.6	1.1	2.1	4		5.4	
t_{PHZ}	\overline{OE}	Y	1.5	5.3		5.9	1.5	2.3	4.5		5.7	ns
t_{PLZ}			1.3	4.7		4.2	1.3	2.8	4.5		4	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

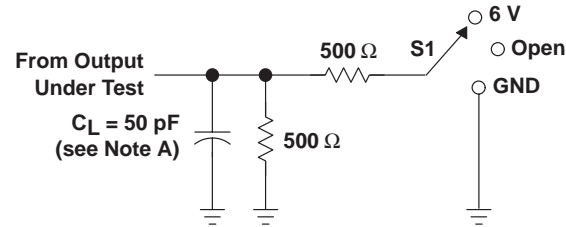
SN54LVTH125, SN74LVTH125

3.3-V ABT QUADRUPLE BUS BUFFERS

WITH 3-STATE OUTPUTS

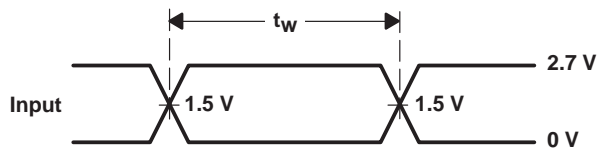
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PARAMETER MEASUREMENT INFORMATION

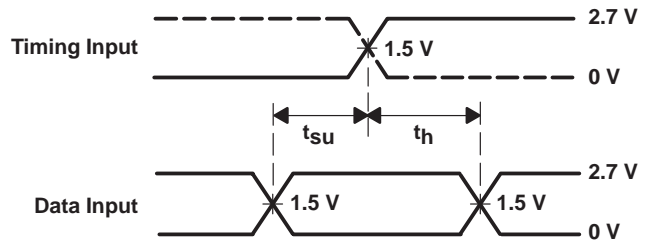


LOAD CIRCUIT

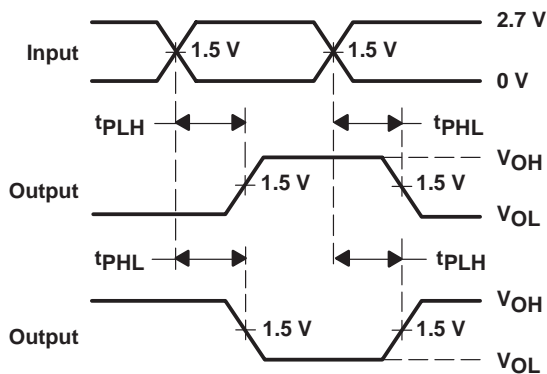
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



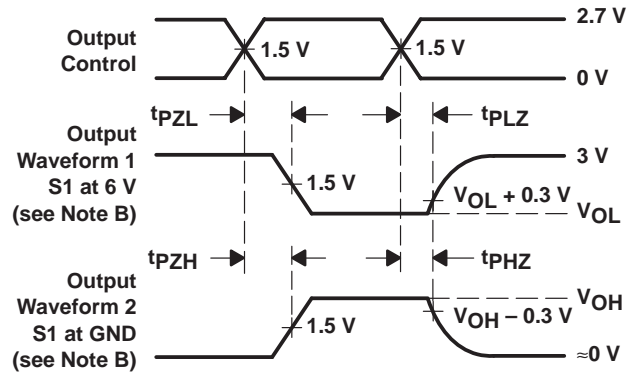
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PRODUCT SUPPORT: [TRAINING](#)

SN74LVTH125, 3.3-V ABT Quadruple Bus Buffers With 3-State Outputs

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN74LVTH125
Voltage Nodes (V)	3.3, 2.7
Vcc range (V)	2.7 to 3.6
Input Level	TTL
Output Level	CMOS
Output Drive (mA)	-32/+64
No. of Gates	4

FEATURES

[Back to Top](#)

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
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- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

DESCRIPTION

[Back to Top](#)

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The LVTH125 devices feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable ($OE\backslash$) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $OE\backslash$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH125 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH125 is characterized for operation from -40°C to 85°C .

TECHNICAL DOCUMENTS

[Back to Top](#)

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[Back to Top](#)

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- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Implications of Slow or Floating CMOS Inputs](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVT Family Characteristics](#) (SCEA002A - Updated: 03/01/1998)
- [LVT-to-LVTH Conversion](#) (SCEA010 - Updated: 12/08/1998)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Low Voltage Logic Families](#) (SCVAE01A - Updated: 06/01/1998)
- [Mixed 3.3-V And 5-V Systems With LVT Logic](#) (SCBA005 - Updated: 04/01/1993)
- [Timing Differences of 10-pF Versus 50pF Loading](#) (SCEA004 - Updated: 11/01/1996)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)

RELATED DOCUMENTS

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- [Advanced Bus Interface Logic Selection Guide](#) (SCYT126, 448 KB - Updated: 01/09/2001)
- [Documentation Rules \(SAP\) And Ordering Information](#) (SZZU001B, 13 KB - Updated: 05/06/1999)
- [Logic Selection Guide First Half 2001](#) (SDYU0010, 4573 KB - Updated: 11/08/2000)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [More Power In Less Space - Technical Article](#) (SCAU001A, 850 KB - Updated: 03/01/1996)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)

SAMPLES

[Back to Top](#)

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	SAMPLES
SN74LVTH125D	D	14	-40 TO 85	ACTIVE	Request Samples
SN74LVTH125DBR	DB	14	-40 TO 85	ACTIVE	Request Samples
SN74LVTH125DGVR	DGV	14	-40 TO 85	ACTIVE	Request Samples
SN74LVTH125DR	D	14	-40 TO 85	ACTIVE	Request Samples
SN74LVTH125PWR	PW	14	-40 TO 85	ACTIVE	Request Samples

PRICING/AVAILABILITY

[Back to Top](#)

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	BUDGETARY PRICE US\$/UNIT QTY= 1000+	PACK QTY	PRICING/AVAILABILITY
SN74LVTH125D	D	14	-40 TO 85	ACTIVE	0.67	50	Check stock or order
SN74LVTH125DBR	DB	14	-40 TO 85	ACTIVE	0.67	2000	Check stock or order
SN74LVTH125DGVR	DGV	14	-40 TO 85	ACTIVE	0.75	2000	Check stock or order
SN74LVTH125DR	D	14	-40 TO 85	ACTIVE	0.67	2500	Check stock or order
SN74LVTH125PWR	PW	14	-40 TO 85	ACTIVE	0.67	2000	Check stock or order

MODELS

[Back to Top](#)

- [IBIS Model of SN74LVTH125](#) (SCEM176, 16 KB, ZIP - Updated: 02/06/2001)

Table Data Updated on: 7/22/2001