T-58-11-31

May 1990
PRELIMINARY

Micro Linear

ML4810, ML4811

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML4810 and ML4811 High Frequency PWM Controllers are optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. The ML4810/11 contain a unique overload protection circuit which helps to limit stress on the output devices and reliably performs a soft-start reset. Propagation delays are minimal through the comparators and logic for reliable high frequency operation and slew rate and bandwidth are maximized on the error amplifier. These controllers are designed to work in either voltage or current mode and provide for input voltage feed forward.

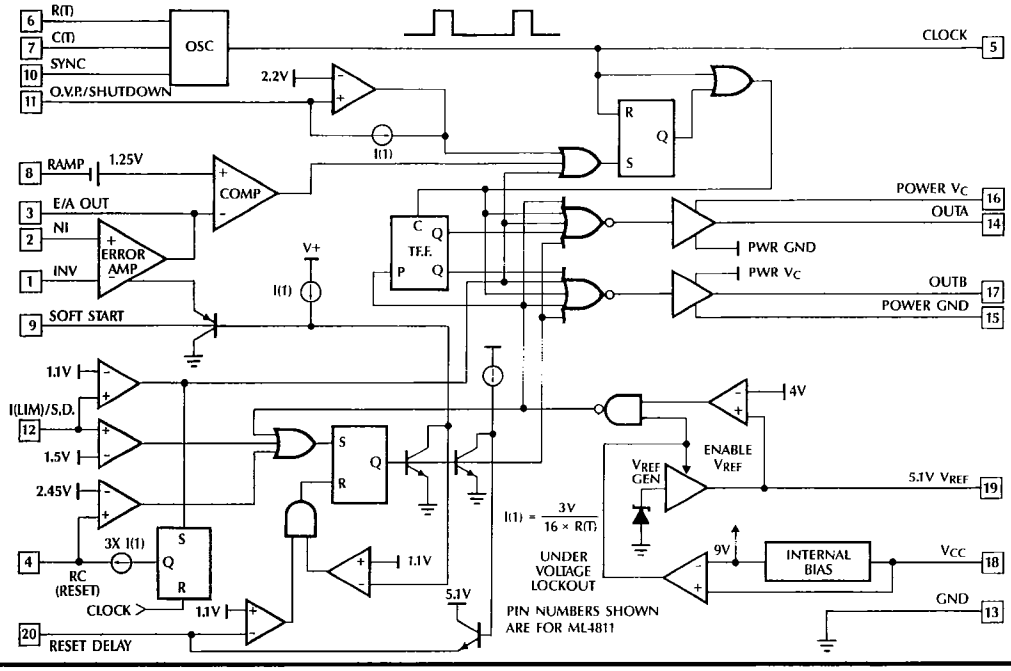
A 1.1V threshold current limit comparator provides a cycle-by-cycle current limit. An integrating circuit "counts" the number of times the 1.1V limit was reached. A soft-start cycle is initiated if the cycle-by-cycle current limit is repeatedly activated. A reset delay function is provided on the ML4811. All logic is fully latched to provide jitter-free operation and prevent multiple pulsing. An under-voltage lockout circuit with 7V of hysteresis assures low startup current and drives the outputs low during fault condition.

The ML4810/11 are fabricated on a 40V bipolar process from the FB3480 Power Supply Controller Array. Customized versions of this controller can therefore be easily implemented. Please refer to the FB3480 datasheet for more information. These controllers are similar to the UC1825 controller, however these controllers include many features not found on the 1825. These features are set in *Italics*.

FEATURES

- *Integrating Soft Start Reset*
- High Current (2A peak) Dual Totem Pole Outputs
- Practical Operation to 1MHz (f_{OSC})
- 5.1V, ±1% Trimmed Bandgap Reference
- *Under Voltage Lockout with 7V Hysteresis*
- *Soft Start Reset Delay* (ML4811)
- *Oscillator Synchronization Function* (ML4811)
- *Soft Start latch ensures full soft start cycle*
- *Outputs pull low for undervoltage lockout*
- *Accurately controlled Oscillator ramp discharge current*
- *All timing currents "slaved" to R(T) for precise control*

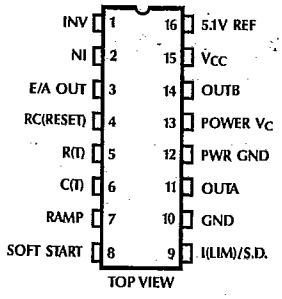
ML4811 BLOCK DIAGRAM



PIN CONNECTIONS

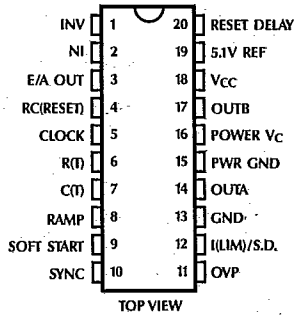
T-58-11-31

ML4810
16-Pin DIP



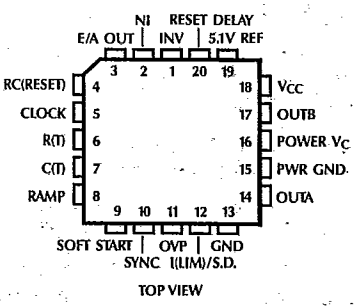
TOP VIEW

ML4811
20-Pin DIP



TOP VIEW

ML4811
20-Pin PCC



TOP VIEW

PIN DESCRIPTION (Pin numbers shown for ML4811)

PIN NO.	NAME	FUNCTION
1	INV	Inverting input to error amp
2	NI	Non-inverting input to error amp
3	E/A Out	Output of error amplifier and input to main comparator
4	RC(RESET)	Timing elements for Integrating Soft Start reset
5	CLOCK	Oscillator output.
6	R(T)	Timing Resistor for Oscillator — sets charging current for oscillator timing capacitor (Pin 6)
7	C(T)	Timing Capacitor for Oscillator
8	RAMP	Non-Inverting input to main comparator. Connected to C(T) for Voltage Mode operation or to current sense resistor for current mode
9	SOFT START	Normally connected to Soft Start Capacitor
10	SYNC	A high going pulse terminates the PWM cycle and discharges C(T)
11	OVP	Exceeding 2.5V terminates the PWM cycle and inhibits the outputs
12	I(LIM)/S.D.	Current limit sense pin. Normally connected to current sense resistor
13	GND	Analog Signal Ground
14	OUTA	High Current Totem pole output. This output is the first one energized after Power On Reset
15	PWR GND	Return for the High Current Totem pole outputs
16	V_C	Positive Supply for the High Current Totem pole outputs
17	OUTB	High Current Totem pole output
18	V_{CC}	Positive Supply for the IC
19	5.1V REF	Buffered output for the 5.1V voltage reference
20	RESET DELAY	Timing Capacitor to determine the amount of delay between fault

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 18, 16) 30V
Output Current, Source or Sink (Pins 14, 17)
DC 0.5A
Pulse (0.5μS) 2.0A
Analog Inputs
(Pins 1, 2, 8) ..... -0.3V to 7V
(Pins 9, 10, 11, 12, 20) ..... -0.3V to 6V
Clock Output Current (Pin 5) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Junction Temperature
ML4811M ..... 150°C
ML4811I, ML4810C, ML4811C ..... 125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 65°C/W
Ceramic DIP ..... 65°C/W
Plastic Chip Carrier (PCC) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range
ML4811M ..... -55°C to +125°C
ML4811I ..... -40°C to +85°C
ML4810C, ML4811C ..... 0°C to +70°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. Pin numbers given for ML4811.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Initial Accuracy		T_J = 25°C (note 1)	360	400	440	KHz
Voltage Stability		10V < V_{CC} < 30V, (note 1)		0.2	2	%
Temperature Stability		(note 1)			5	%
Total Variation		line, temp. (note 1)	340		460	KHz
Clock Out High			3.9	4.5		V
Clock Out Low				2.3	2.9	V
Ramp Peak		(note 1)	2.6	2.8	3.0	V
Ramp Valley		(note 1)	0.7	1.0	1.25	V
Ramp Valley to Peak		(note 1)	1.6	1.8	2.0	V
Sync Input Threshold			0.8	1.0	1.2	V
Sync Input Current		$V_{PIN\ 10}$ = 4V				μA
Reference Section						
Output Voltage	ML4810/11C	T_J = 25°C, I_O = 1mA	5.00	5.10	5.2	V
	ML4811M, ML4811I		5.05	5.10	5.15	V
Line Regulation		10V < V_{CC} < 30V		2	20	mV
Load Regulation		1mA < I_O < 10mA		5	20	mV
Temperature Stability		-55°C < T_J < 150°C, (note 1)		.2	.4	%
Total Variation	ML4810/11C	line, load, temp. (note 1)	4.95		5.25	V
	ML4811M, ML4811I		5.0		5.20	V
Output Noise Voltage		10Hz to 10KHz		50		μV
Long Term Stability		T_J = 125°C, 1000 Hrs (note 1)		5	25	mV
Short Circuit Current		V_{REF} = 0V	-15	-50	-100	mA
Under-Voltage Lockout Section						
Start Threshold			15	16	17	V
UVLO Hysteresis			6.5	7	7.5	V
Supply Current						
Start Up Current		V_{CC} = 8V		2	3	mA
I_{CC}		$V_{PIN\ 1,\ 7,\ 9}$ = 0V, $V_{PIN\ 2}$ = 1V, T_A = 25°C		32	42	mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, R_T = 3.65KΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section						
Input Offset Voltage	ML4810/11C				15	mV
	ML4811M, ML4811I				10	mV
Input Bias Current				.6	3	µA
Input Offset Current				.1	1	µA
Open Loop Gain		$1 < V_O < 4V$	60	96		dB
CMRR		$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR		$10 < V_{CC} < 30V$	75	90		dB
Output Sink Current		$V_{PIN\ 3}$ = 1V	1	2.5		mA
Output Source Current		$V_{PIN\ 3}$ = 4V	-.5	-1.3		mA
Output High Voltage		$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	V
Output Low Voltage		$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	V
Unity Gain Bandwidth		(note 1)	3	5.5		MHz
Slew Rate		(note 1)	6	12		V/µs
PWM Comparator Section						
Pin 8 Bias Current		$V_{PIN\ 8}$ = 0V		-1	-5	µA
Duty Cycle Range			0		75	%
Pin 3 Zero DC Threshold			1.1	1.25		V
Delay to Output		(note 1)		50	80	ns
Soft-Start Section						
Charge Current (Pin 9)		$V_{PIN\ 9}$ = 1V, $V_{PIN\ 12}$ = 0, $V_{PIN\ 4}$ = 0	40	50	60	µA
Discharge Current (Pin 9)		$V_{PIN\ 9}$ = 3V, $V_{PIN\ 4} > 2.5$	1	5		mA
		$V_{PIN\ 9}$ = 3V, $V_{PIN\ 12} > 1.65$, $V_{PIN\ 4} < 2$	1	5		mA
Charge Current (Pin 20)		$V_{PIN\ 20}$ = 1V	1	5		mA
Discharge Current (Pin 20)		Requires external discharge resistor		0		µA
Current Limit/Shutdown Section						
Pin 12 Bias Current	ML4810/11C	$0V < V_{PIN\ 12} < 4V$			+15	µA
	ML4811M, ML4811I	$0V < V_{PIN\ 12} < 4V$			+10	µA
Current Limit Threshold			1.0	1.1	1.2	V
Reset Threshold (Pin 12)		$V_{PIN\ 4} < 2V$	1.35	1.50	1.65	V
Delay to Output		(note 1)		40	70	ns
Pin 4 Charging Current		$V_{PIN\ 12}$ = 2V	120	150	180	µA
Restart Threshold (Pin 4)			2	2.45	3	V
OVP Shutdown Threshold (Pin 11)			1.8	2.2	2.6	V
OVP Input Current		$V_{PIN\ 11}$ = 3V	40	50	60	µA
Output Section						
Output Low Level		I_{OUT} = 20mA		.25	.4	V
		I_{OUT} = 200mA		1.2	2.2	V
Output High Level		I_{OUT} = -20mA	13.0	13.5		V
		I_{OUT} = -200mA	12.0	13.0		V
Collector Leakage		V_C = 30V		100	500	µA
Rise/Fall Time		C_L = 1000pF, (note 1)		30	80	ns

Note 1: This parameter not 100% tested in production but guaranteed by design.

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FUNCTIONAL DESCRIPTION

SOFT START AND CURRENT LIMIT — INTEGRATING SOFT START RESET

The ML4810/11 offers a unique system of fault detection and reset. Most PWM controllers use a two threshold method which relies on the buildup of current in the output inductor during a fault. This buildup occurs because:

1. Inductor di/dt is a small number when the switch is off under load fault (short circuit) conditions, since V_L is small.
2. Some energy is delivered to the inductor since the IC must first detect the over-current because there is a finite delay before the output switch can turn off.

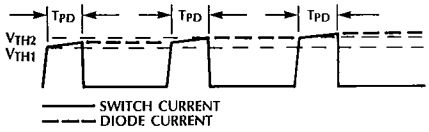

Figure 1. Current Waveforms for Slow Turn-Off System with Load Fault

This scheme was adequate for controllers with longer comparator propagation delays and turn-off delays than is desirable in a high frequency system. For systems with low propagation delays, very little energy will be delivered to the inductor and the current "ratcheting" described above will not occur. This results in the controller never detecting the load fault and continuing to pump full current to the load indefinitely, causing heating in the output rectifiers and inductor.

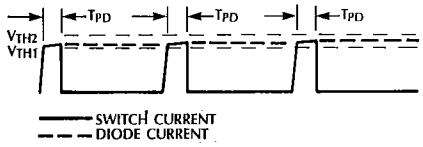

Figure 2. Current Waveforms for High Speed System with Load Fault

A method of circumventing this problem involves "counting" the number of times the controller terminates the PWM cycle due to the cycle by cycle current limit.

When the switch current crosses the 1.1V threshold A1 signals the F1 to terminate the cycle and sets F3, which is reset at the beginning of the PWM cycle. The output of F3 turns on a current source to charge C2. When, after several cycles, C2 has charged to 2.45V, A5 turns on F2 to discharge soft start capacitor C1. Charge is continually bled from C2 by R1. If a current surge is short lived (for instance a disk drive start-up or a board being plugged into a live rack) the control can "ride

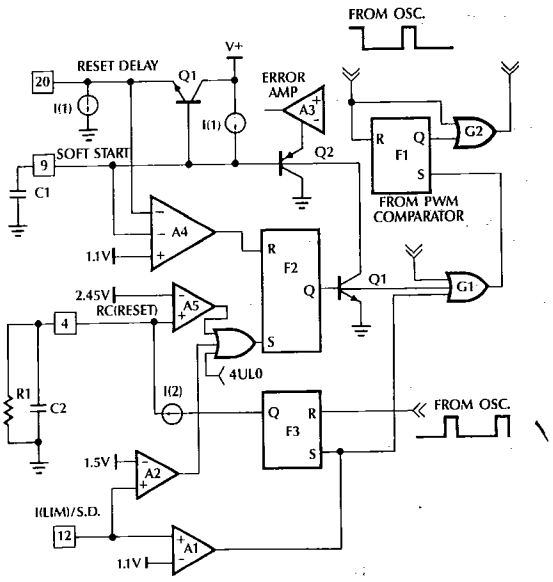

Figure 3. Integrating Soft Start Reset

out" the surge with the switch protected by the cycle by cycle limit. R1 and C1 can be selected to track diode heating, or to ride out various system surge requirements as required.

If the high current demanded is caused by a short circuit, the duty cycle will be short and the output diodes will carry the current for the majority of the PWM cycle. C2 charges fastest for low duty cycles (since F3 will be on for a longer time) providing for quicker shutdown during short-circuit when the output diodes are being maximally stressed.

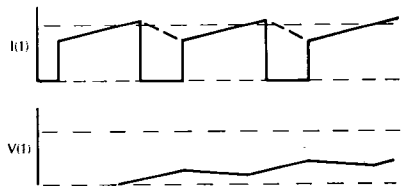

Figure 4. Switching Current and Pin 4 Voltage — Normal

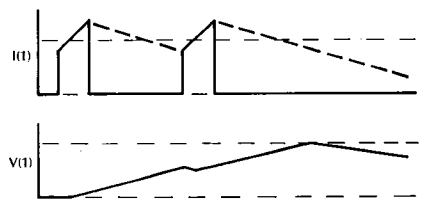

Figure 5. Switching Current and Pin 4 Voltage — Load Fault

OSCILLATOR

The ML4811 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_T$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse. A discharge of the oscillator can be initiated by applying a high level to the Sync pin. A short pulse of a frequency higher than the oscillator's free running frequency can be used to synchronize the ML4811 to an external clock. The pulse can be equal to the desired deadtime (T_D) or the deadtime can be determined by I_{DIS} and C_T, whichever is greater.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: $T_{RAMP} = C$ (Ramp Valley to Peak)/I_{SET}
and: $T_{DEADTIME} = C$ (Ramp Valley to Peak)/I_{Q1}

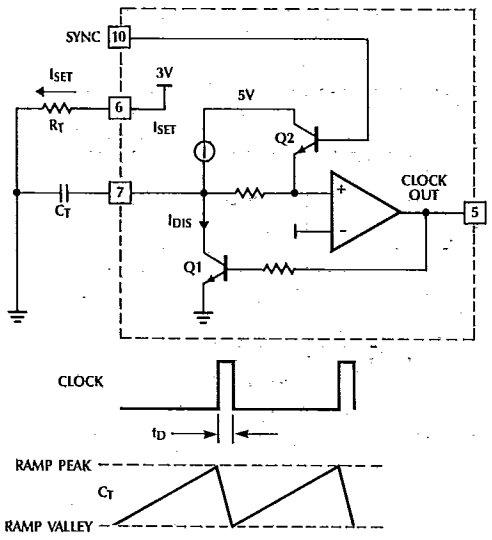

Figure 6. Simplified Oscillator Block Diagram and Timing

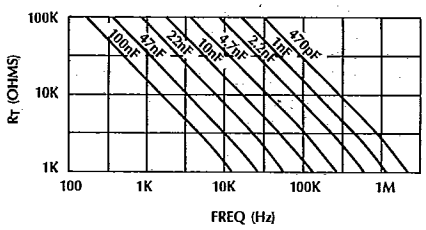

Figure 7. Oscillator Timing Resistance vs. Frequency

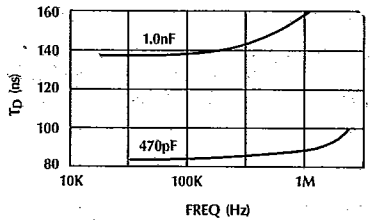

Figure 8. Oscillator Deadtime vs Frequency

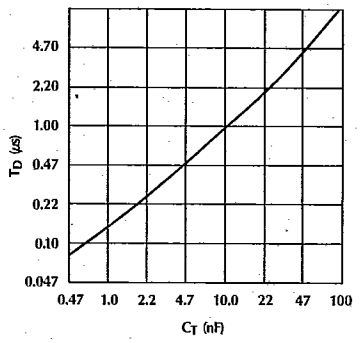

Figure 9. Oscillator Deadtime vs C(T) ($3 \leq R(T) \leq 100K\Omega$)

ERROR AMPLIFIER

The ML4811 error amplifier is a 5.5MHz bandwidth 12V/µsec slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

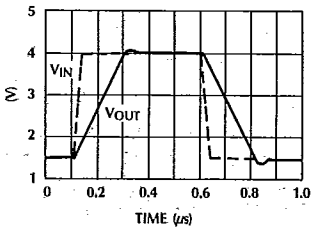

Figure 10. Unity Gain Slew Rate

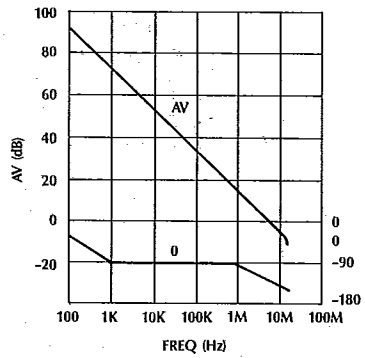

Figure 11. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML4811 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

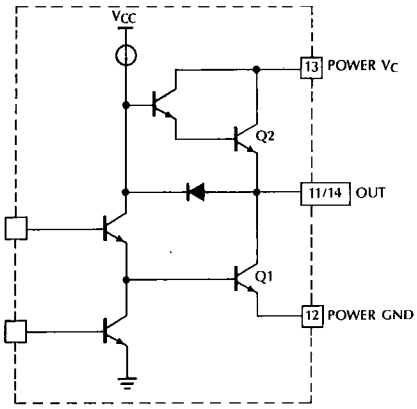

Figure 12. Simplified Schematic

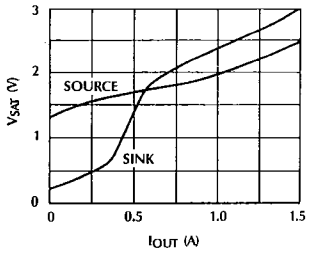

Figure 13. Saturation Curves

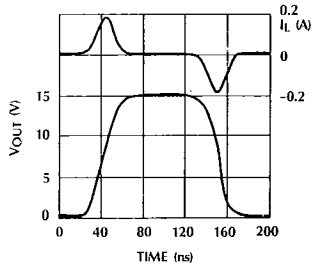

Figure 14. Rise/Fall Time (C_L = 1000pF)

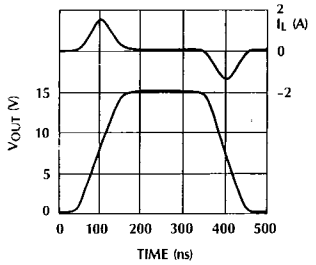

Figure 15. Rise/Fall Time (C_L = 10,000pF)

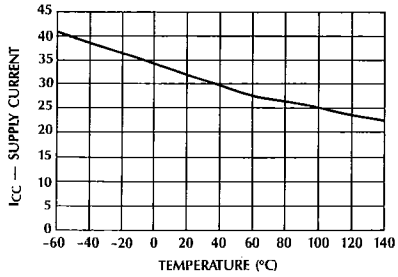

Figure 16. Suppy Current vs. Temperature

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4810CP	0°C to +70°C	16-Pin MOLDED DIP
ML4811CP	0°C to +70°C	20-Pin MOLDED DIP
ML4811CQ	0°C to +70°C	20-Pin MOLDED PCC
ML4811IP	–40°C to +85°C	20-Pin MOLDED DIP
ML4811IQ	–40°C to +85°C	20-Pin MOLDED PCC
ML4811MJ	–55°C to +125°C	20-Pin HERMETIC DIP