DATASHEET

Description

The 9FGL0241/51/P1 are members of IDT's 3.3V Low-Power (LP) PCIe family. The devices have 2 output enables for clock management and support 2 different spread spectrum levels in addition to spread off. The 9FGL0241/51/P1 supports both Common Clock (CC) with or without spread spectrum and Separate Reference no-Spread (SRnS) PCIe clocking architectures. The 9FGL02P1 can be programmed with a user-defined power up default SMBus configuration.

Recommended Application

3.3V PCIe Gen1-2-3 Clock Generator

Output Features

- 2 – 100 MHz Low-Power HCSL (LP-HCSL) DIF pairs
  - 9FGL0241 default ZOUT = 100Ω
  - 9FGL0251 default ZOUT = 85Ω
  - 9FGL02P1 factory programmable defaults
- 1 - 3.3V LVCMOS REF output w/Wake-On-LAN (WOL) support

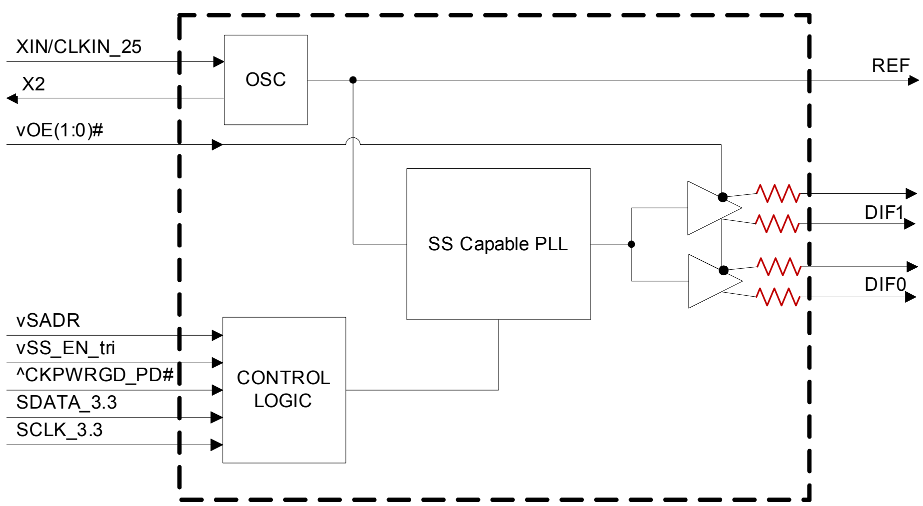
Key Specifications

- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew <50ps
- DIF phase jitter is PCIe Gen1-2-3 compliant with SSC on or off
- DIF 12k-20M phase jitter is <3ps rms when SSC is off
- REF phase jitter is <300fs rms (SSC off) and < 1ps RMS (SSC on)
- ±100ppm frequency accuracy on all clocks

Features/Benefits

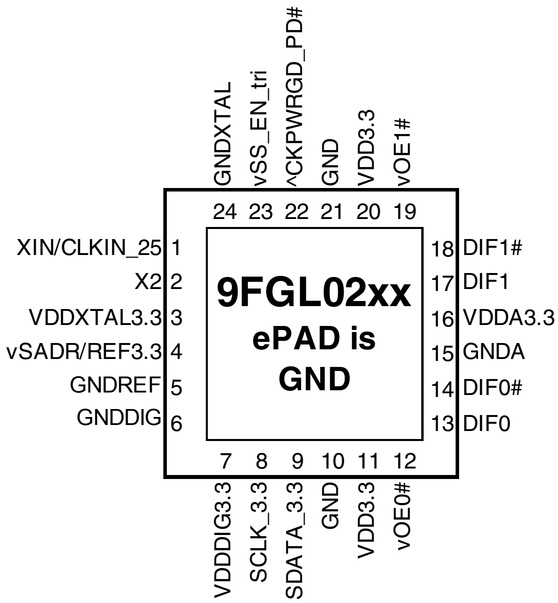
- Direct connection to 100Ω (xx41) or 85Ω (xx51) transmission lines; saves 8 resistors compared to standard PCIe devices
- 112mW typical power consumption; eliminates thermal concerns
- SMBus-selectable features allows optimization to customer requirements:
  - control input polarity
  - control input pull up/downs
  - slew rate for each output
  - 33, 85 or 100Ω output impedance for each output
  - spread spectrum amount
- 41 and 51 devices contain default configuration; SMBus interface not required for device operation
- P1 device allows factory programming of customer-defined SMBus power up default; allows exact optimization to customer requirements
- OE# pins; support DIF power management
- 8MHz – 40MHz input frequency (25MHz default); flexibility
- Pin/SMBus selectable 0%, -0.25% or -0.5% spread on DIF outputs %; minimize EMI and phase jitter for each application
- DIF outputs blocked until PLL is locked; clean system start-up
- Two selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 24-pin 4x4mm VFQFPN; minimal board space

Block Diagram



Note: Resistors default to internal on 41/51 devices. P1 devices have programmable default impedances on an output-by-output basis.

Pin Configuration



24-pin VFQFPN, 4x4 mm, 0.5mm pitch

^ prefix indicates internal 120KOhm pull up resistor

v prefix indicates internal 120KOhm pull down resistor

SMBus Address Selection Table

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	x
	1	1101010	x

Power Management Table

CKPWRGD_PD#	SMBus OE bit	DIFx/DIFx#		REF
		True O/P	Comp. O/P	
0	X	Low[1]	Low[1]	Hi-Z[2]
1	1	Running	Running	Running
1	1	Disabled[1]	Disabled[1]	Running
1	0	Disabled[1]	Disabled[1]	Disabled[4]

1. The output state is set by B11[1:0] (Low/Low default)
2. REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is disabled unless Byte3[5]=1, in which case REF is running..
3. Input polarities defined at default values for 9FGLxx41/xx51.
4. See SMBus description for Byte 3, bit 4

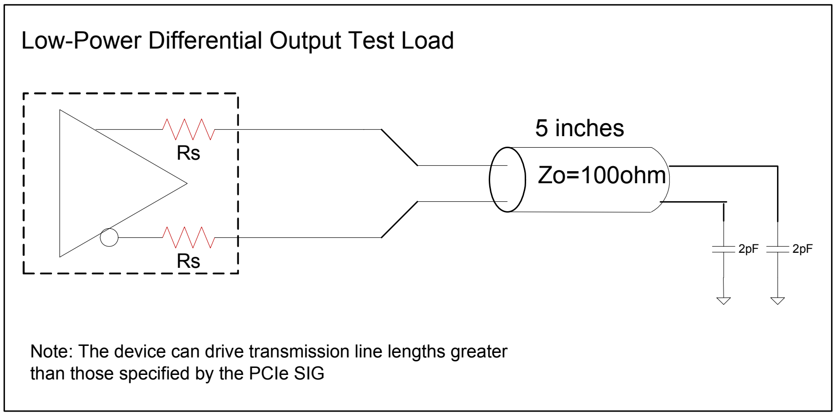
Power Connections

Pin Number		Description
VDD	GND	
3	5,24	XTAL, REF
7	6	Digital Power
11,20	10,21,25	DIF outputs
16	15	PLL Analog

Pin Descriptions

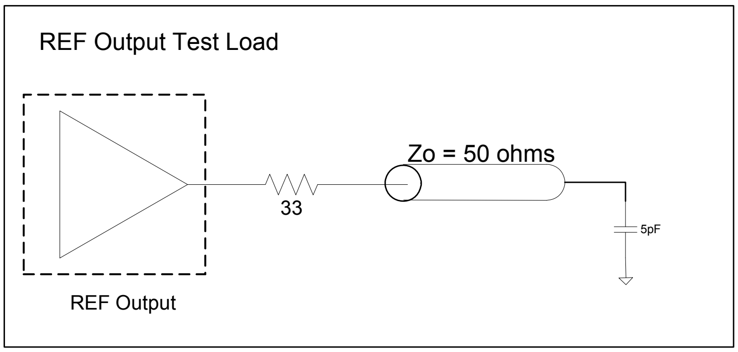
Pin#	Pin Name	Type	Pin Description
1	XIN/CLKIN_25	IN	Crystal input or Reference Clock input. Nominally 25MHz.
2	X2	OUT	Crystal output.
3	VDDXTAL3.3	PWR	Power supply for XTAL, nominal 3.3V
4	vSADR/REF3.3	LATCHED I/O	Latch to select SMBus Address/3.3V LVCMOS copy of X1/REFIN pin
5	GNDREF	GND	Ground pin for the REF outputs.
6	GNDDIG	GND	Ground pin for digital circuitry
7	VDDDIG3.3	PWR	3.3V digital power (dirty power)
8	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
9	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
10	GND	GND	Ground pin.
11	VDD3.3	PWR	Power supply, nominal 3.3V
12	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	DIF0	OUT	Differential true clock output
14	DIF0#	OUT	Differential Complementary clock output
15	GNDA	GND	Ground pin for the PLL core.
16	VDDA3.3	PWR	3.3V power for the PLL core.
17	DIF1	OUT	Differential true clock output
18	DIF1#	OUT	Differential Complementary clock output
19	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
20	VDD3.3	PWR	Power supply, nominal 3.3V
21	GND	GND	Ground pin.
22	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
23	vSS_EN_tri	LATCHED IN	Latched select input to select spread spectrum amount at initial power up : 1 = -0.5% spread, M = -0.25%, 0 = Spread Off
24	GNDXTAL	GND	GND for XTAL
25	ePAD	GND	Connect to ground

Test Loads



Terminations

Device	Zo (Ω)	Rs (Ω)
9FGL0241	100	None needed
9FGL0251	100	7.5
9FGL02P1	100	Prog.
9FGL0241	85	N/A
9FGL0251	85	None needed
9FGL02P1	85	Prog.



Alternate Terminations

The 9FGL family can easily drive LVPECL, LVDS, and CML logic. See “AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs” for details.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9FGL02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDxxx	Applies to VDD pins.	-0.5		3.9	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.5V.

Electrical Characteristics–SMBus Parameters

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V			0.8	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V	2.1		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			400	kHz	

[1] Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDxxx	Supply voltage for core, analog and single-ended LVCMOS outputs.	3.135	3.3	3.465	V	
IO Supply Voltage	VDDIO	Supply voltage for differential Low Power outputs.	0.9975	1.05-3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Commmercial range	0	25	70	°C	
		Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	$0.75xV_{DD}$		$V_{DD}+0.3$	V	
Input Mid Voltage	V_{IM}	Single-ended tri-level inputs ('_tri' suffix)	$0.4xV_{DD}$	0.5 V_{DD}	$0.6xV_{DD}$	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus	-0.3		$0.25xV_{DD}$	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F_{in}	XTAL, or X1 input	8	25	40	MHz	4
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.35	1.8	ms	1,2
SS Modulation Frequency	f_{MOD}	Allowable Frequency (Triangular Modulation)	30	31.6	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	1,2
Trise	t_R	Rise time of single-ended control inputs			5	ns	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are >200 mV

[4] The 9FGLxxP1 devices can be programmed for various input frequencies from 8 to 40MHz. The 9FGLxx41/51 devices use 25MHz.

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on, fast setting	2	3.1	4	V/ns	2,3
		Scope averaging, slow setting	1	2.2	3	V/ns	2,3
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	376.5	550	mV	1,4,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		13.8	140	mV	1,4,9
Avg. Clock Period Accuracy	T_{PERIOD_AVG}		-100		+2600	ppm	2,10,13
Absolute Period	T_{PERIOD_ABS}	Includes jitter and Spread Spectrum Modulation	9.847		10.203	ns	2,6
Jitter, Cycle to cycle	$t_{jcyc-cyc}$			23	50	ps	2
Voltage High	V_{HIGH}		660	797	850	mV	1
Voltage Low	V_{LOW}		-150	10	150		1
Absolute Max Voltage	Vmax			822	1150	mV	1,7,15
Absolute Min Voltage	Vmin		-300	-101			1,8,15
Duty Cycle	t_{DC}		45	50	55	%	2
Slew rate matching	ΔTrf			6	20	%	1,14
Skew, Output to Output	t_{sk3}	Averaging on, V_T = 50%		24	50	ps	2

[1] Measured from single-ended waveform.

[2] Measured from differential waveform.

[3] Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[6] Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation.

[7] Defined as the maximum instantaneous voltage including overshoot.

[8] Defined as the minimum instantaneous voltage including undershoot.

[9] Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.

[10] Refer to Section 4.3.7.1.1 of the PCI Express Base Specification, Revision 3.0 for information regarding PPM considerations.

[11] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2 pF.

[12] T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range.

[13] PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM, then we have an error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum Clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,800 PPM.

[14] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[15] At default SMBus amplitude settings.

Electrical Characteristics–DIF LP-HCSL Output Phase Jitter Parameters

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	IND. LIMIT	UNITS	Notes
Phase Jitter, PCI Express (Common Clock Architecture)[1]	$t_{jphPCIeG1}$	PCIe Gen 1		17	30	86	ps (p-p)	1,3,4,6
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.5	0.9	3	ps (rms)	1,3,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		1.0	1.5	3.1	ps (rms)	1,3,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.3	0.5	1	ps (rms)	1,3,6
Phase Jitter, 12k-20M	$t_{jph12k20M}$	100MHz, REF output enabled			2	N/A	ps (rms)	2,6

[1] Defined for Spread Spectrum On or Off

[2] Only defined for Spread Spectrum Off.

[3] See http://www.pcisig.com for complete specs

[4] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[5] Calculated from Intel-supplied Clock Jitter Tool

[6] Applies to all differential outputs

Electrical Characteristics–Current Consumption

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDAOP}	VDDA, All outputs active @100MHz		13	16	mA	
	I_{DDOP}	All VDD, except VDDA, All outputs active @100MHz		21	30	mA	
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I_{DDAPD}	VDDA, DIF outputs off, REF output running		0.70	1	mA	1
	I_{DDPD}	All VDD, except VDDA, DIF outputs off, REF output running		9.4	1	mA	1
Powerdown Current (Power down state and Byte 3, bit 5 = '0')	I_{DDAPD}	VDDA, all outputs off		0.72	1	mA	
	I_{DDPD}	All VDD, except VDDA, all outputs off		3.9	8	mA	

[1] This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1)

Electrical Characteristics– REF

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values		0		ppm	1,2
Clock period	T_{period}	25 MHz output		40		ns	2
Output High Voltage	V_{IH}	I_{OH} = -2mA	0.8xV_{DDREF}			V	
Output Low Voltage	V_{IL}	I_{OL} = 2mA			0.2xV_{DDREF}	V	
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 1F, V_{OH} = VDD-0.45V, V_{OL} = 0.45V	0.5	0.8	1.2	V/ns	1
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 5F, V_{OH} = VDD-0.45V, V_{OL} = 0.45V	1.0	1.5	2.0	V/ns	1,3
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 9F, V_{OH} = VDD-0.45V, V_{OL} = 0.45V	1.5	2.2	2.8	V/ns	1
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = DF, V_{OH} = VDD-0.45V, V_{OL} = 0.45V	2.2	2.9	3.5	V/ns	1
Duty Cycle	d_{t1X}	V_T = VDD/2 V	45	49.8	55	%	1,4
Duty Cycle Distortion	d_{tcd}	V_T = VDD/2 V	-0.5	0.0	+0.5	%	1,5
Jitter, cycle to cycle	$t_{jcyc-cyc}$	V_T = VDD/2 V		81	250	ps	1,4
Noise floor	t_{jdBc1k}	1kHz offset			-120	dBc	1,4
Noise floor	$t_{jdBc10k}$	10kHz offset to Nyquist			-130	dBc	1,4
Jitter, phase	t_{jphREF}	12kHz to 5MHz, DIF SSC Off			0.3	ps (rms)	1,4
Jitter, phase	t_{jphREF}	12kHz to 5MHz, DIF SSC On			1	ps (rms)	1,4

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

[3] Default SMBus Value

[4] When driven by a crystal.

[5] When driven by an external oscillator via the X1 pin, X2 should be floating.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Note: SMBus Read/Write Address is Latched on SADR pin. Unless otherwise indicated, default values are for the xx41 and xx51. P1 devices are fully factory programmable.

SMBus Table: Output Enable Register

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	DIF OE1	Output Enable	RW	Low/Low	Enabled	1
Bit 1	DIF OE0	Output Enable	RW	Low/Low	Enabled	1
Bit 0	Reserved					X

1. A low on these bits will overide the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default).

SMBus Table: SS Readback and Vhigh Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SSENRB1	SS Enable Readback Bit1	R	00' for SS_EN_tri = 0, '01' for SS_EN_tri = 'M', '11 for SS_EN_tri = '1'		Latch
Bit 6	SSENRB1	SS Enable Readback Bit0	R			Latch
Bit 5	SSEN_SWCNTRL	Enable SW control of SS	RW	SS control locked	Values in B1[4:3] control SS amount.	0
Bit 4	SSENSW1	SS Enable Software Ctl Bit1	RW[1]	00' = SS Off, '01' = -0.25% SS, '10' = Reserved, '11'= -0.5% SS		0
Bit 3	SSENSW0	SS Enable Software Ctl Bit0	RW[1]			0
Bit 2	Reserved					X
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01 = 0.7V	1
Bit 0	AMPLITUDE 0		RW	10= 0.8V	11 = 0.9V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	SLEWRATESEL DIF1	Adjust Slew Rate of DIF1	RW	Slow Setting	Fast Setting	1
Bit 1	SLEWRATESEL DIF0	Adjust Slew Rate of DIF0	RW	Slow Setting	Fast Setting	1
Bit 0	Reserved					X

Note: See "Low-Power HCSL Outputs" table for slew rates.

SMBus Table: REF Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	REF	Slew Rate Control	RW	00 = Slowest	01 = Slow	0
Bit 6			RW	10 = Fast	11 = Faster	1
Bit 5	REF Power Down Function	Wake-on-Lan Enable for REF	RW	REF disabled in Power Down	REF runs in Power Down	0
Bit 4	REF OE	REF Output Enable	RW	Disabled[1]	Enabled	1
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

1. The disabled state depends on Byte11[1:0]. '00' = Low, '01'=HiZ, '10'=Low, '11'=HIgh

Byte 4 is Reserved

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	**R**	A rev = 0000		0
Bit 6	RID2		**R**			0
Bit 5	RID1		**R**			0
Bit 4	RID0		**R**			0
Bit 3	VID3	VENDOR ID	**R**	0001 = IDT		0
Bit 2	VID2		**R**			0
Bit 1	VID1		**R**			0
Bit 0	VID0		**R**			1

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	**R**	00 = FGx, 01 = DBx, 10 = DMx, 11= DBx w/oPLL		0
Bit 6	Device Type0		**R**			0
Bit 5	Device ID5	Device ID	**R**	00010 binary or 02 hex		0
Bit 4	Device ID4		**R**			0
Bit 3	Device ID3		**R**			0
Bit 2	Device ID2		**R**			0
Bit 1	Device ID1		**R**			1
Bit 0	Device ID0		**R**			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Bytes 8 and 9 are Reserved .

SMBus Table: PLL MN Enable, PD_Restore

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	PLL M/N En	M/N Programming Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 6	Power-Down (PD) Restore	Restore Default Config. In PD	RW	Clear Config in PD	Keep Config in PD	1
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

SMBus Table: Stop State Control

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	STP[1]	True/Complement DIF Output Disable State	RW	00 = Low/Low	10 = High/Low	0
Bit 0	STP[0]		RW	01 = HiZ/HiZ	11 = Low/High	0

SMBus Table: Impedance Control

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	DIF0_imp[1]	DIF0 Zout	RW	00=33 DIF Zout	10=100 DIF Zout	See Note
Bit 6	DIF0_imp[0]	DIF0 Zout	RW	01=85 DIF Zout	11 = Reserved	
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

SMBus Table: Impedance Control

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	DIF1_imp[1]	DIF1 Zout	RW	00=33 DIF Zout	10=100 DIF Zout	See Note
Bit 2	DIF1_imp[0]	DIF1 Zout	RW	01=85 DIF Zout	11 = Reserved	
Bit 1	Reserved					X
Bit 0	Reserved					X

SMBus Table: Pull-up Pull-down Control

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	OE0_pu/pd[1]	OE0 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 6	OE0_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

SMBus Table: Pull-up Pull-down Control

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					1
Bit 5	Reserved					0
Bit 4	Reserved					1
Bit 3	OE1_pu/pd[1]	OE1 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 2	OE1_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 1	Reserved					0
Bit 0	Reserved					1

SMBus Table: Pull-up Pull-down Control

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					1
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	1
Bit 0	CKPWRGD_PD_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	0

Byte 17 is Reserved

SMBus Table: Polarity Control

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	OE1_polarity	Sets OE1 polarity	RW	Enabled when Low	Enabled when High	0
Bit 4	Reserved					0
Bit 3	OE0_polarity	Sets OE0 polarity	RW	Enabled when Low	Enabled when High	0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: Polarity Control

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	CKPWRGD_PD	Determines CKPWRGD_PD polarity	RW	Power Down when Low	Power Down when High	0

Recommended Crystal Characteristics (3225 package)

PARAMETER	VALUE	UNITS	NOTES
Frequency	25	MHz	1
Resonance Mode	Fundamental	-	1
Frequency Tolerance @ 25°C	±20	PPM Max	1
Frequency Stability, ref @ 25°C Over Operating Temperature Range	±20	PPM Max	1
Temperature Range (commerical)	0~70	°C	1
Temperature Range (industrial)	-40~85	°C	1
Equivalent Series Resistance (ESR)	50	Ω Max	1
Shunt Capacitance (C_O)	7	pF Max	1
Load Capacitance (C_L)	8	pF Max	1
Drive Level	0.3	mW Max	1
Aging per year	±5	PPM Max	1

Notes:
1. IDT 603-25-150JA4C or 603-25-150JA4I

Marking Diagrams

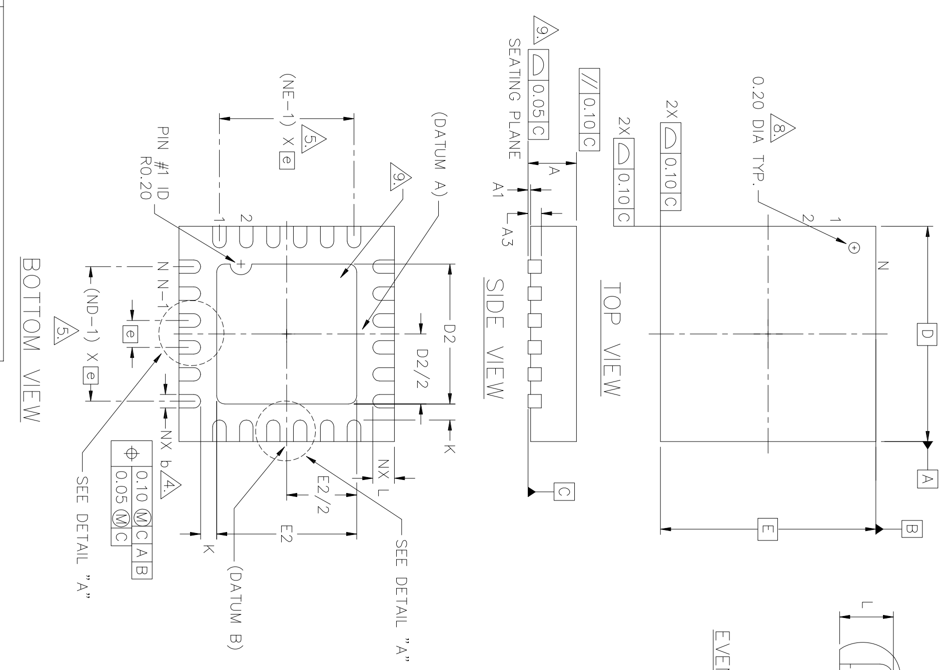
Notes:
1. “LOT” is the lot sequence number.
2. “YYWW” is the last two digits of the year and week that the part was assembled.
3. Line 2: truncated part number
4. “I” denotes industrial temperature range device.
5. “P” denotes factory programmable defaults

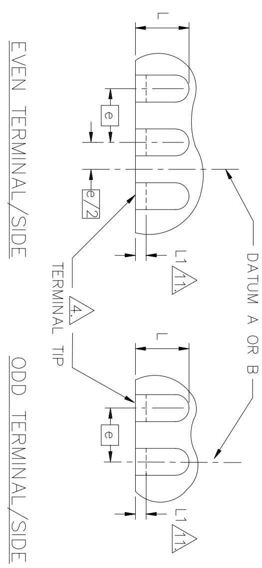
Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NLG24	62	°C/W	1
	θ_{Jb}	Junction to Base		5.4	°C/W	1
	θ_{JA0}	Junction to Air, still air		50	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		43	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		39	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		38	°C/W	1

[1]ePad soldered to board

Package Outline and Package Dimensions (NLG24)





NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220
11. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L1) MAYBE PRESENT
12. PULLBACK DESIGN OPTION IS FOR 0.50mm NOMINAL LANDLENGTH ONLY.

SYMBOL	MIN.	NOM.	MAX.
e		0.50 BSC.	
N		24	
ND		6	
NE		6	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
D2	2.30	2.45	2.60
E2	2.30	2.45	2.60

SYMBOL	DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.90	1.0	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
θ	0	——	12	2
K		0.20 MIN.		
D		4.0 BSC		
E		4.0 BSC		
L1		0.15 mm MAX		11

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/15/08	RAC
01	ADD LAND PATTERN	11/19/10	JG

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±

APPROVALS DATE
DRAWN RAC 10/15/08
CHECKED

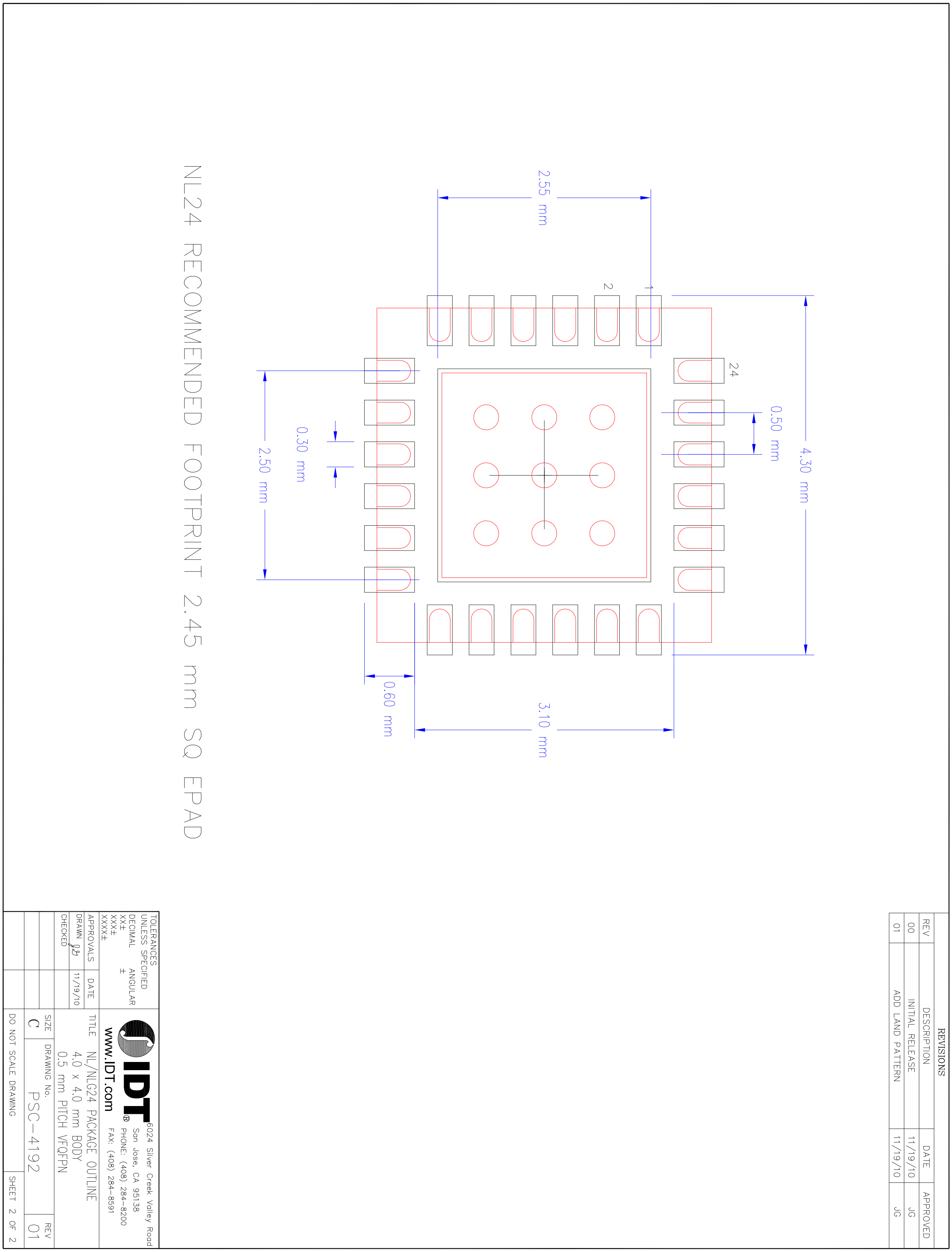
IDT www.IDT.com 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591

TITLE NL/NLG24 PACKAGE OUTLINE 4.0 x 4.0 mm BODY 0.5 mm PITCH QFN

SIZE C DRAWING No. PSC-4192 REV 01

DO NOT SCALE DRAWING SHEET 1 OF 2

Package Outline and Package Dimensions (NLG24), cont.



Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9FGL0241AKILF	Trays	24-pin VFQFPN	-40 to +85° C
9FGL0241AKILFT	Tape and Reel	24-pin VFQFPN	-40 to +85° C
9FGL0251AKILF	Trays	24-pin VFQFPN	-40 to +85° C
9FGL0251AKILFT	Tape and Reel	24-pin VFQFPN	-40 to +85° C
9FGL02P1A000KILF	Trays	24-pin VFQFPN	-40 to +85° C
9FGL02P1A000KILFT	Tape and Reel	24-pin VFQFPN	-40 to +85° C
9FGL02P1AxxxKILF	Trays	24-pin VFQFPN	-40 to +85° C
9FGL02P1AxxxKILFT	Tape and Reel	24-pin VFQFPN	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"A" is the device revision designator (will not correlate with the datasheet revision).
"000" is a blank device.
"xxx" is a unique factory assigned number to identify a particular default configuration.

Revision History

Rev.	Issue Date	Intiator	Description	Page #
A	7/17/2015	RDW	1. Update electrical tables with characterization data. 2. Minor formatting updates for readability and consistency. 3. Added I-temp crystal part number to crystal characteristics table 4. Added reference to AN-891 for terminating to other logic families. 5. Removed LVDS termination drawing (now in AN-891) 6. Move to final.	Various

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