# 1.8V CMOS 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

# IDT74AUCH16245

# FEATURES:

- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.8V Optimized
- 0.8V to 2.7V Operating Range
- · Inputs/outputs tolerant up to 3.6V
- Output drivers: ±9mA @ VDD = 2.3V
- · Supports hot insertion
- Available in TSSOP package

### **APPLICATIONS:**

- · High performance, low voltage communications systems
- · High performance, low voltage computing systems

# DESCRIPTION:

This 16-bit bus transceiver is built using advanced CMOS technology. The AUCH16245 is designed specifically for asynchronous communications between data buses. The control function implementation minimizes external timing requirements.

This device can be used as one 16-bit transceiver or two 8-bit transceivers. It allows data transmission from A bus to B bus or from B bus to A bus, depending on the logic level at the direction-control (DIR) input. The output-enable  $\overline{(OE)}$  input can be used to disable the device so that the buses are effectively isolated.

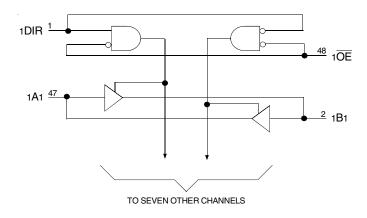
This device is fully specified for partial power-down applications using IOFF. The IOFF circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

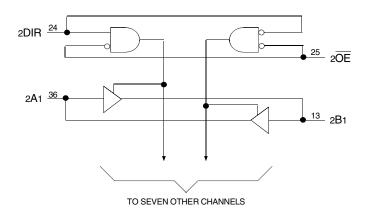
The AUCH16245 is designed with a  $\pm$ 9mA output driver. This driver is capable of driving a moderate load while maintaining speed performance.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to Vod through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The AUCH16245 data I/Os have bus-hold, which retains the last value whenever the I/O goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/pull-down resistors. Control inputs do not have bus-hold and should not be allowed to float.

# FUNCTIONAL BLOCK DIAGRAM



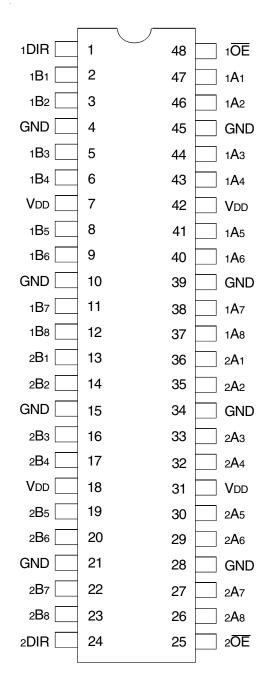


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### FEBRUARY 2006

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### PINCONFIGURATION



#### TSSOP TOP VIEW

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description		Max	Unit
VTERM	Terminal Voltage with Respec	t to GND	-0.5 to +3.6	V
	(all input and VDD terminals)			
VTERM	Terminal Voltage with Respec	t to GND	-0.5 to +3.6	V
	(any I/O or Output terminals ir	n high-		
	impedance or power-off state)			
VTERM	Terminal Voltage with Respec	t to GND	-0.5 to +3.6	V
	(any I/O or Output terminals ir	n high or		
	low state)			
Tstg	Storage Temperature		-65 to +150	°C
Ιουτ	Continuous DC Output Currer	nt	±20	mA
Ік	Continuous Clamp Current	Vi > Vdd	+50	mA
		-50		
Іок	Continuous Clamp Current, V	-50	mA	
Idd	Continuous Current through	±100	mA	
Iss	each VDD or GND			

NOTE:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### CAPACITANCE (TA = +25°C, f = 1.0MHz, VDD = 2.5V)

Symbol	Parameter	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance <sup>(1)</sup>	VIN = 0V	3		pF
CI/O	I/O Port Capacitance <sup>(2)</sup>	VIN = 0V	8		pF

NOTES:

1. Applies to the Control Inputs.

2. Applies to ports A and B.

# PINDESCRIPTION

Pin Names	Description	
xŌĒ	3-State Output Enable Inputs (Active Low)	
xDIR	Direction Control Inputs	
хАх	A Side Inputs or 3-State Outputs <sup>(1)</sup>	
хВх	B Side Inputs or 3-State Outputs <sup>(1)</sup>	

NOTE:

1. These pins have "bus-hold". All other pins are standard outputs, inputs, or I/Os.

# FUNCTION TABLE (EACH 8-BIT SECTION)<sup>(1)</sup>

Inp	outs	
xOE	xDIR	Outputs
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	Х	Z

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Z = High-Impedance

# RECOMMENDED OPERATING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vdd	Supply Voltage		0.8	2.7	V
		VDD = 0.8V	Vdd	_	
		VDD = 1.1V to 1.3V	0.65 x Vdd	_	1
Vih	Input HIGH Voltage Level	VDD = 1.4V to 1.6V	0.65 x Vdd	_	V
		VDD = 1.65V to 1.95V	0.65 x Vdd	-	1
		VDD = 2.3V to 2.7V	1.7	-	1
		VDD = 0.8V	-	0	
		VDD = 1.1V to 1.3V	-	0.35 x Vdd	1
VIL	Input LOW Voltage Level	VDD = 1.4V to 1.6V	_	0.35 x Vdd	l v
		VDD = 1.65V to 1.95V	-	0.35 x Vdd	
		VDD = 2.3V to 2.7V	_	0.7	]
Vi	InputVoltage		0	2.7	V
Vo	Output Voltage	Active State	0	Vdd	V
		3-State	0	2.7	
		VDD = 0.8V	_	-0.7	
		VDD = 1.1V	_	-3	]
Іон	HIGH Level Output Current	VDD = 1.4V	_	-5	mA
		VDD = 1.65V	-	-8	]
		VDD = 2.3V	-	-9	1
		VDD = 0.8V	-	0.7	
		VDD = 1.1V	-	3	1
IOL	LOW Level Output Current	VDD = 1.4V	-	5	mA
		VDD = 1.65V	_	8	
		VDD = 2.3V	-	9	
$\Delta t/\Delta v$	Input Transition Rise or Fall Time		_	5	ns/V
TA	Operating Free-Air Temperature		-40	+85	°C

NOTE:

1. All unused inputs of the device must be held at  $\mathsf{V}_\mathsf{DD}$  or GND to ensure proper operation.

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE<sup>(1)</sup>

 $Following\,Conditions\,Apply\,Unless\,Otherwise\,Specified:$ 

Operating Conditions:  $TA = -40^{\circ}C$  to  $+85^{\circ}C$ 

Symbol	Parameter		Test Conditions		Min.	Тур.	Max.	Unit
Ін	Input HIGH or LOW Current	Data Inputs	VDD = 2.7V, VI = VDD or GN	D	—	_	±10	μA
lı.		Control Inputs			_	_	±5	
loff	Input/Output Power Off Leaka	age	VDD = $0V$ , VIN or VO $\leq 2.7V$		—	_	±10	μA
IOZH <sup>(2)</sup>	High Impedance Output Curr	ent	Vdd = 2.7V	Vo = Vdd	_	_	±10	μA
IOZL <sup>(2)</sup>	(3-State Output Pins)			Vo = GND	—	—	±10	
Iddl	Quiescent Power Supply Cu	rrent	VDD = 0.8V to 2.7V		—	_	20	μA
Iddh			VIN = GND  or  VDD					
Iddz								

#### NOTES:

1. All unused inputs of the device must be held at  $V_{\text{DD}}$  or GND to ensure proper operation.

<sup>2.</sup> For the I/O ports, the parameters lozH and lozL include the input leakage current.

# **BUS-HOLD CHARACTERISTICS**

Symbol	Parameter <sup>(1)</sup>	Test Conditi	ons	Min.	Тур.	Max.	Unit
		Vdd = 1.1V	VI = 0.8V	-10	_	_	
			VI = 0.35V	10	_	_	
Івнн	Bus-Hold Input Sustain Current	Vdd = 1.4V	VI = 0.9V	-15	—	_	
IBHL			VI = 0.47V	15	—	_	
		Vdd = 1.65V	VI = 1.07V	-20	_		μA
			VI = 0.57V	20			
		Vdd = 2.3V	VI = 1.7V	-40	—	_	
			VI = 0.7V	40	—	_	
		Vdd = 1.3V		_	—	±125	
Івнно	Bus-Hold Input Overdrive Current	Vdd = 1.6V	VI = 0 to VDD	_	—	±175	μA
Ibhlo		Vdd = 1.95V		_	—	±250	
		Vdd = 2.7V		—	—	±400	

NOTE:

1. Pins with Bus-hold are identified in the pin description.

# OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditior	IS <sup>(1)</sup>	Min.	Тур.	Max.	Unit
Vон	Output HIGH Voltage	Vdd = 0.8V - 2.7V	Іон = –100μА	Vdd - 0.1	—	-	
		Vdd = 0.8V	Iон = -0.7mA	—	0.55	—	
		VDD = 1.1V <sup>(2)</sup>	Iон = -3mA	0.8	_	—	V
		VDD = 1.4V <sup>(3)</sup>	Iон = -5mA	1	_	—	
		VDD = 1.65V <sup>(4)</sup>	Iон = -8mA	1.2	—	_	
		VDD = 2.3V <sup>(5)</sup>	Iон = <b>-9mA</b>	1.8	—	—	
Vol	Output LOW Voltage	Vdd = 0.8V - 2.7V	Іон = 100μА	—	-	0.2	
		Vdd = 0.8V	IOL = 0.7mA	_	0.25	_	
		VDD = 1.1V <sup>(2)</sup>	IOL = 3mA	_		0.3	V
		$VDD = 1.4V^{(3)}$	Iol = 5mA	_	—	0.4	
		VDD = 1.65V <sup>(4)</sup>	IOL = 8mA	—	-	0.45	
		VDD = 2.3V <sup>(5)</sup>	Iон = 9mA	—	_	0.6	

NOTES:

1. VIL and VIH must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate VDD range. TA = -40°C to +85°C.

2. Demonstrates operation for nominal VDD = 1.2V.

3. Demonstrates operation for nominal VDD = 1.5V.

4. Demonstrates operation for nominal VDD = 1.8V.

5. Demonstrates operation for nominal VDD = 2.5V.

#### IDT74AUCH16245 1.8V CMOS 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

**INDUSTRIAL TEMPERATURE RANGE** 

# OPERATING CHARACTERISTICS, $TA = 25^{\circ}C$

Symbol	Parameter	Test Conditions	VDD = 0.8V	VDD = 1.2V	Vdd = 1.5V	Vdd = 1.8V	VDD = 2.5V	Unit
Cpd	Power Dissipation Capacitance Outputs Enabled	CL = 0pF f = 10MHz	22	23	24	25	29	pF
Cpd	Power Dissipation Capacitance Outputs Disabled		1	1	1	1	1	pF

# SWITCHING CHARACTERISTICS<sup>(1)</sup>

		VDD = 0.8V	Vdd = 1.2	2V±0.1V	Vdd = 1.	5V±0.1V	Vdd	= 1.8V±0.	15V	Vdd = 2.	5V±0.2V	
Symbol	Parameter	Тур.	Min.	Max.	Min.	Max.	Min.	Тур.	Max.	Min.	Max.	Unit
<b>t</b> PLH	Propagation Delay	5.6	0.5	3.1	0.5	2	0.5	1.5	2	0.4	1.9	ns
<b>t</b> PHL	xAx to xBx or xBx to xAx											
tрzн	Output Enable Time	10	0.7	4.6	0.7	3.1	0.7	2.1	3.1	0.7	2.6	ns
tPZL	xOE to xAx or xBx											
tPHZ tPLZ	Output Disable Time xOE to xAx or xBx	12.8	0.8	6.8	0.8	5	0.8	3.4	4.8	0.5	2.9	ns

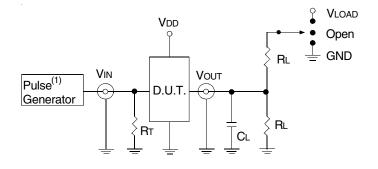
NOTE:

1. See TEST CIRCUITS AND WAVEFORMS. TA =  $-40^{\circ}$ C to  $+85^{\circ}$ C.

# **TEST CIRCUITS AND WAVEFORMS**

### TEST CONDITIONS<sup>(1)</sup>

Symbol	VDD = 0.8V	Vdd = 1.2V±0.1V	$V_{DD} = 1.5V \pm 0.1V$	VDD = 1.8V±0.15V	VDD = 2.5V±0.2V	Unit
VLOAD	2xVdd	2xVdd	2xVdd	2xVdd	2xVdd	V
VT	Vdd/2	Vdd/2	Vdd/2	Vdd/2	Vdd/2	V
VLZ	100	100	100	150	150	mV
VHZ	100	100	100	150	150	mV
R∟	2	2	2	1	0.5	KΩ
CL	15	15	15	30	30	pF



### Test Circuits for All Outputs

#### **DEFINITIONS:**

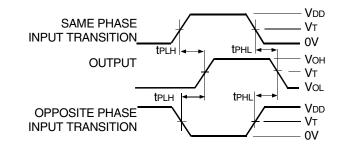
CL = Load capacitance: includes jig and probe capacitance.

 $\mathsf{R}\mathsf{T}$  = Termination resistance: should be equal to  $\mathsf{Z}\mathsf{o}\mathsf{u}\mathsf{T}$  of the Pulse Generator. NOTE:

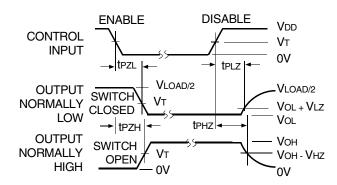
1. Pulse Generator for All Pulses: Rate  $\leq$  10MHz; Slew Rate  $\geq$  1V/ns.

# **SWITCH POSITION**

Test	Switch
Open Drain Disable Low Enable Low	Vload
Disable High Enable High	GND
All Other Tests	Open



### Propagation Delay

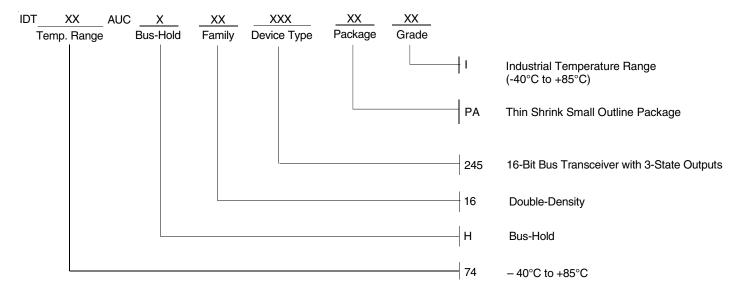


#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

#### Enable and Disable Times

# ORDERING INFORMATION





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