T-43-25

GEC PLESSEY
SEMICONDUCTORS

SL2363 & SL2364

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable fT of 2.5GHz, (typically 5GHz).

FEATURES

- Complete Dual Long-Tailed Pair in One Package
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ORDERING INFORMATION

SL2363 C CM
SL2363 CB CM
SL2364 C DC
SL2364 C DP
SL2364 C LC
SL2364 C MP
SL2364 CB DC

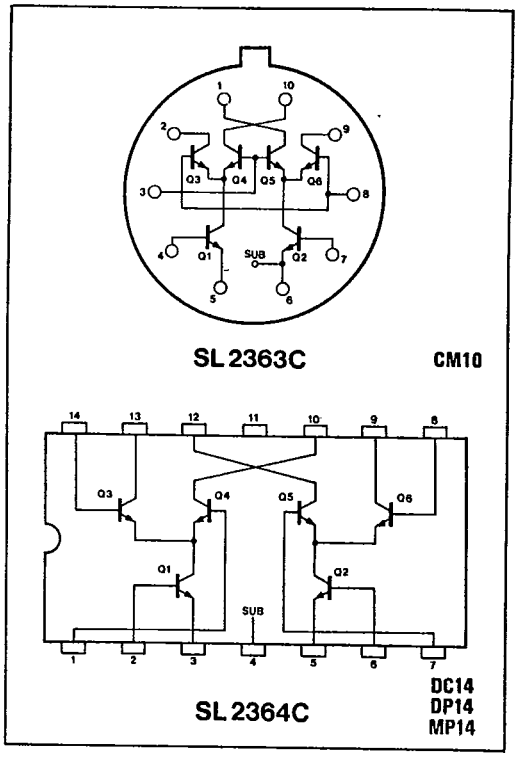

Fig. 1 Pin connections for CM, DC, DP and MP packages - top view. NOTE: See Fig. 4 for pinout of SL2364 in LC package

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
h_{FE}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$		-1.7		mV/°C	I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1 ΔV_{BE} applies to $V_{BEQ3} - V_{BEQ4}$ and $V_{BEQ5} - V_{BEQ6}$

TYPICAL CHARACTERISTICS

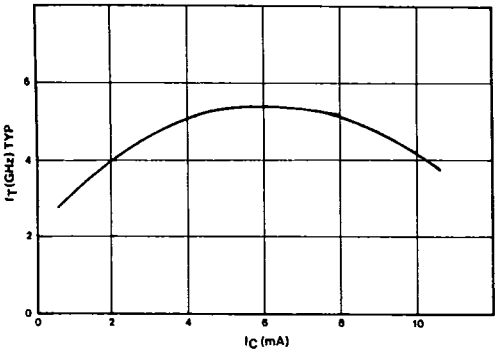

Fig. 2 Collector current

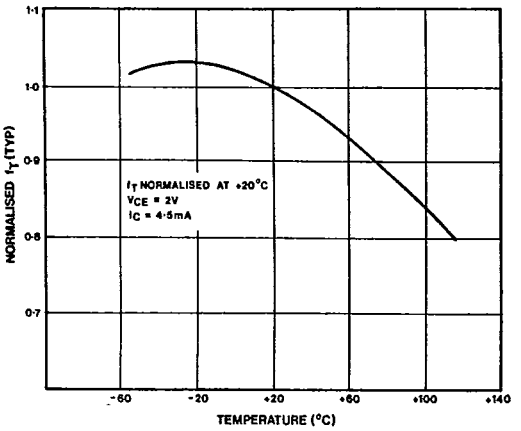

Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature	−55°C to +150°C
Maximum junction temperature	+150°C
Package thermal resistance (°C/W):	
Chip to case	65 (CM10)
Chip to ambient	225 (CM10) 175 (DP14)

V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V, IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

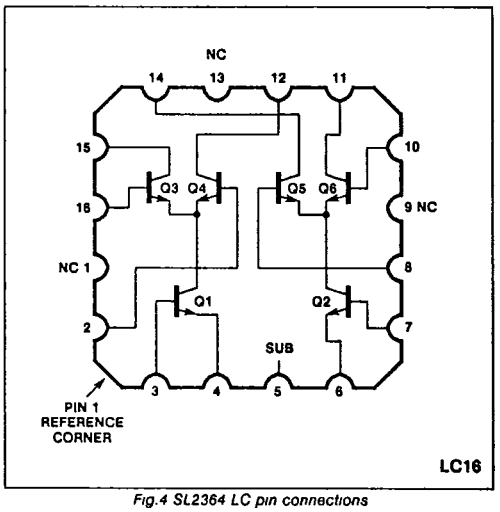

Fig.4 SL2364 LC pin connections